Three Dimensional IC Package Module

ABSTRACT

A high performance package is described where semiconductor chips of varying sizes are stacked on one another and an interface substrate. Inter chip communications is facilitated by chip-to-chip vias formed through the material of each chip. The chip-to-chip vias are formed from the back of a chip through the silicon substrate stopping at the first level of metallization and invoking the wiring of the chip to complete the signal path including to another chip. Signal and power can travel the full length of a via column from the bottom chip to the top chip, or the wiring within the chips can interrupt the signal flow and form interstitial connections. To accommodate cooling, the chips are ordered in size from the largest at the bottom of the stack to the smallest at the top, allowing heat sinks to be attached to each chip.

FIG. 2b