

MEMORY CELL IN WHICH THE CHANNEL PASSES THROUGH A BURIED
DIELECTRIC LAYER

ABSTRACT

The invention relates, according to a first aspect, to a memory cell comprising:

- a semiconductor-on-insulator substrate comprising a thin layer of semiconductor material separated from a base substrate by an insulating layer (BOX);
- an FET transistor comprising a source region (S) and a drain region (D) that are arranged at least essentially in the thin layer of the semiconductor-on-insulator substrate, a channel (C) in which a trench is made, and a gate region (G) in the trench,

characterized in that the trench extends into the depth of the base substrate beyond the insulating layer (BOX) and in that the channel extends between the source region and the drain region at least essentially beneath the insulating layer. The invention also extends to a memory array comprising a plurality of memory cells according to the first aspect of the invention and also to a process for fabricating such a memory cell.

FIGURE 2a.