

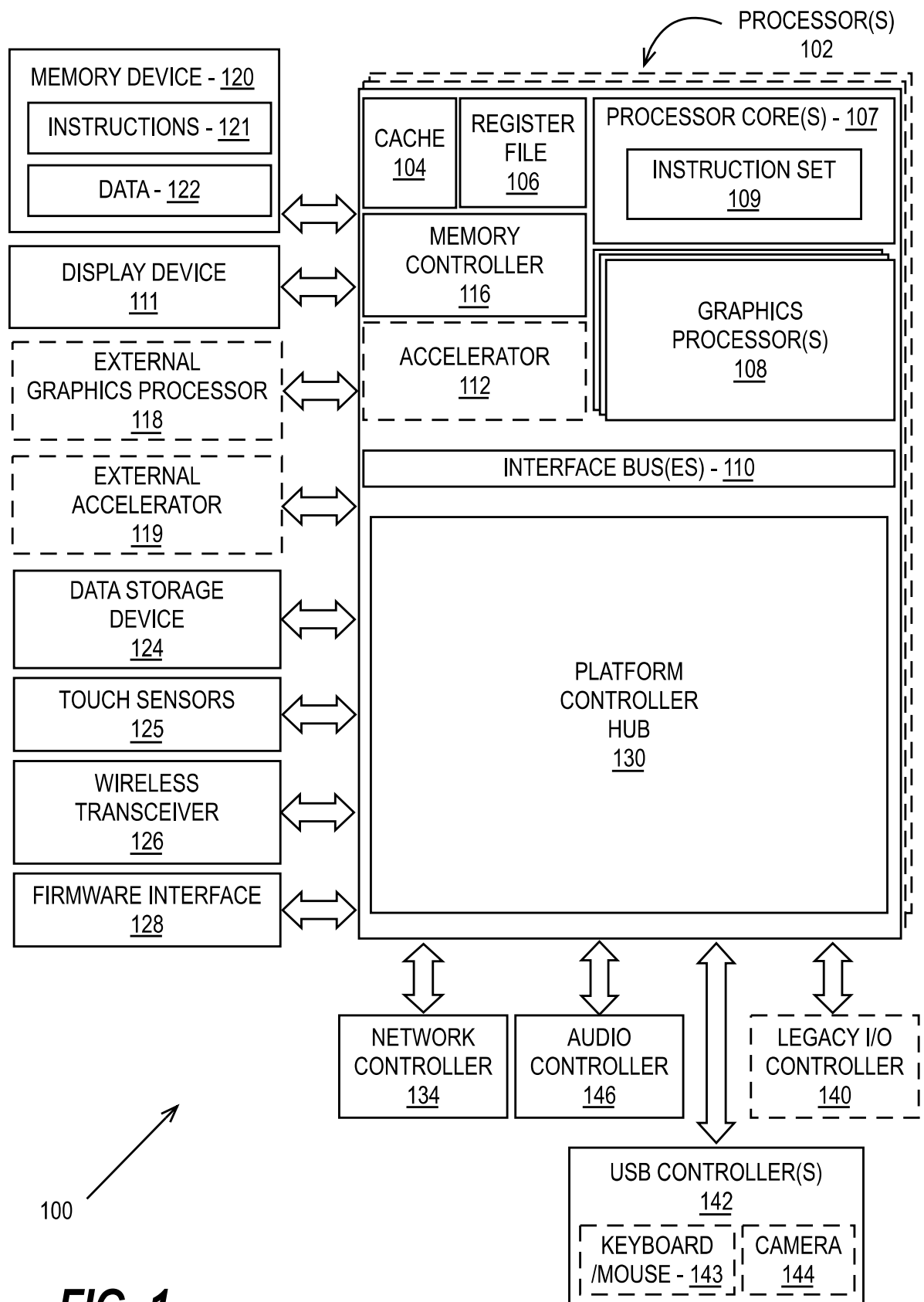


FIG. 1

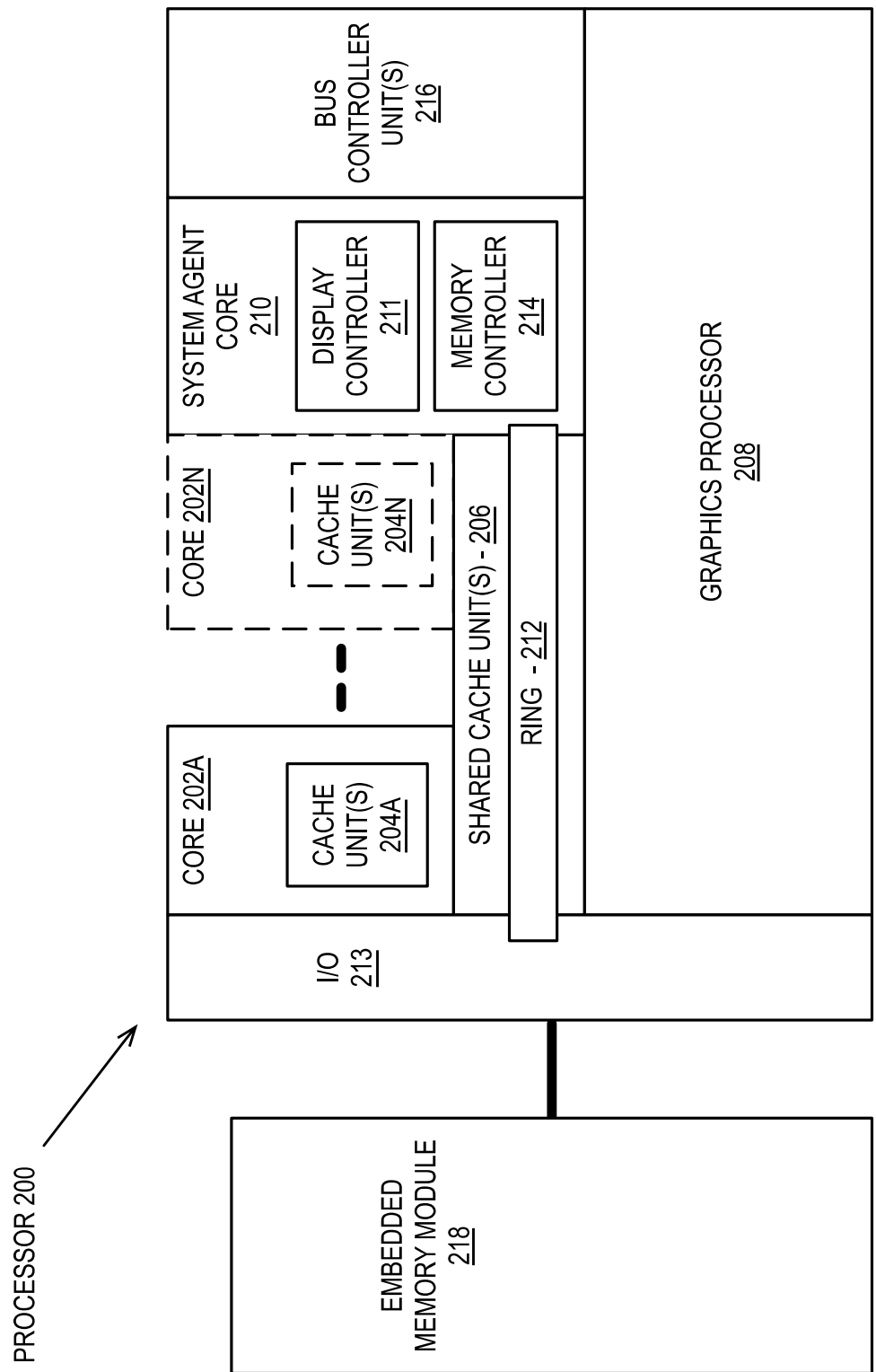


FIG. 2A

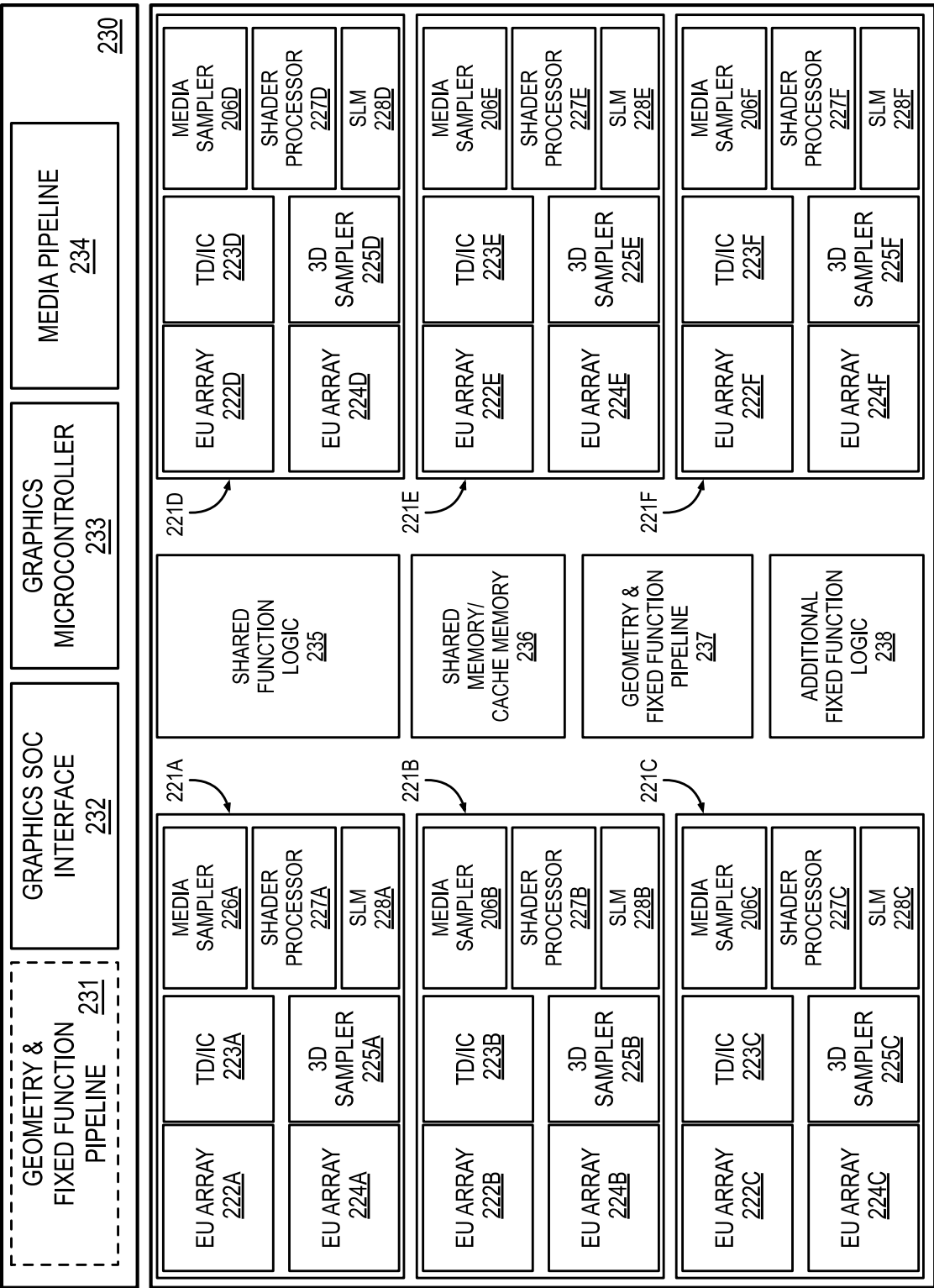
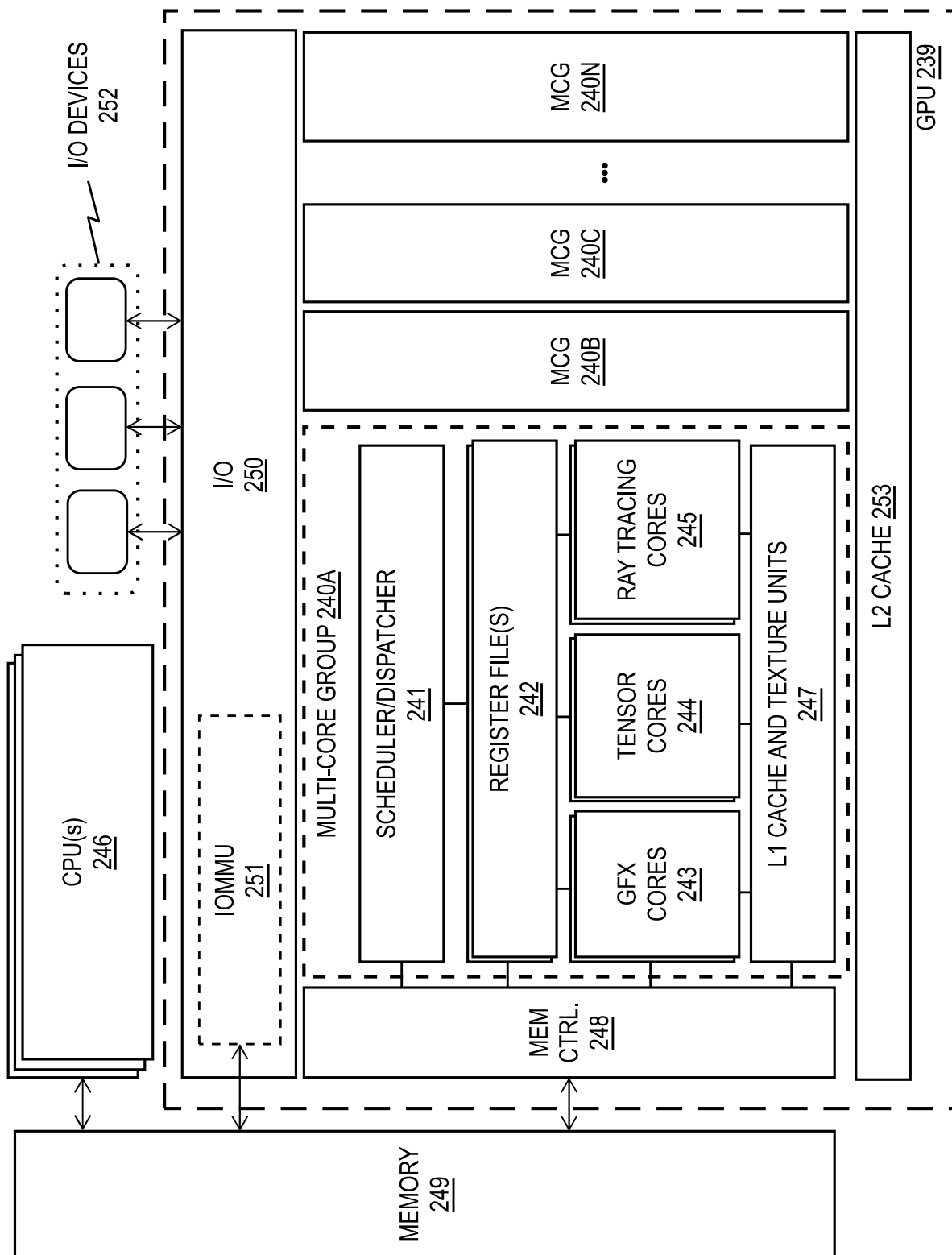
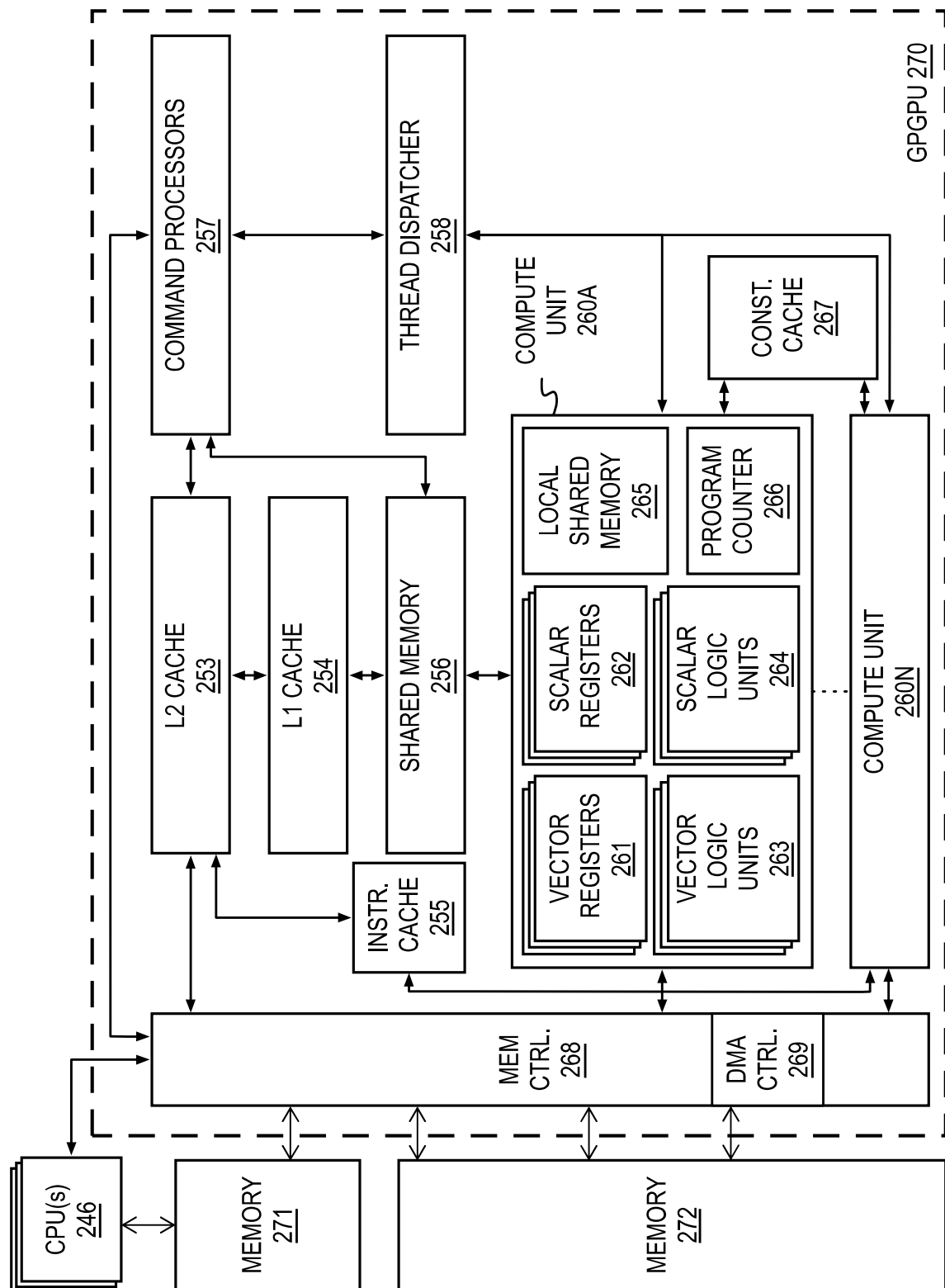


FIG. 2B





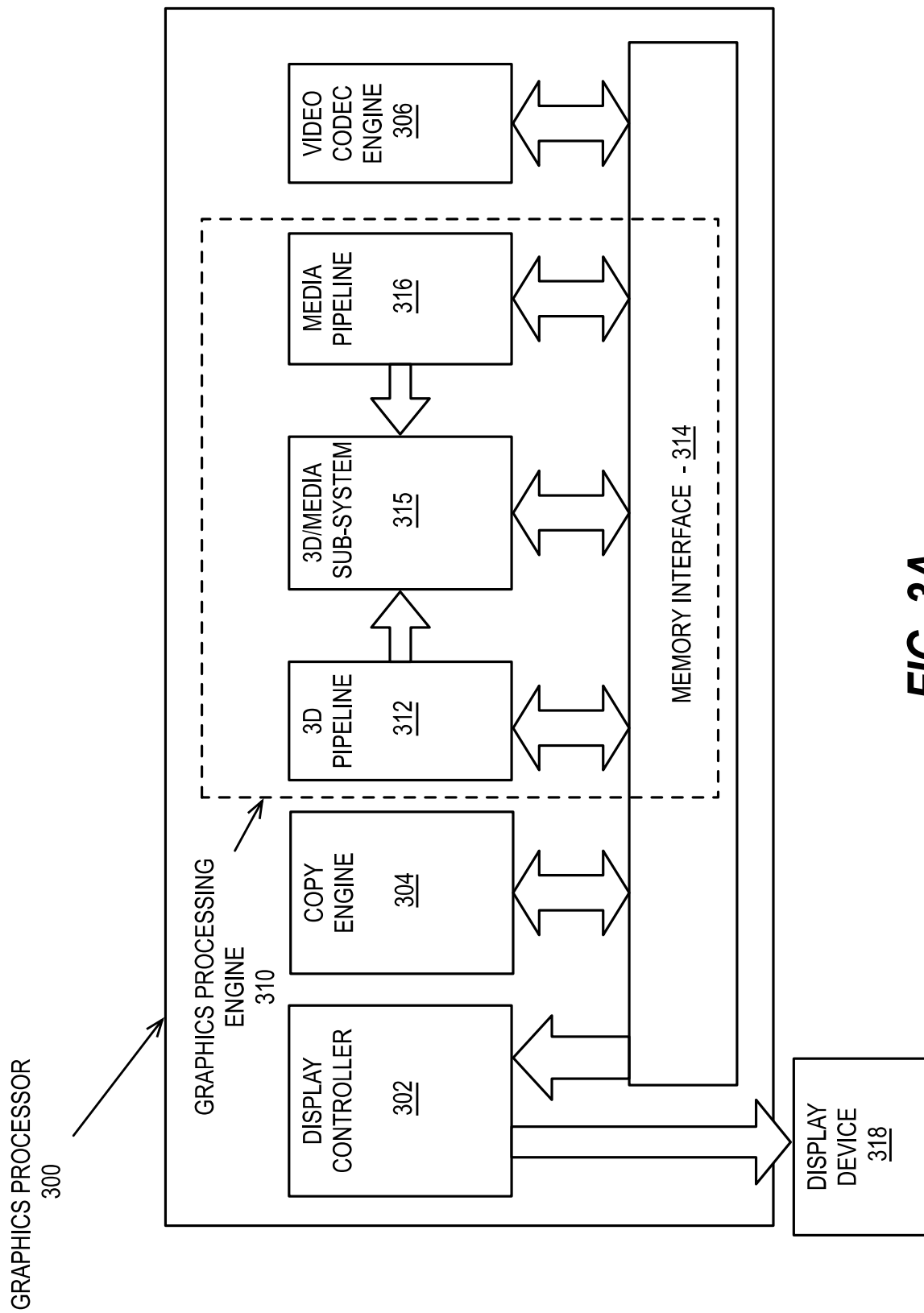


FIG. 3A

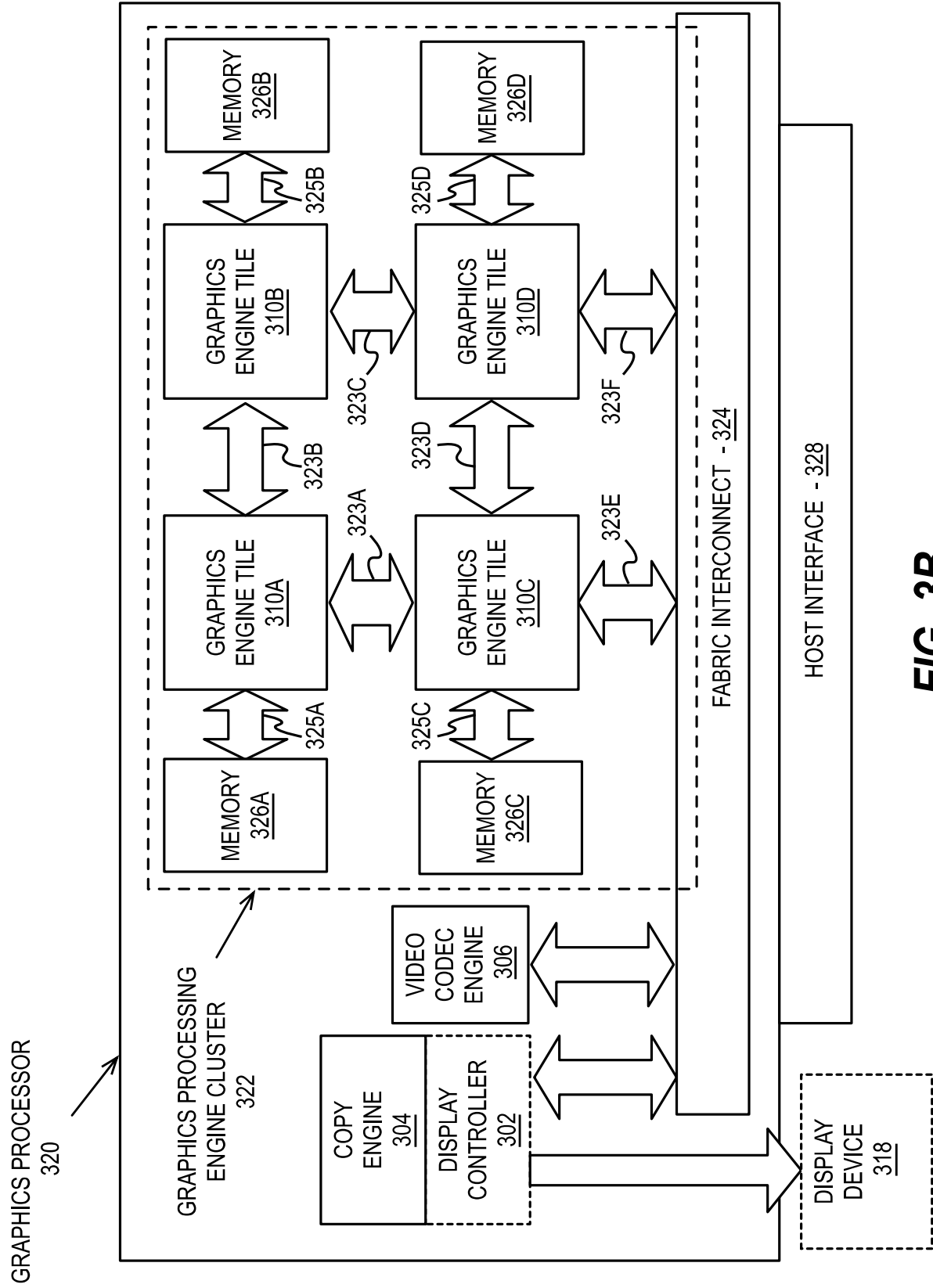


FIG. 3B

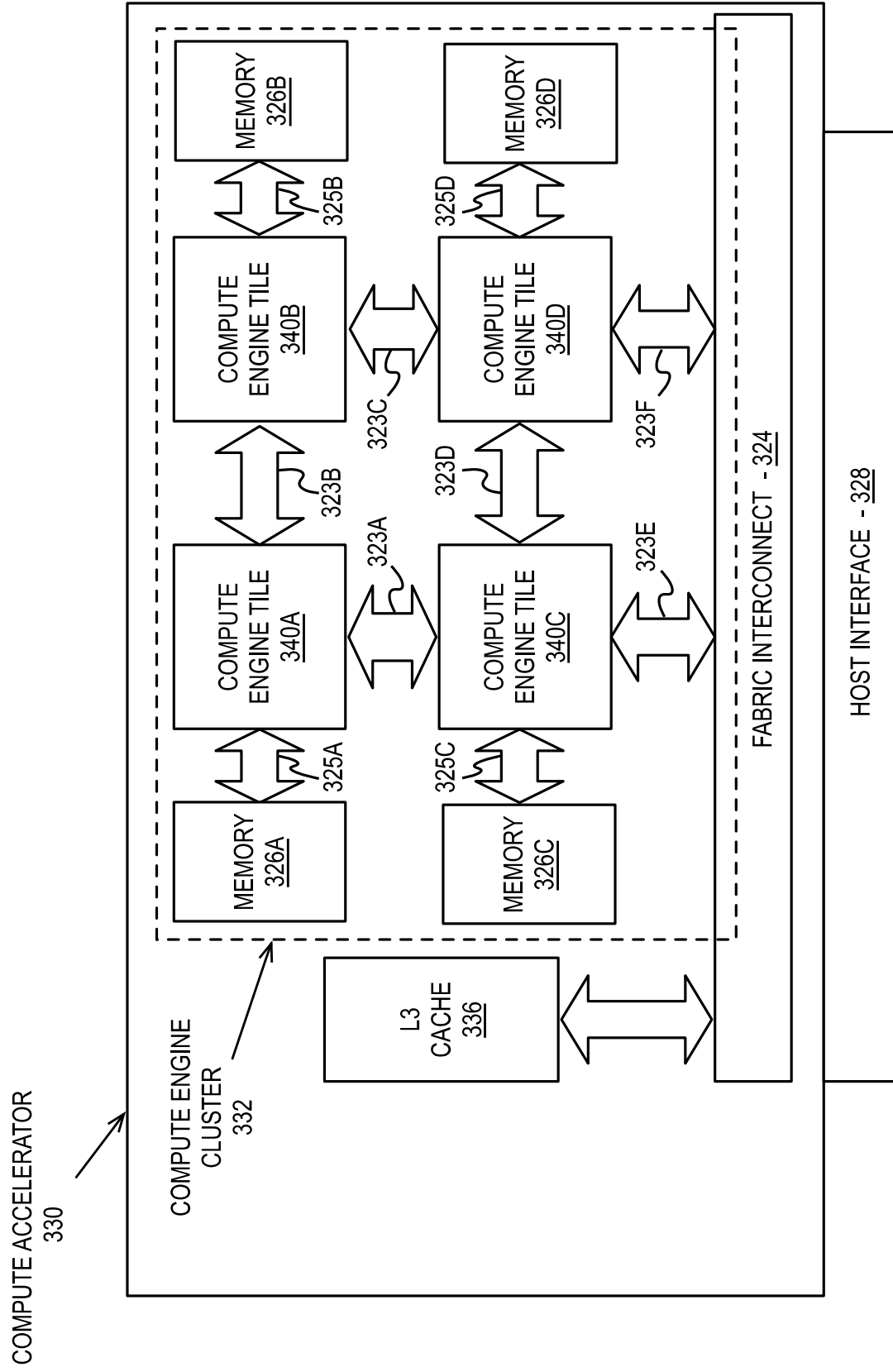


FIG. 3C

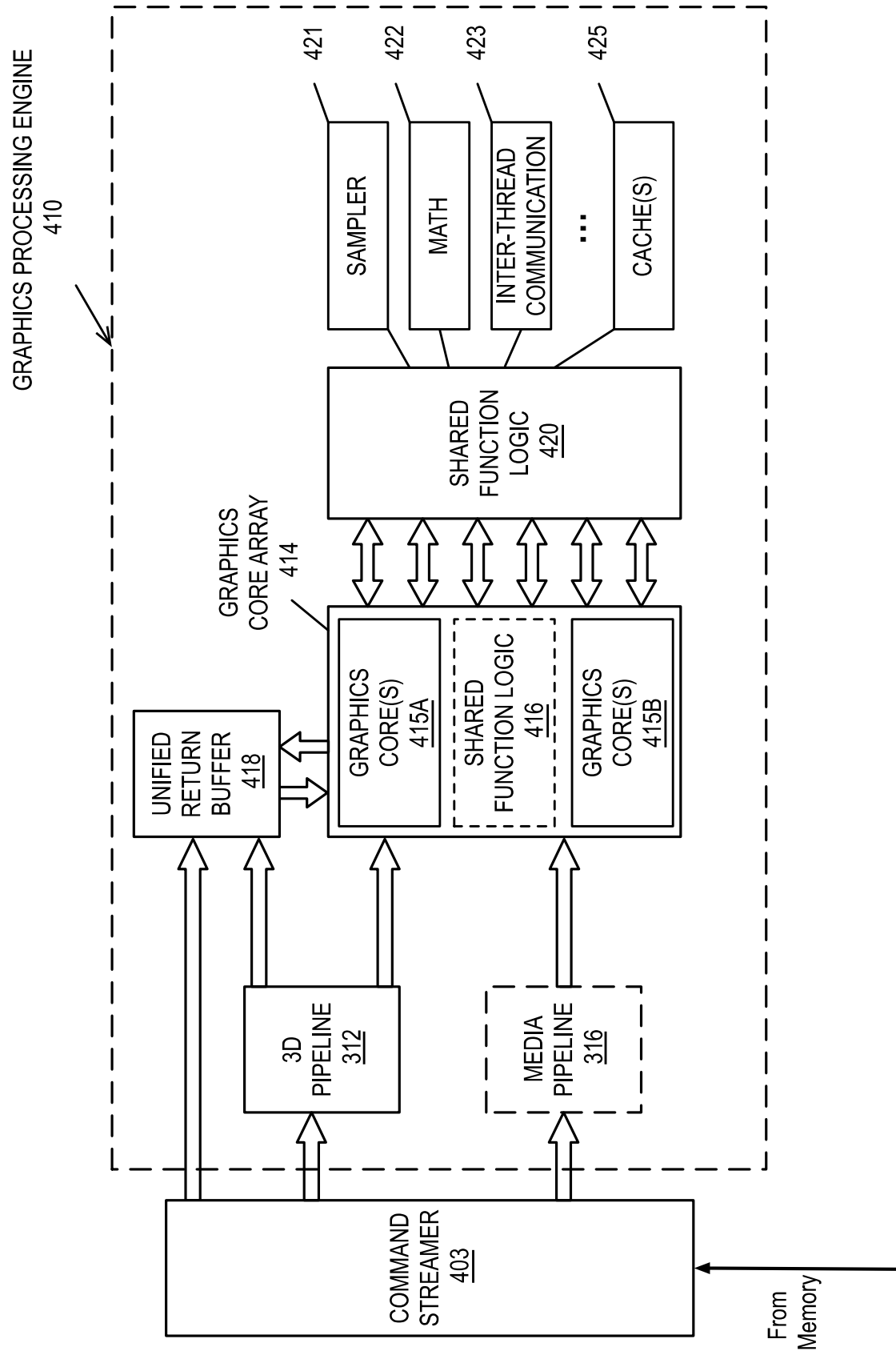


FIG. 4

EXECUTION LOGIC
500

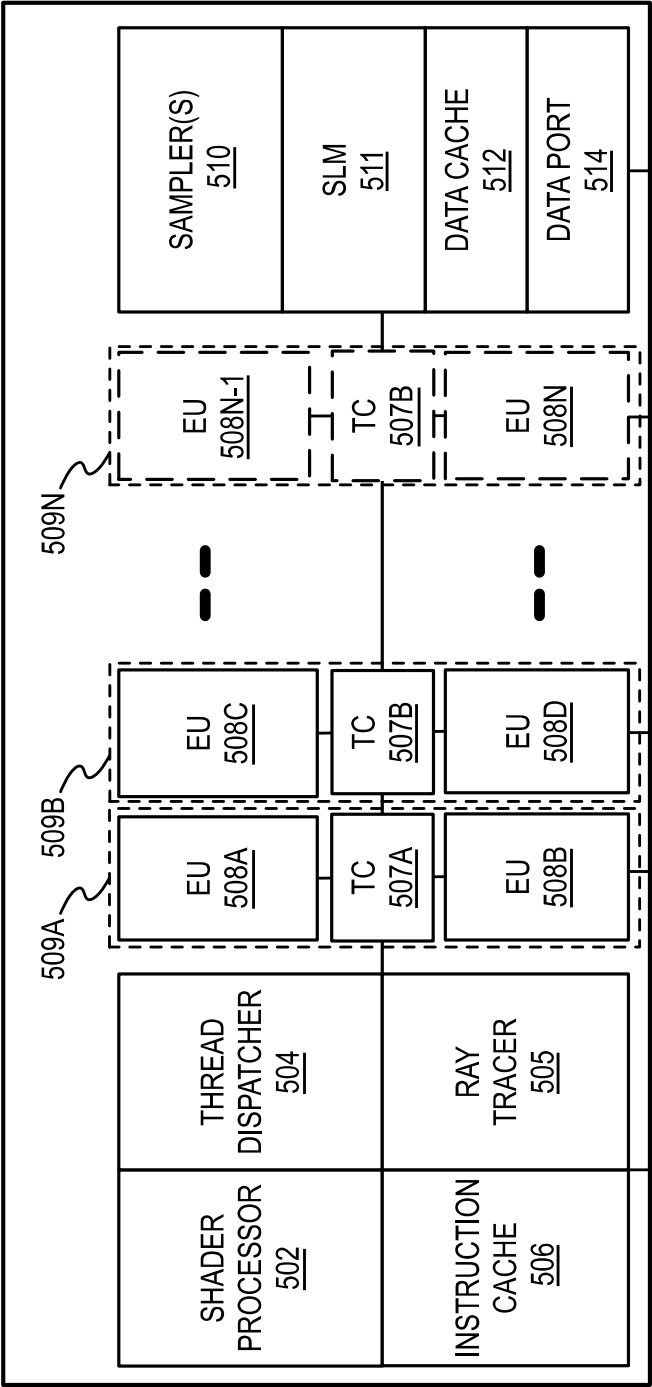


FIG. 5A

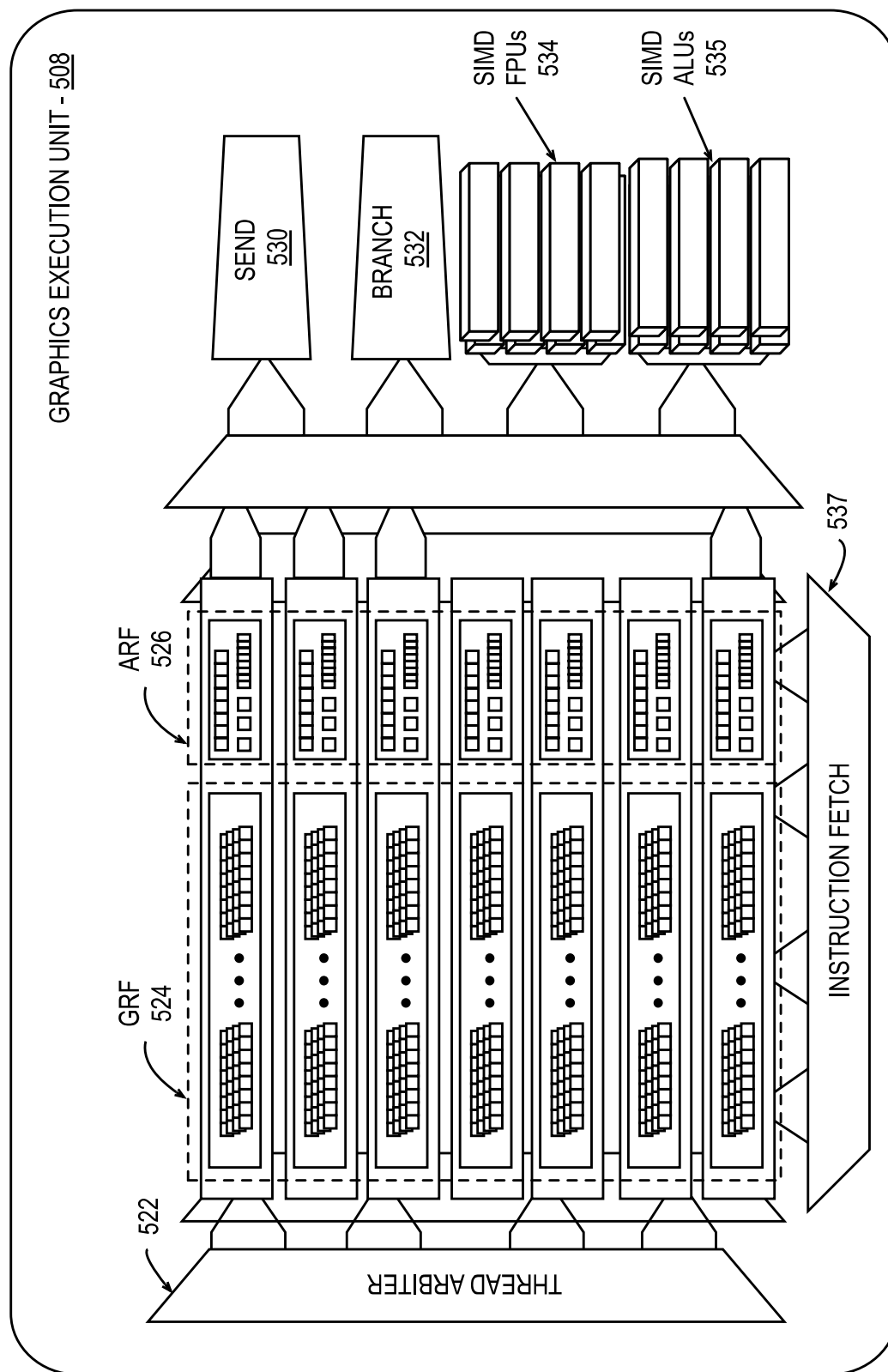


FIG. 5B

EXECUTION UNIT
600

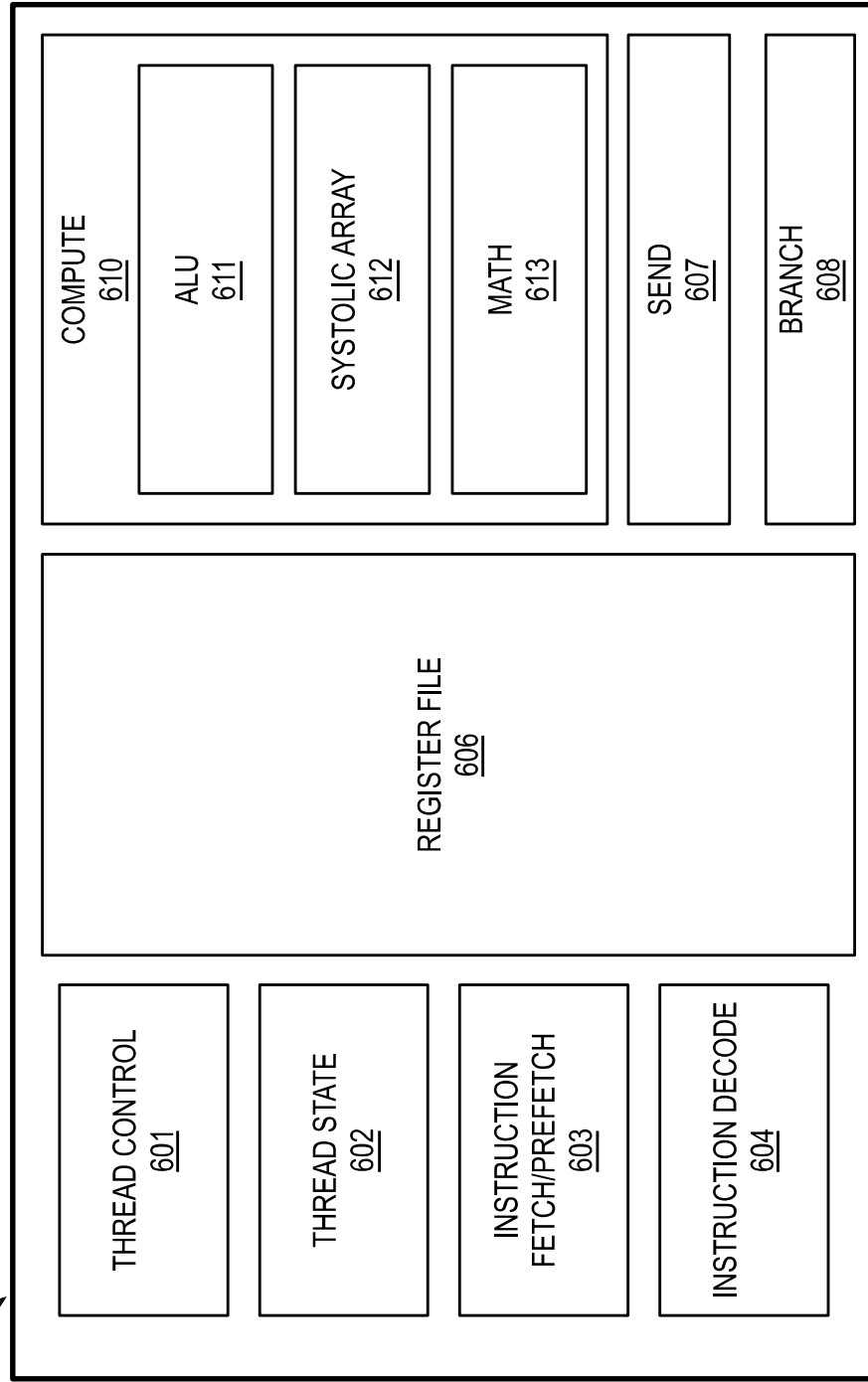


FIG. 6

GRAPHICS PROCESSOR INSTRUCTION FORMATS

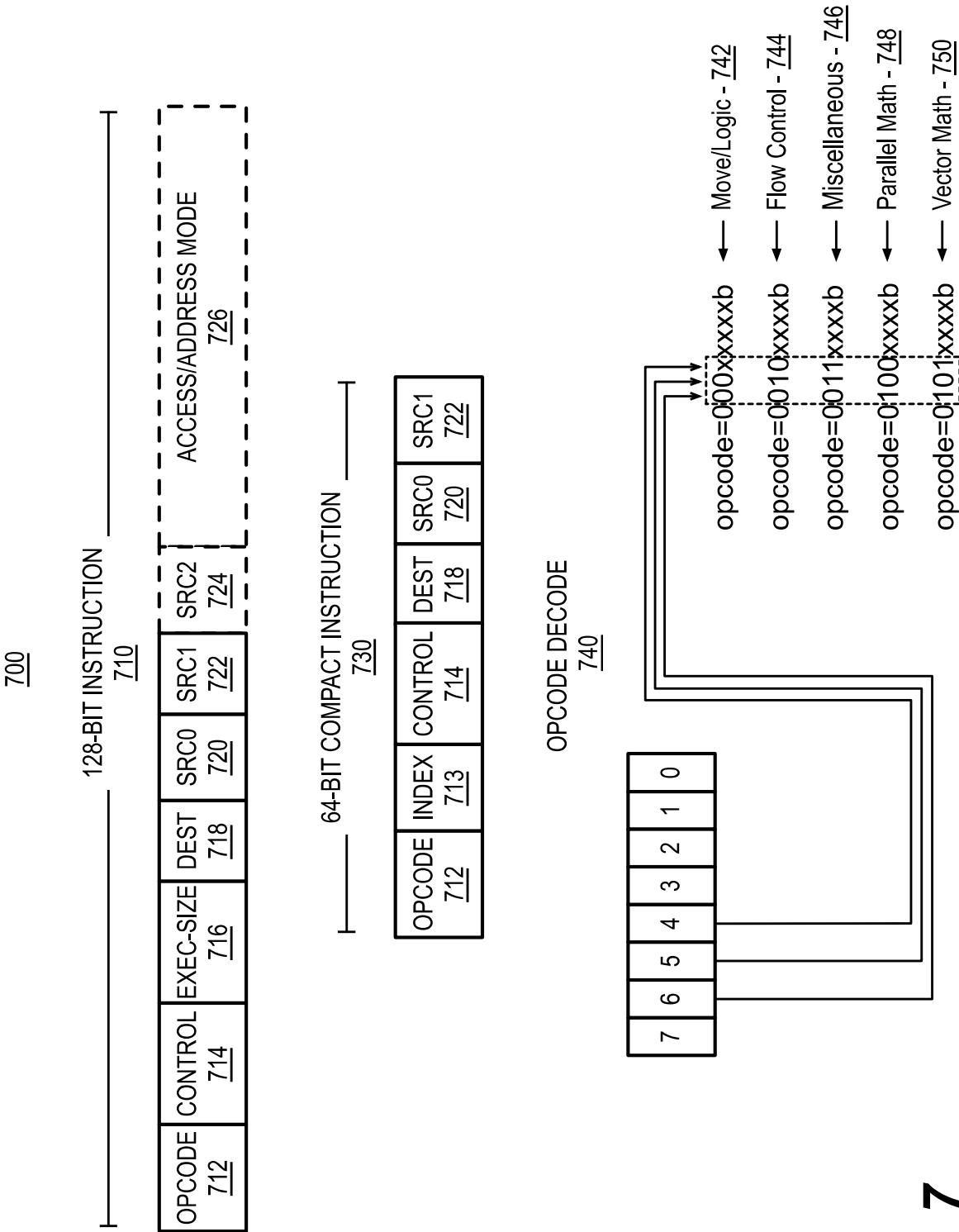


FIG. 7

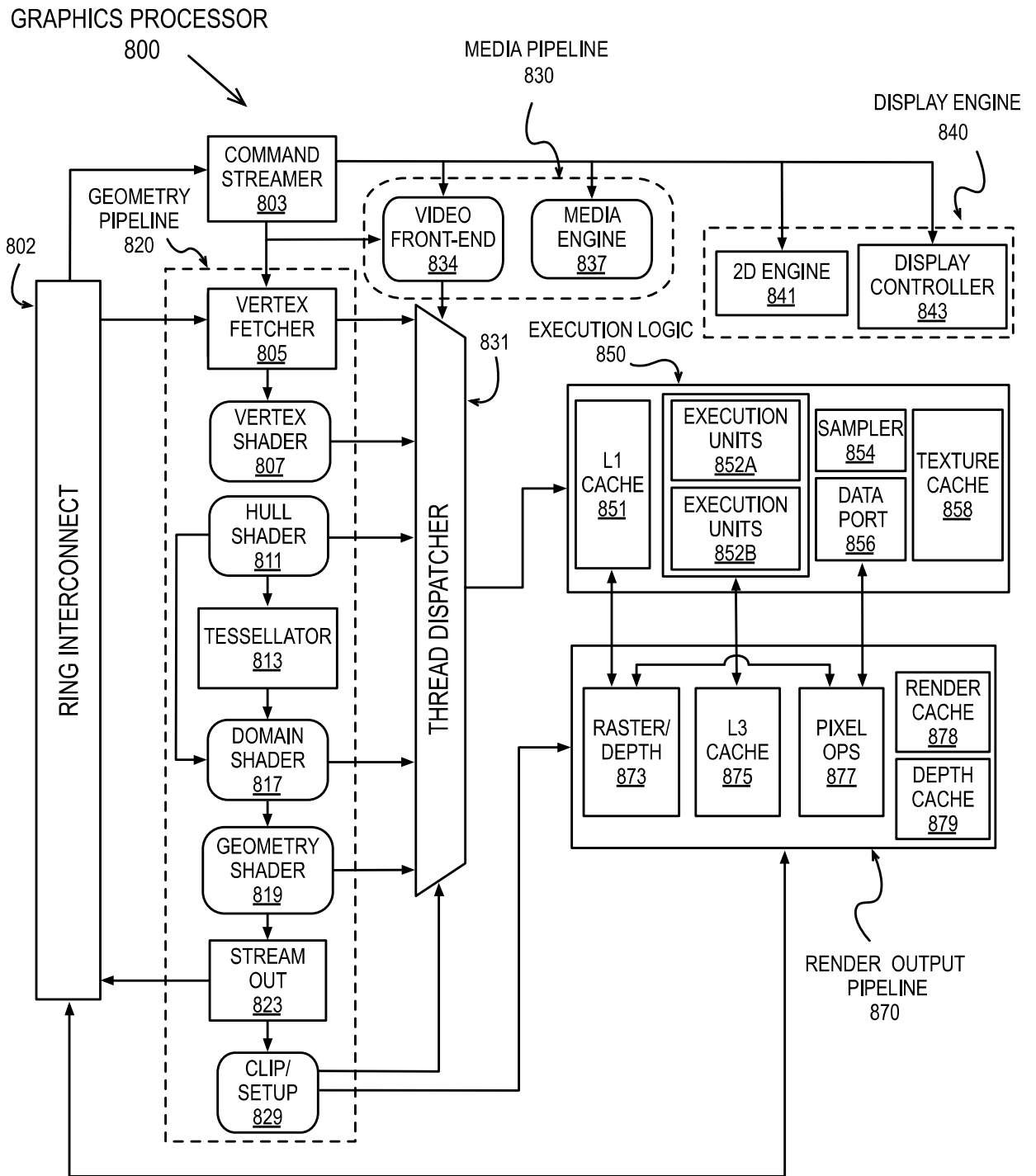


FIG. 8

FIG. 9A **GRAPHICS PROCESSOR COMMAND FORMAT**
900

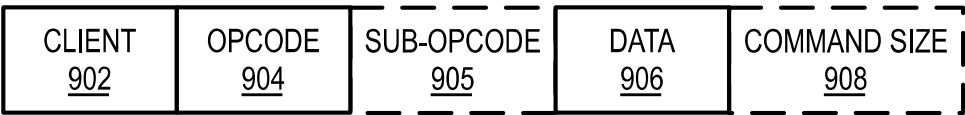
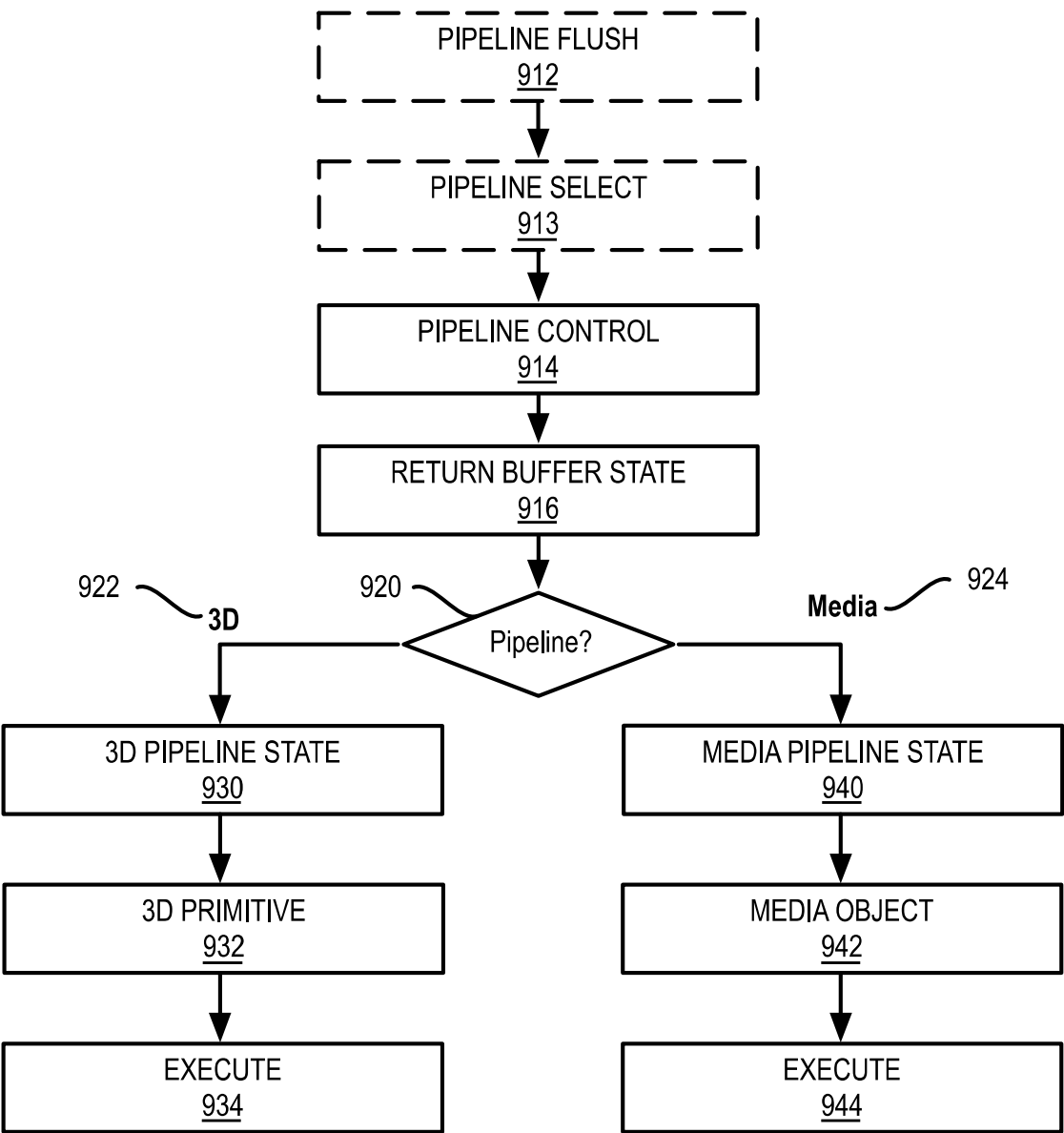


FIG. 9B **GRAPHICS PROCESSOR COMMAND SEQUENCE**
910



DATA PROCESSING SYSTEM -1000

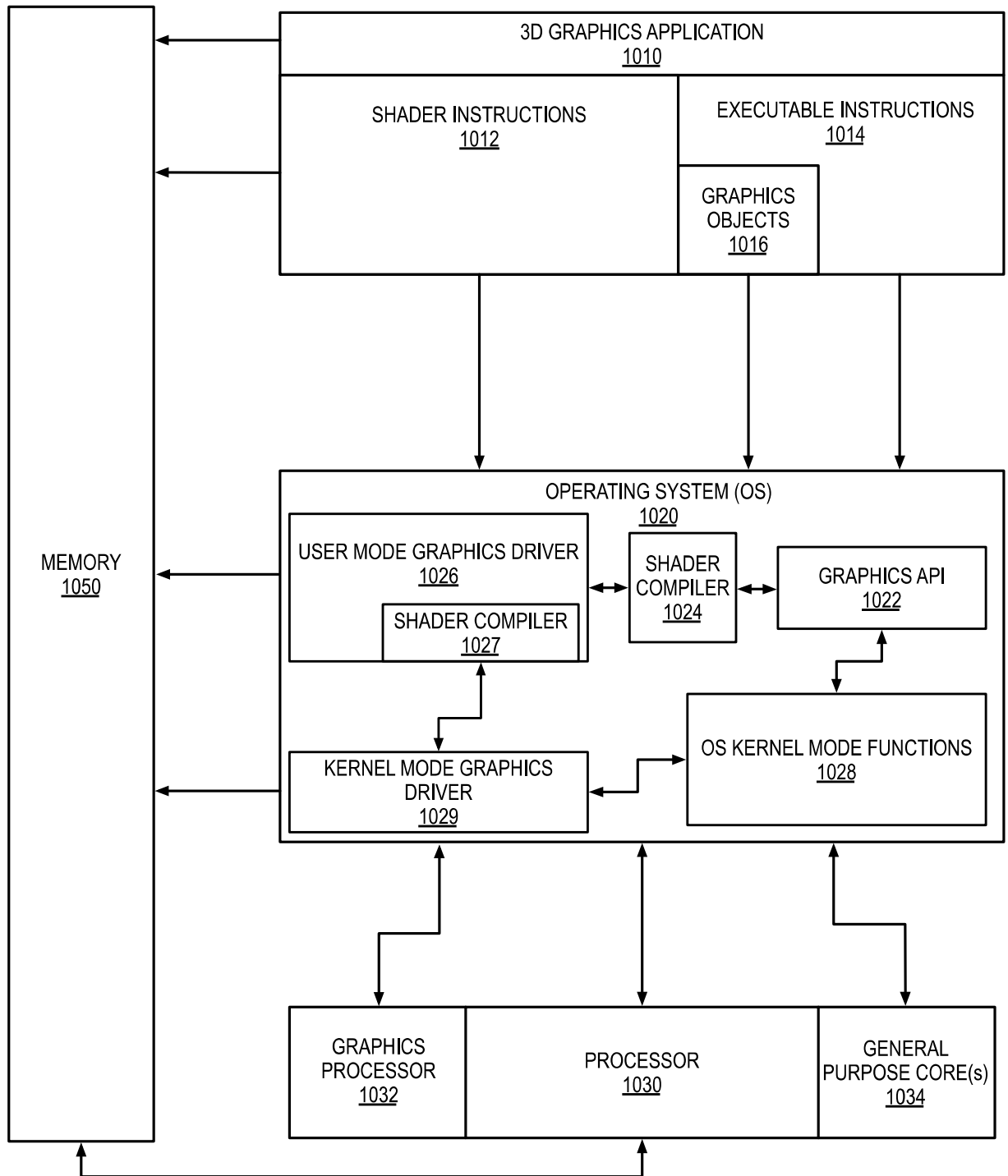


FIG. 10

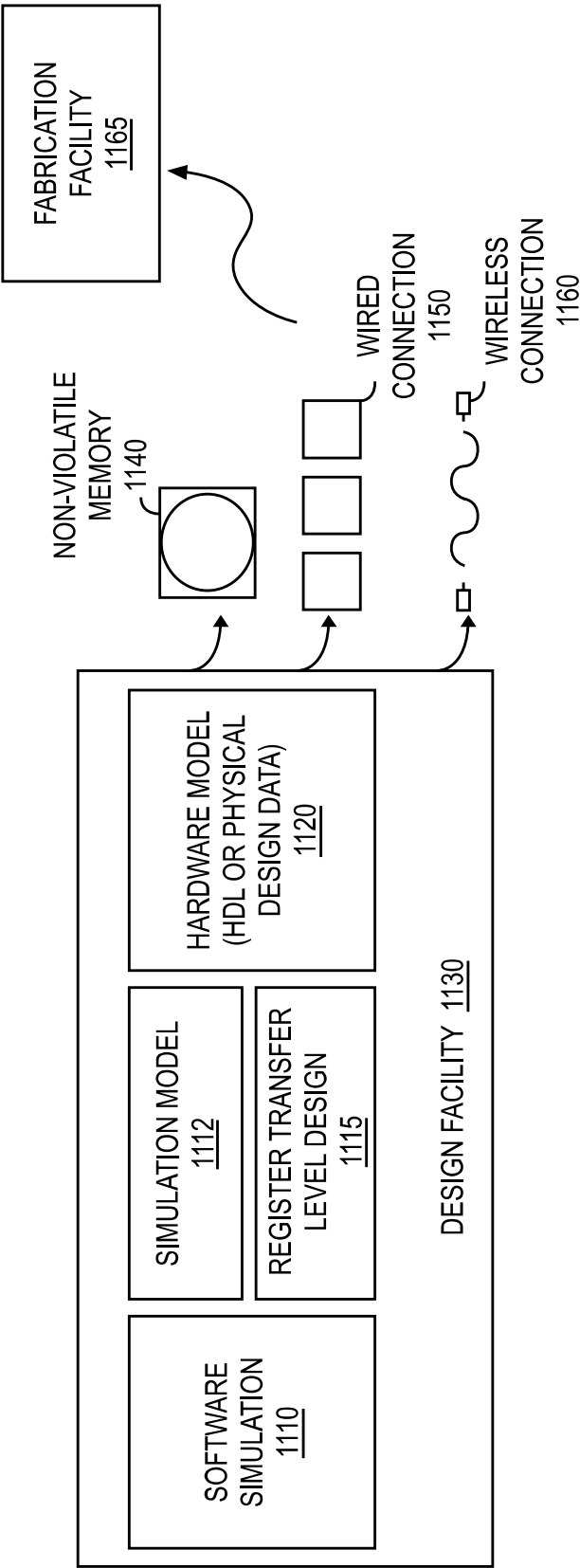


FIG. 11A

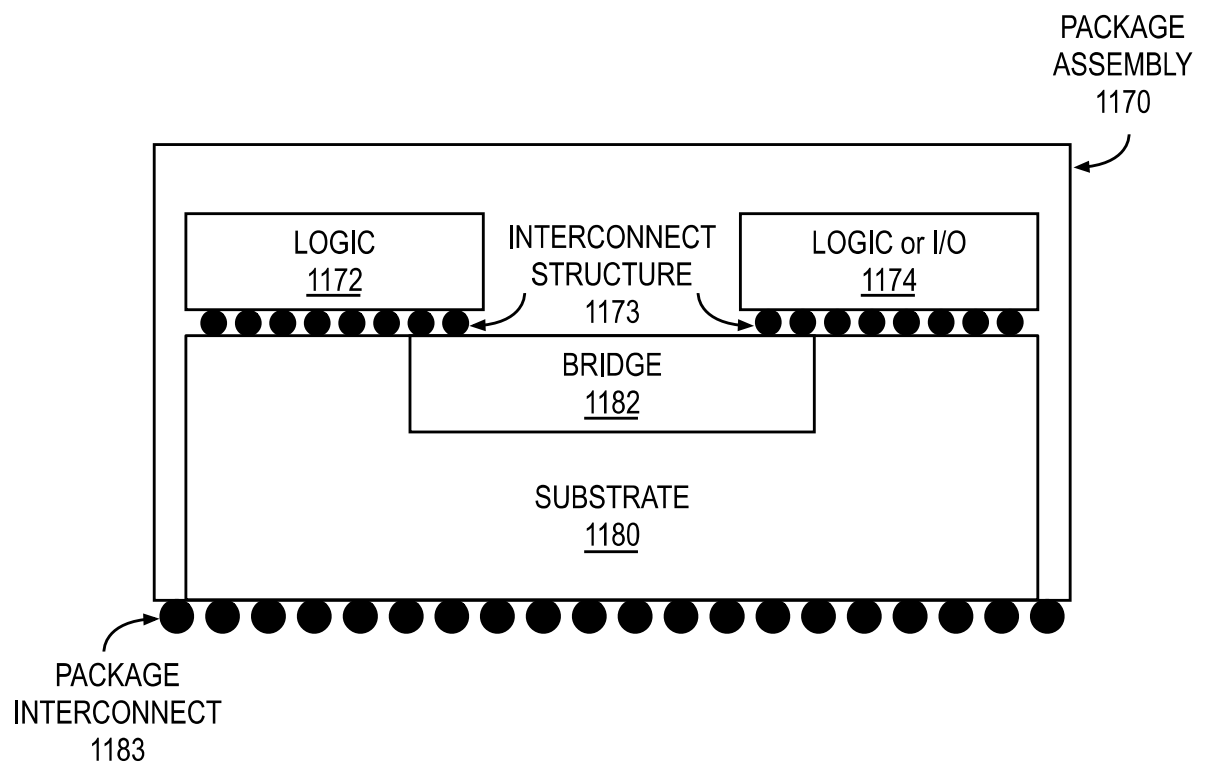


FIG. 11B

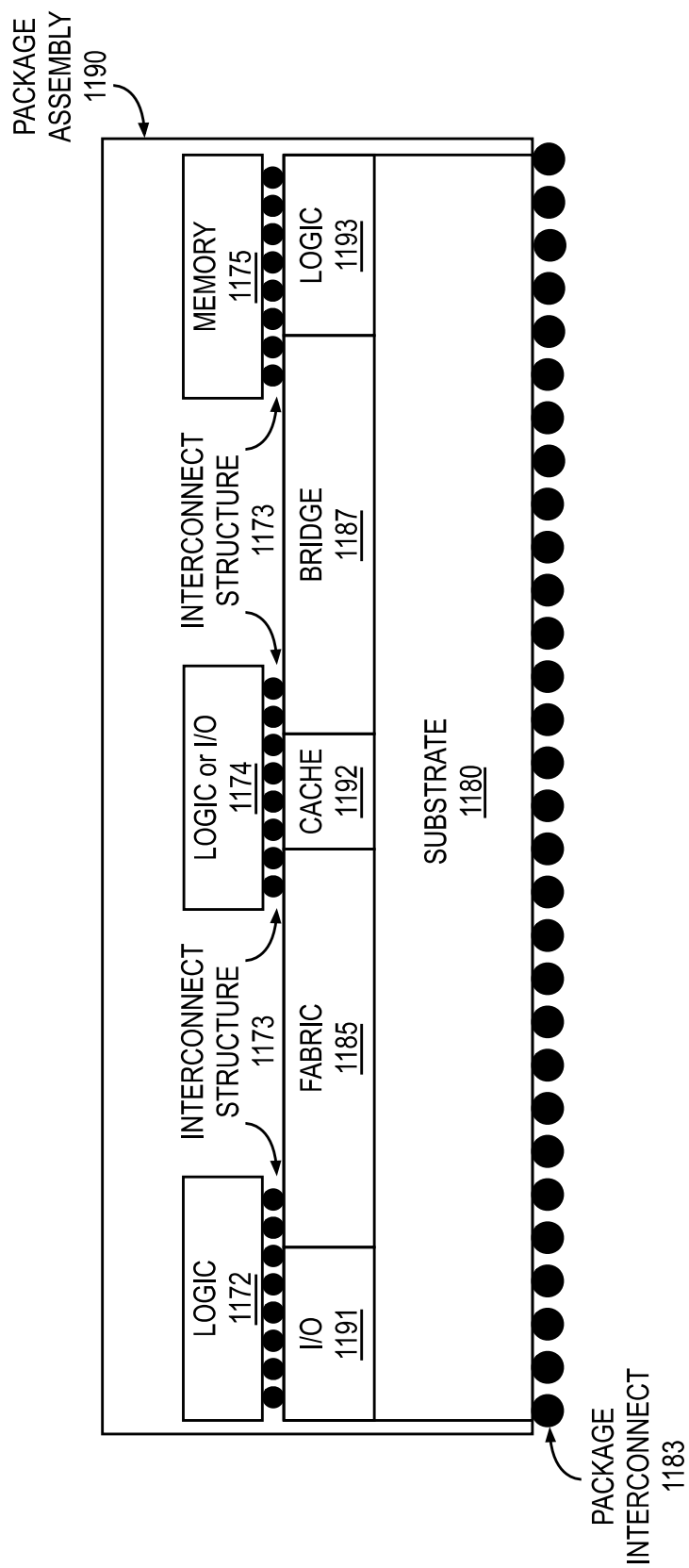


FIG. 11C

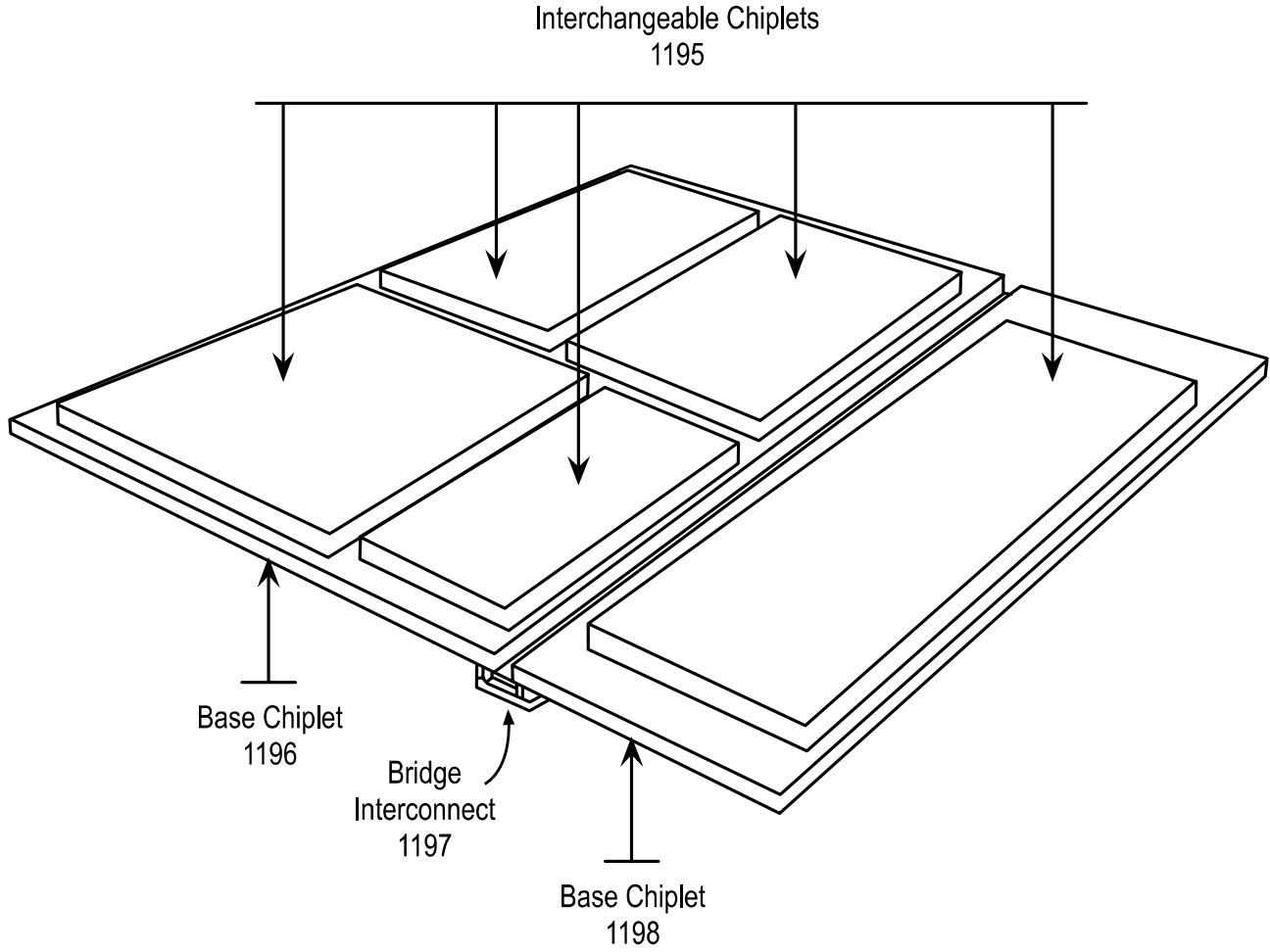


FIG. 11D

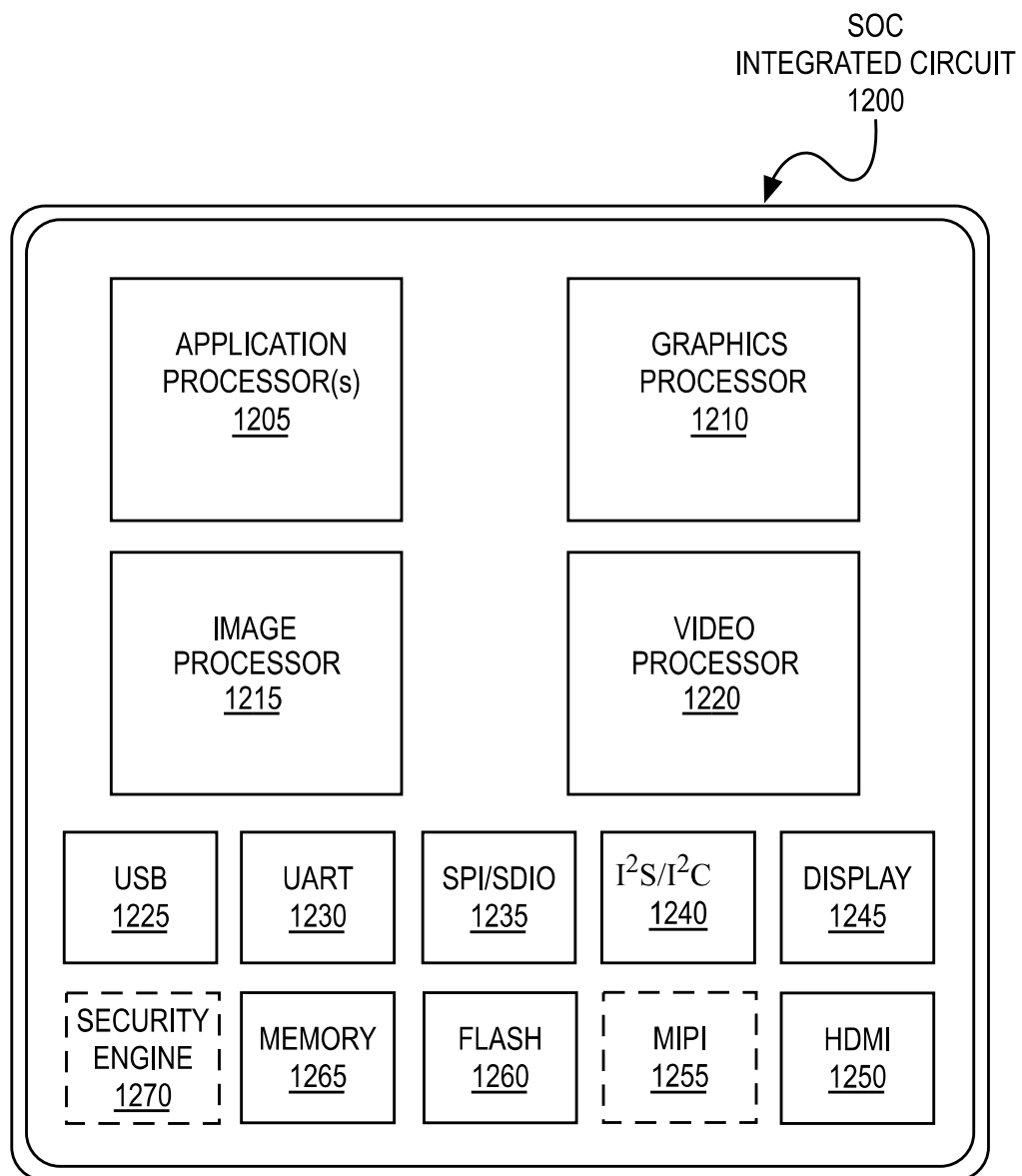


FIG. 12

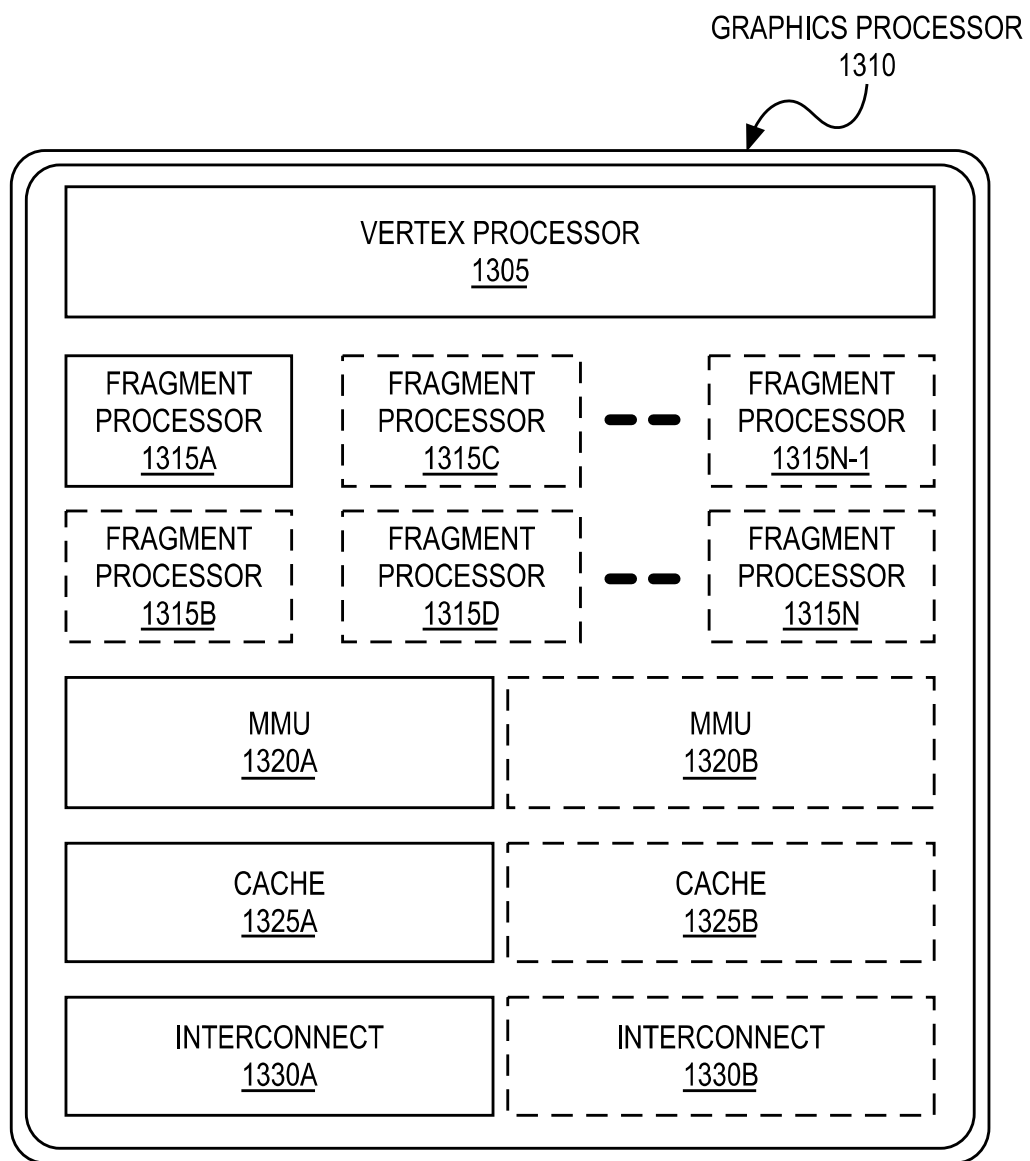


FIG. 13

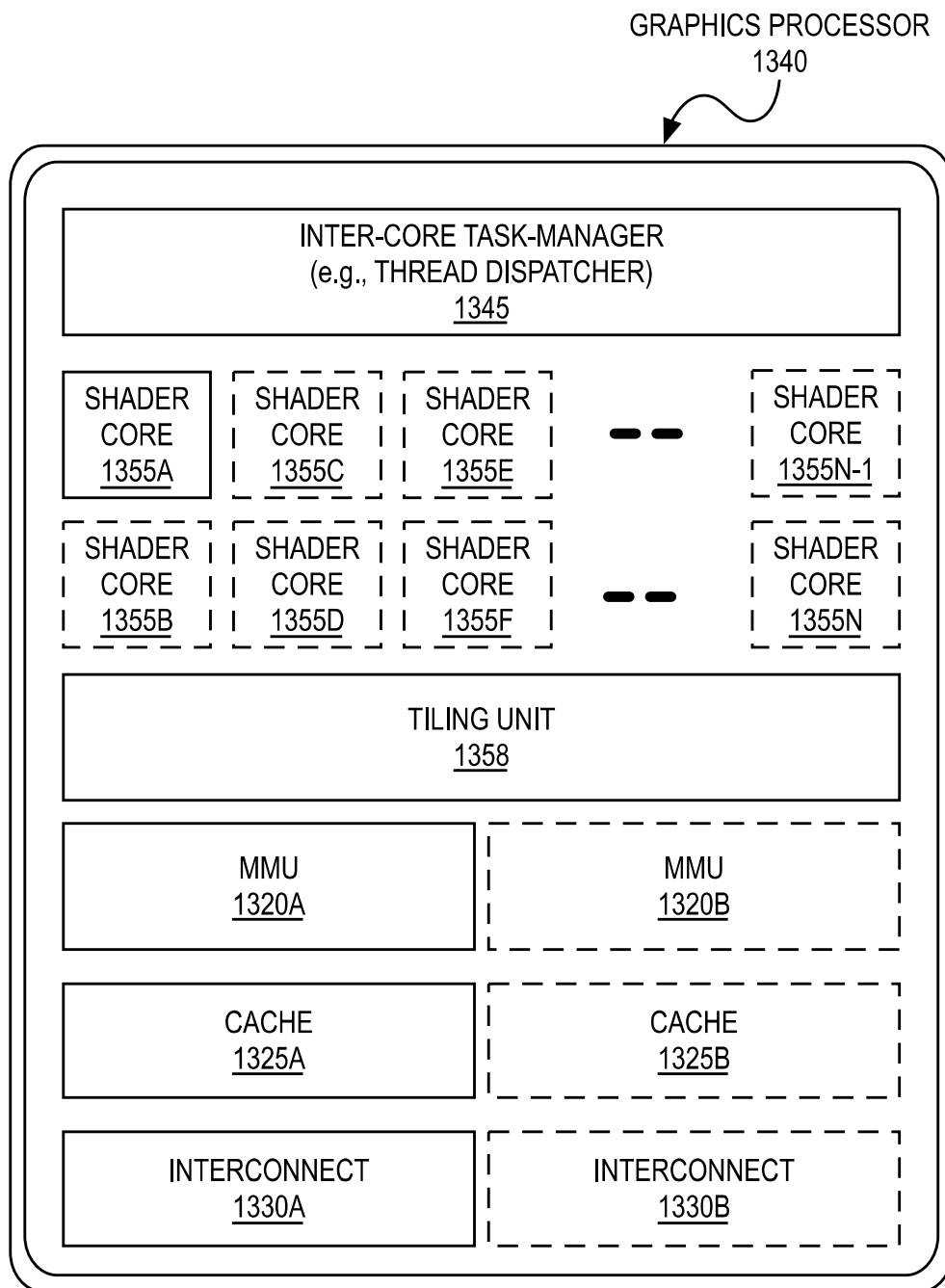


FIG. 14

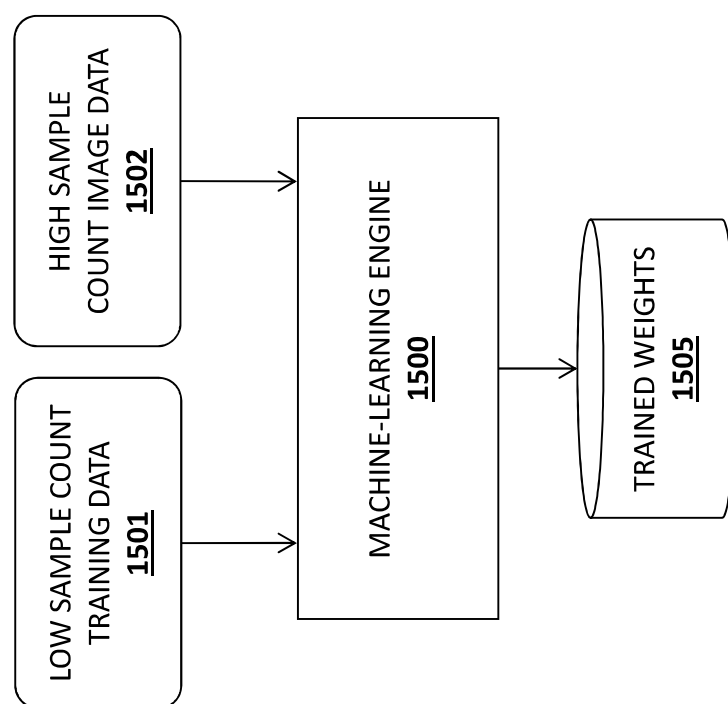


FIG. 15

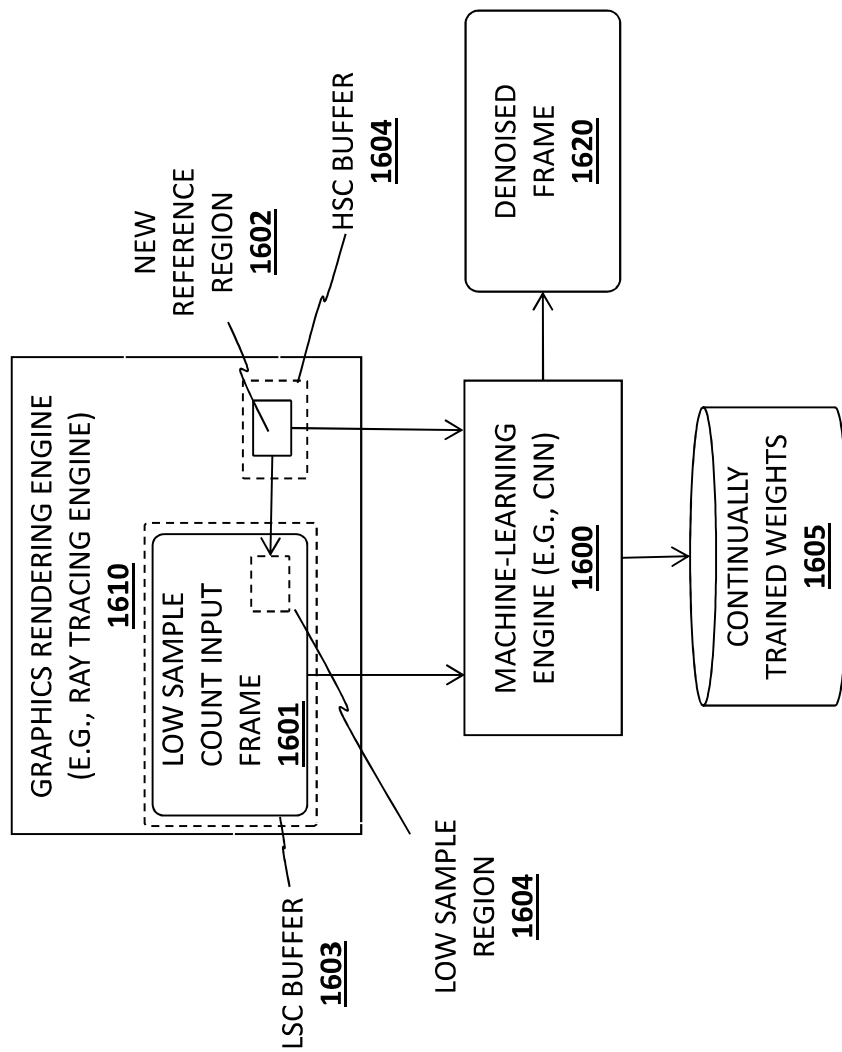


FIG. 16

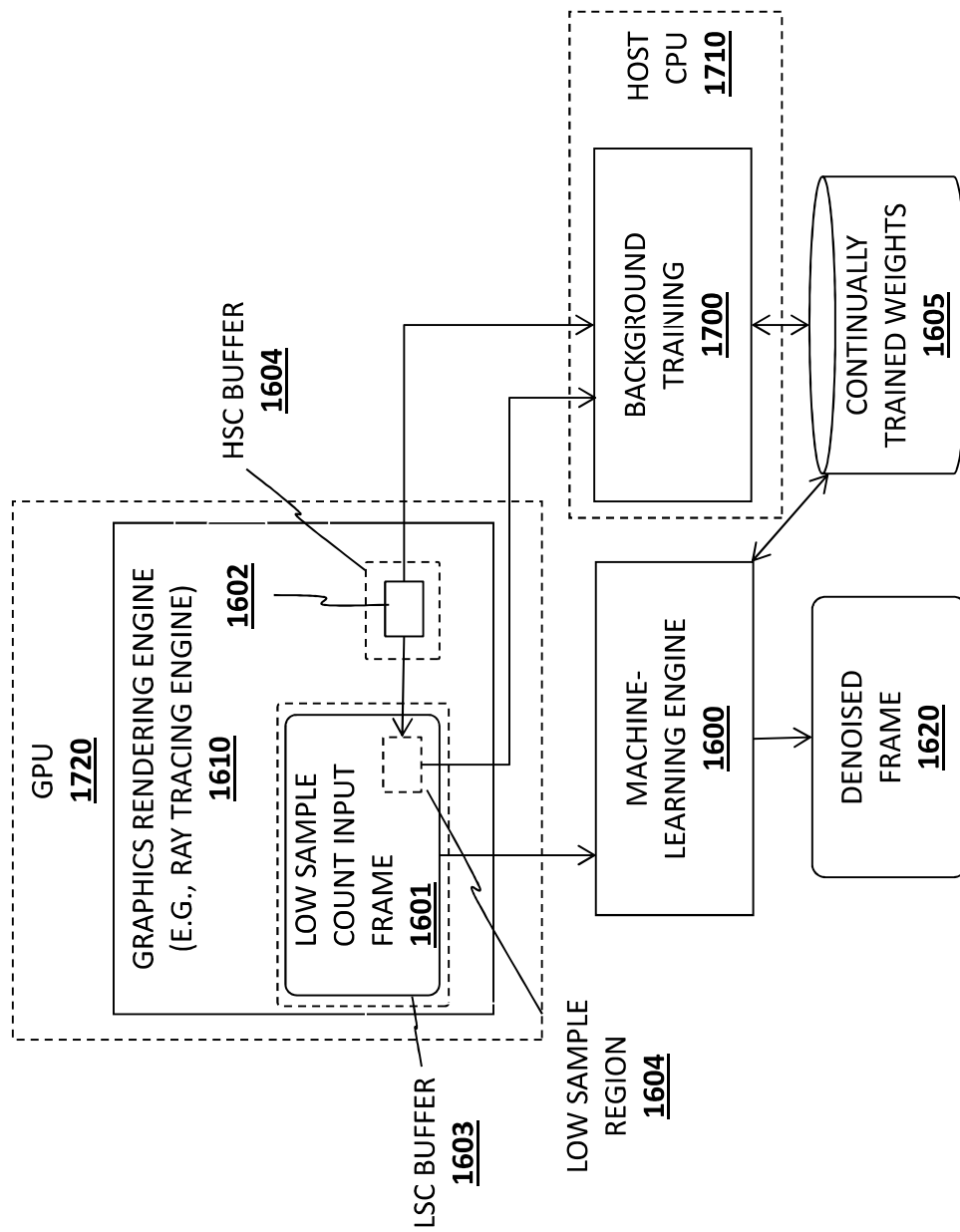


FIG. 17

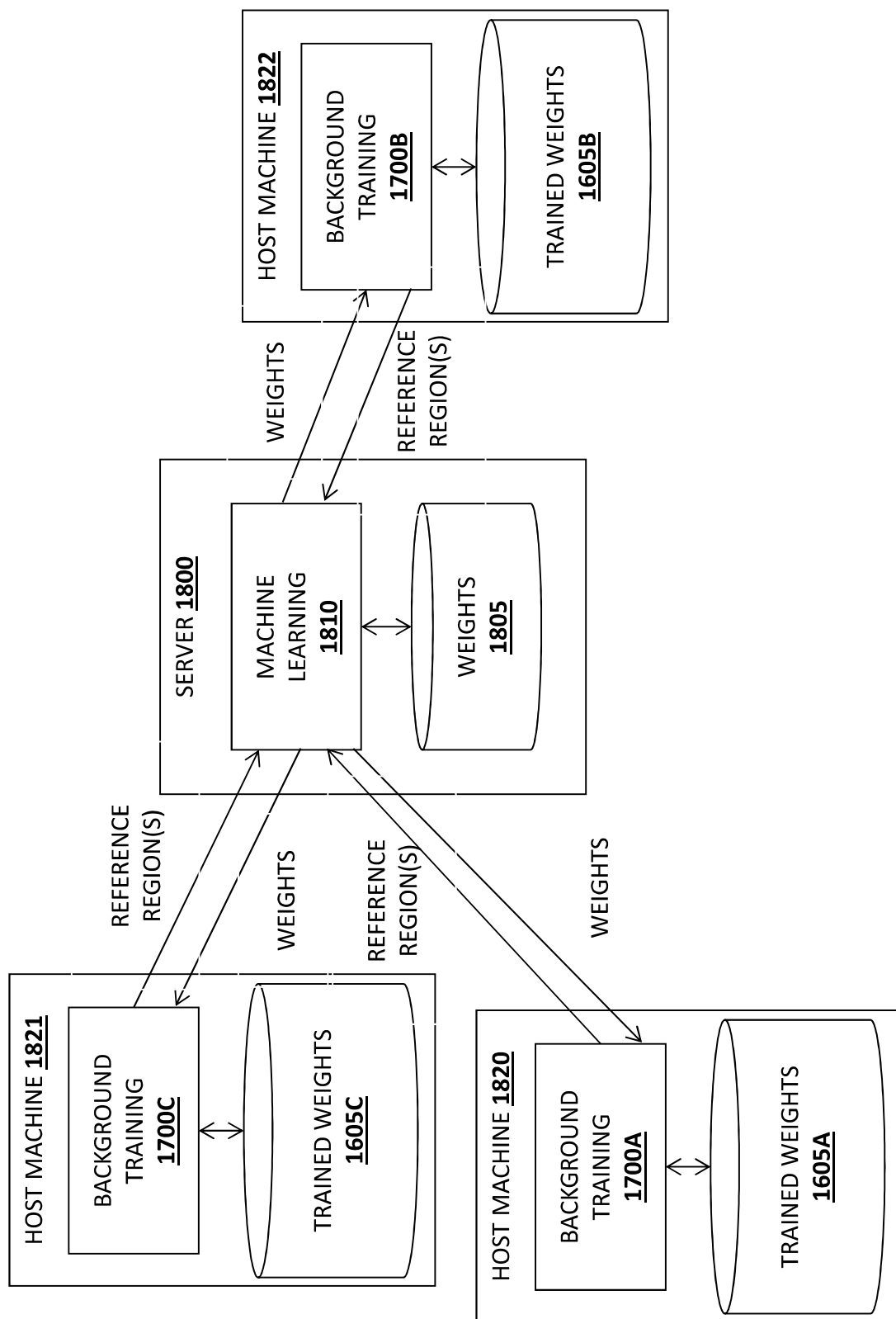


FIG. 18A

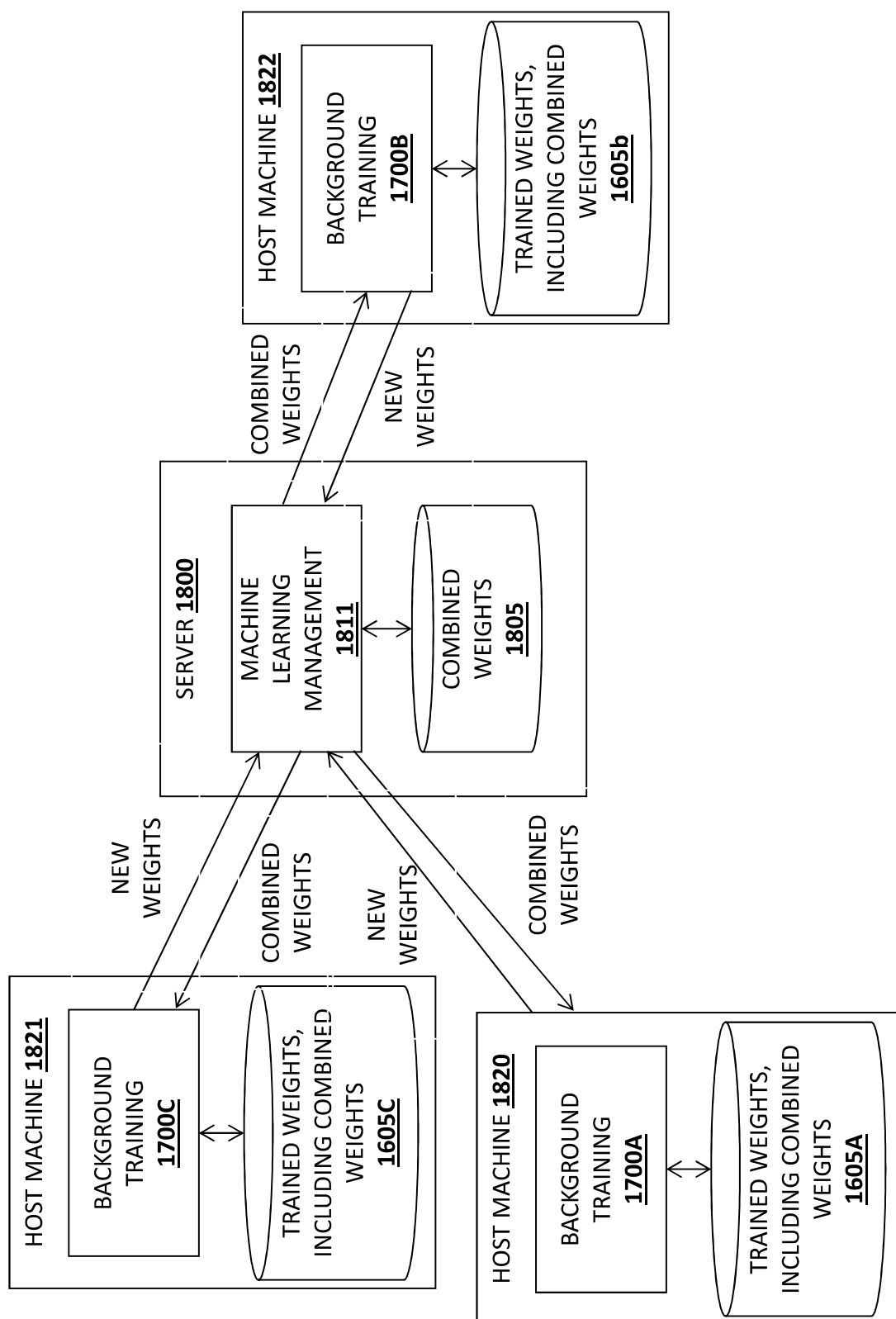


FIG. 18B

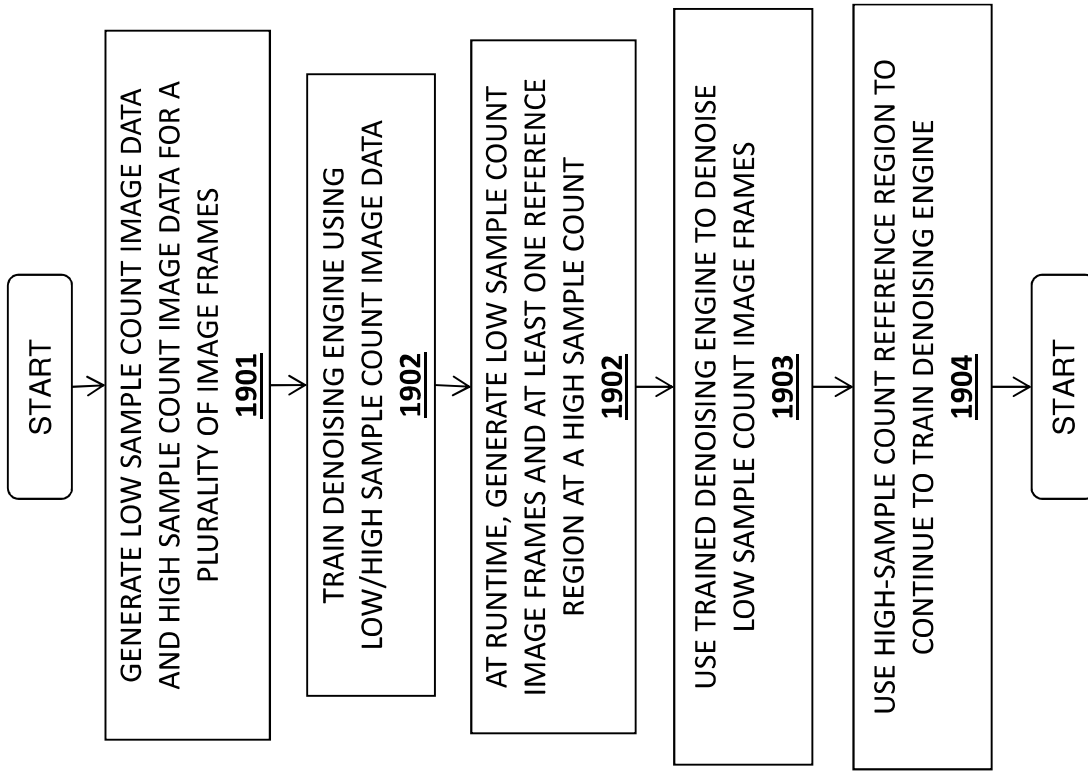


FIG. 19

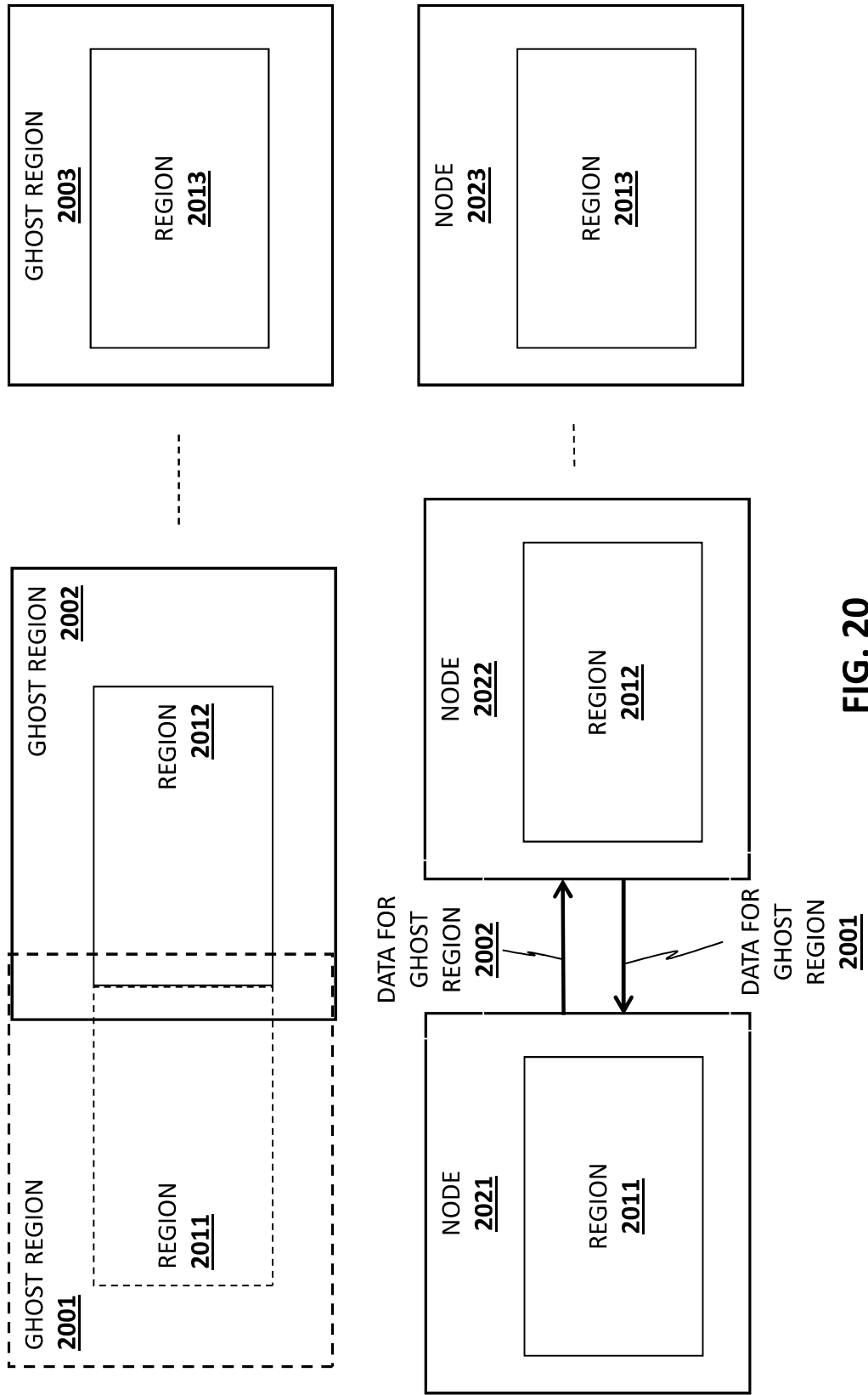


FIG. 20

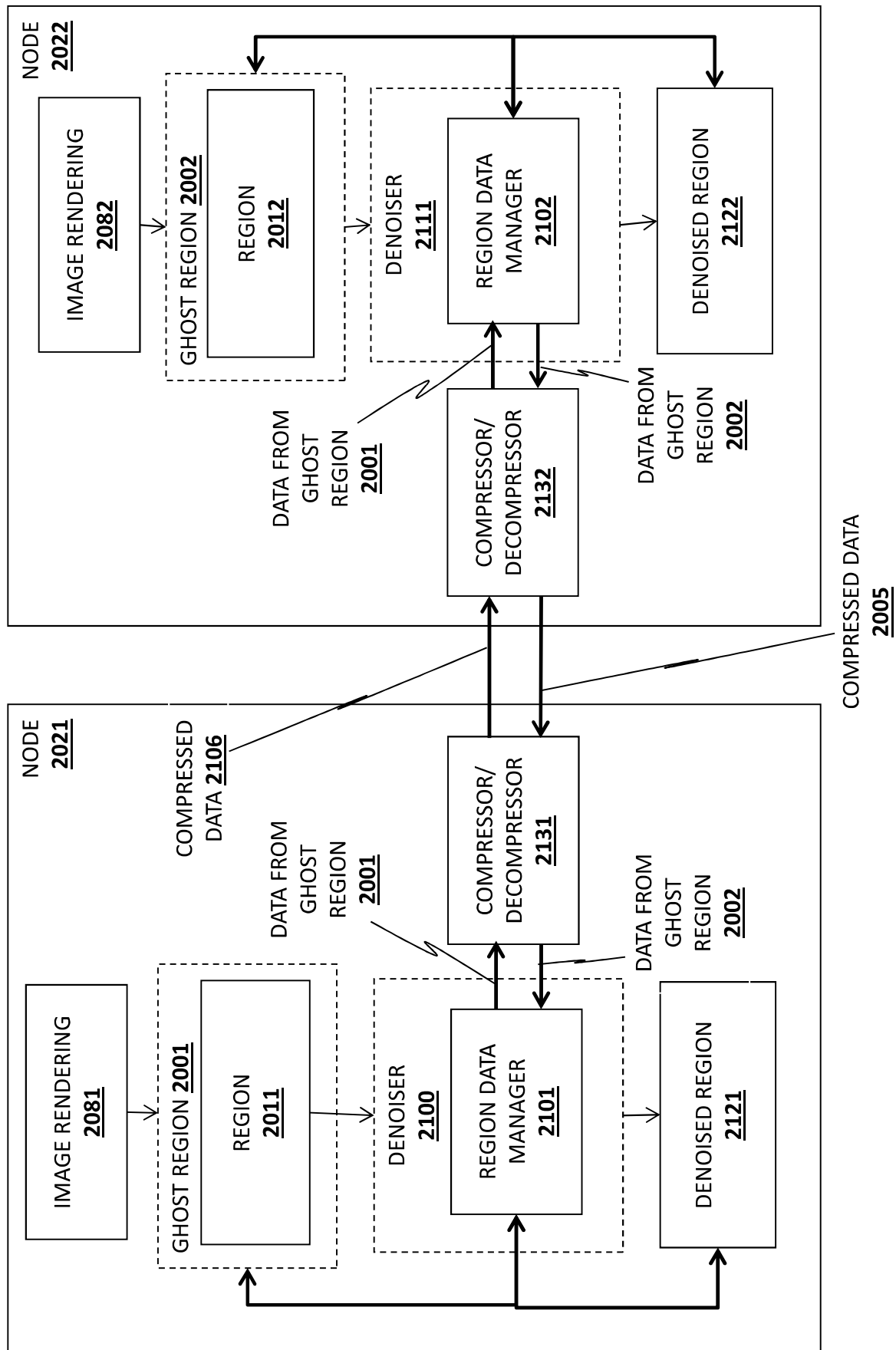


FIG. 21

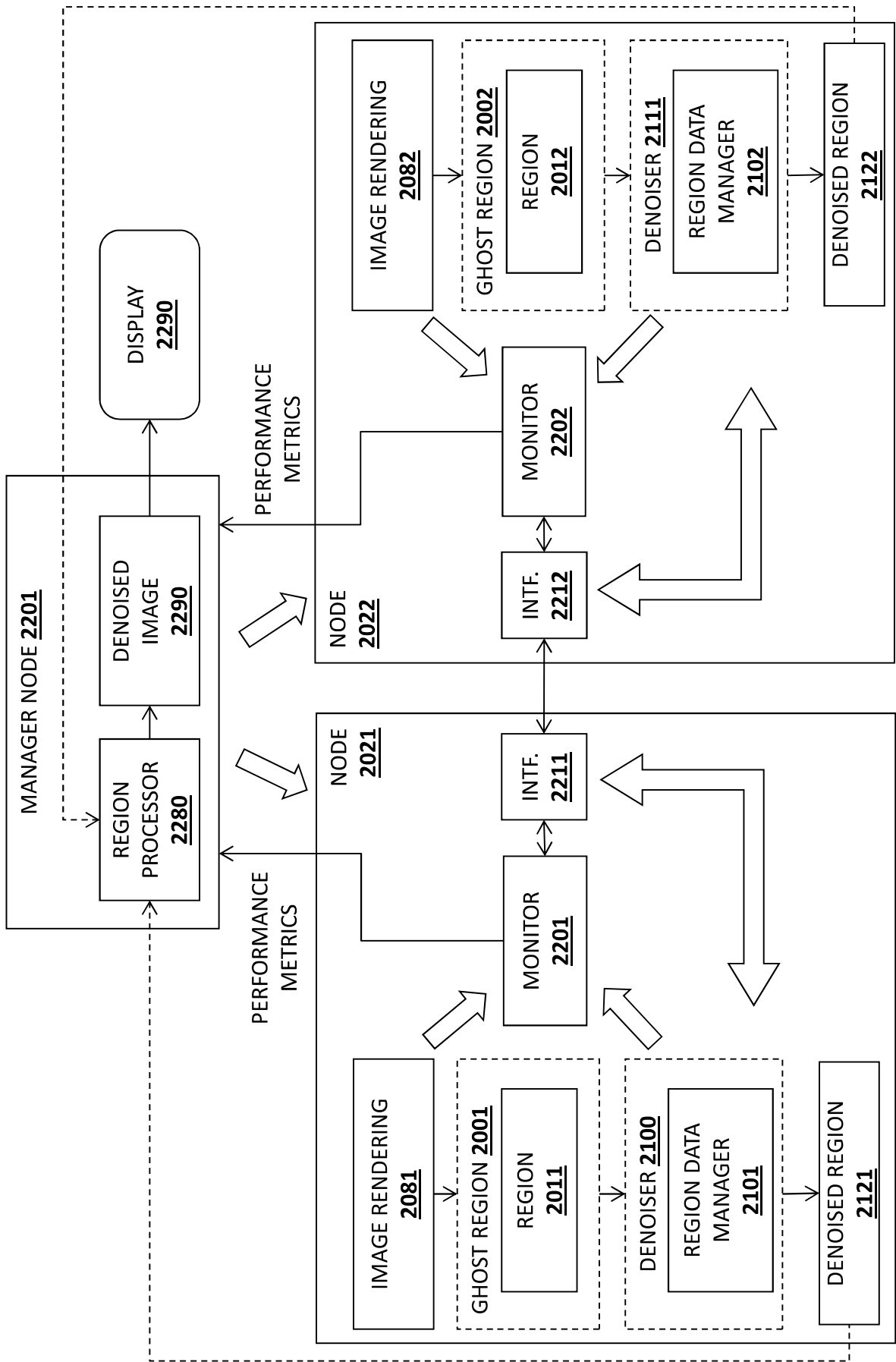


FIG. 22

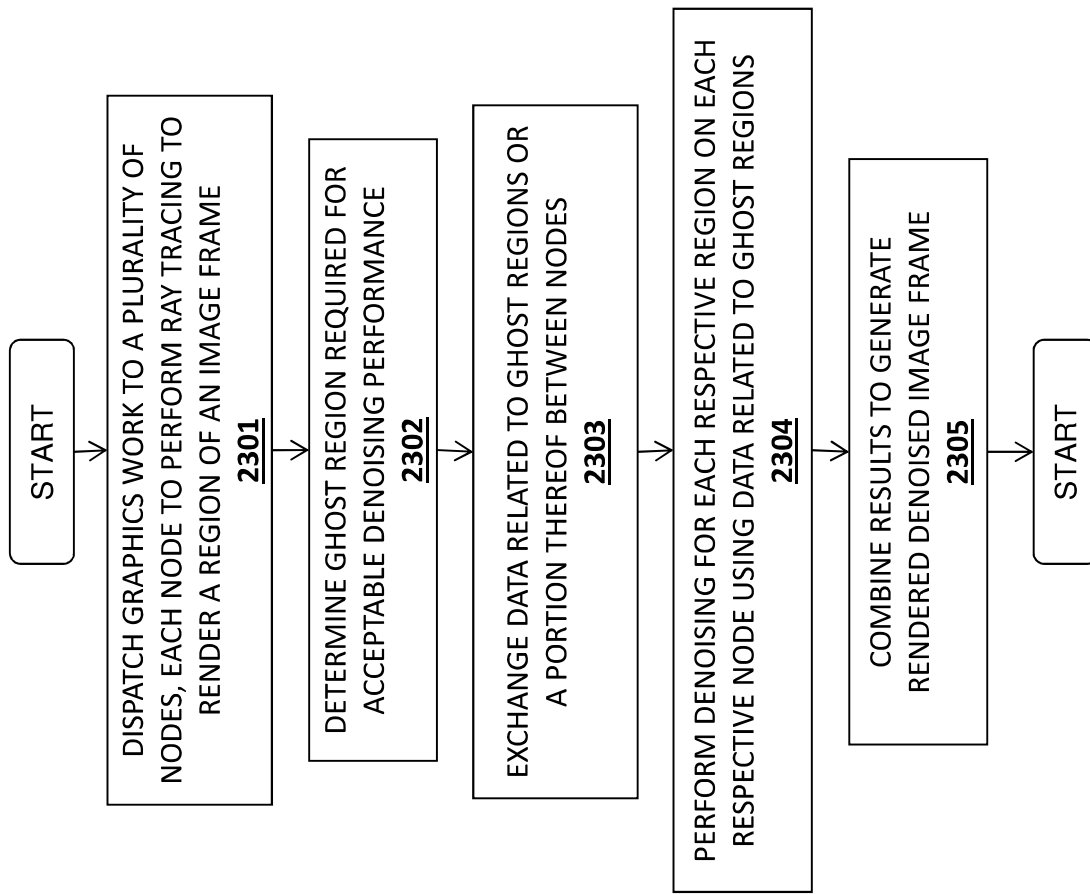


FIG. 23

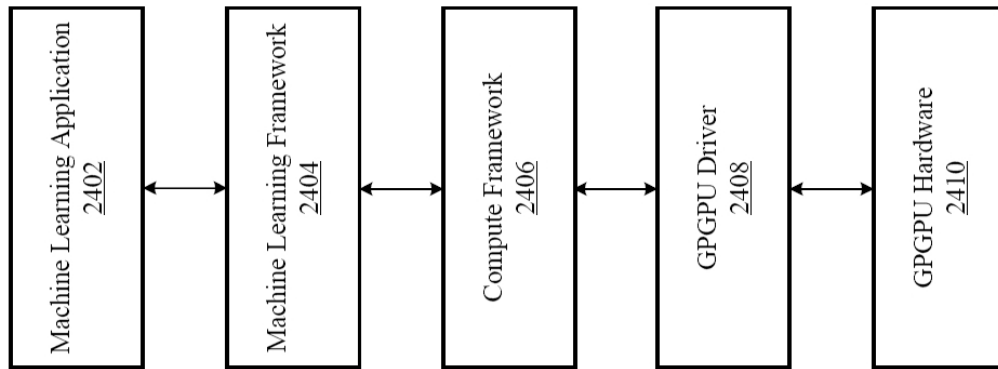


FIG. 24

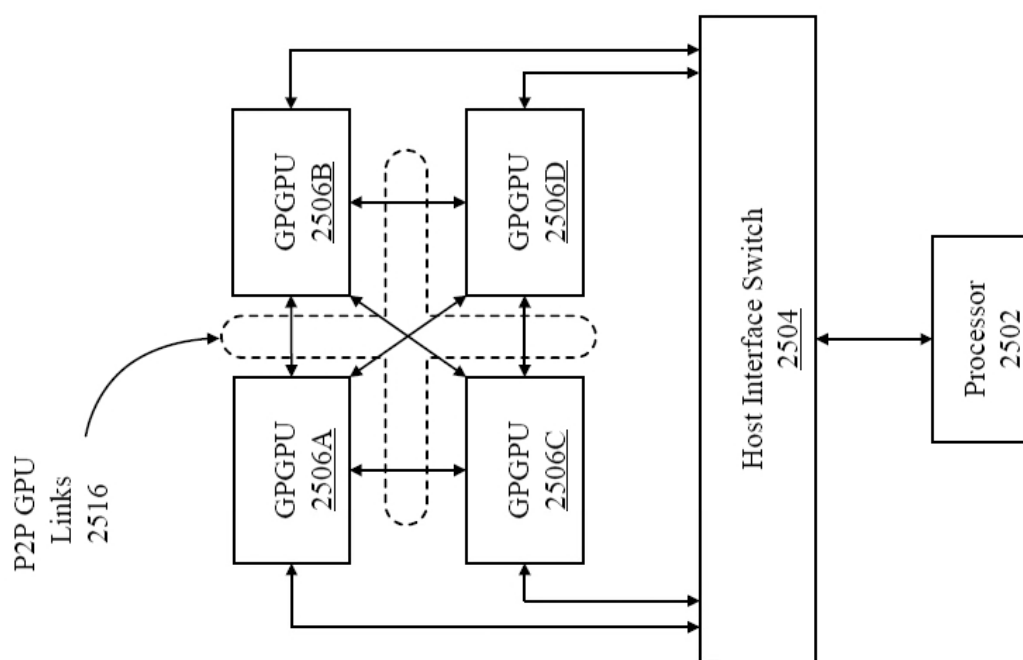


FIG. 25

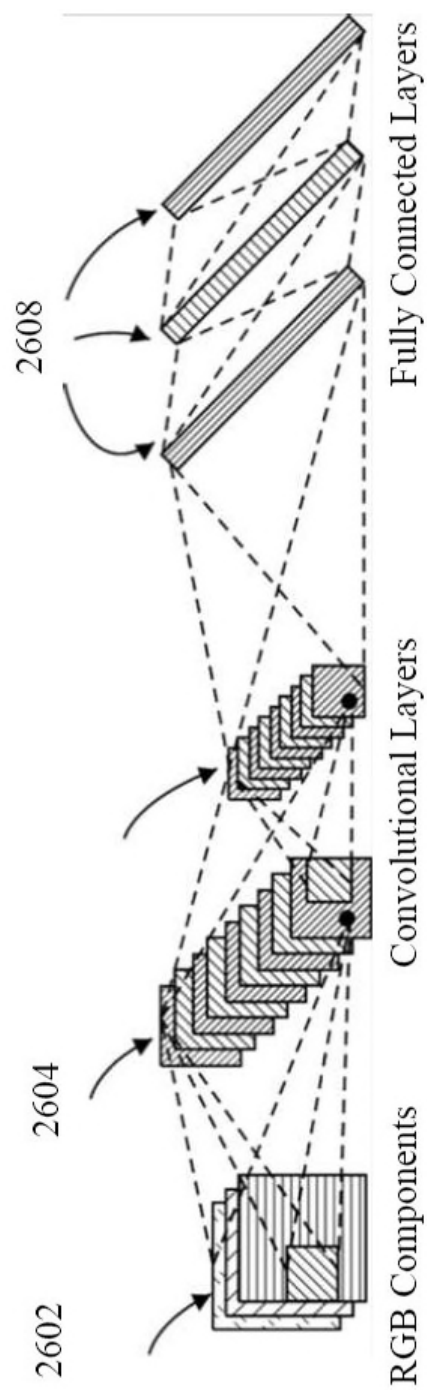


FIG. 26

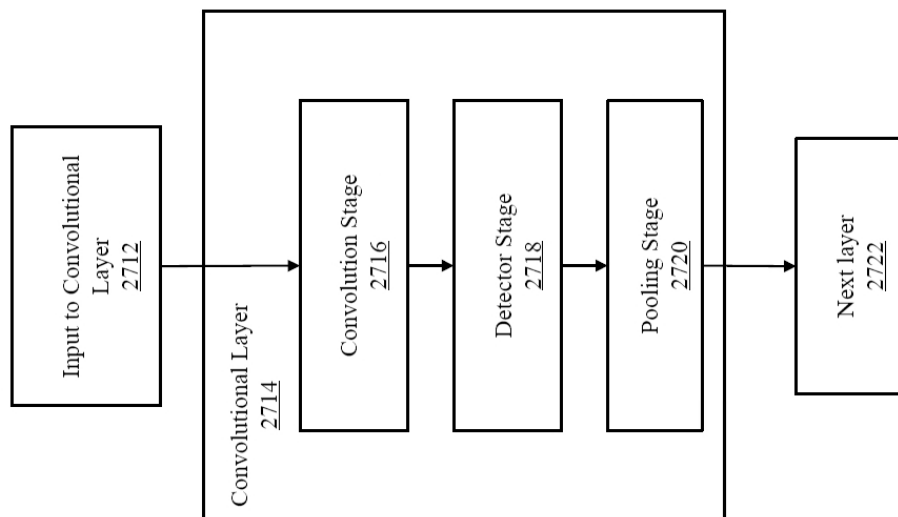


FIG. 27

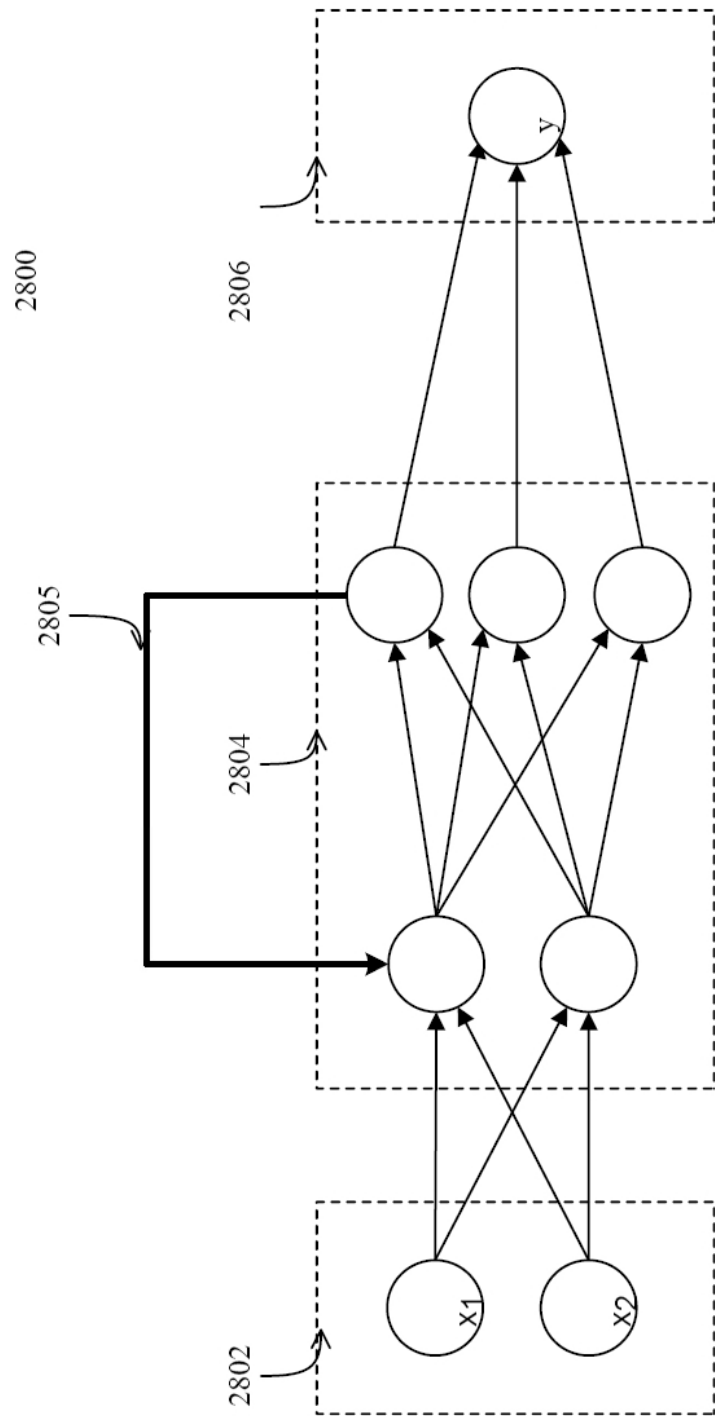


FIG. 28

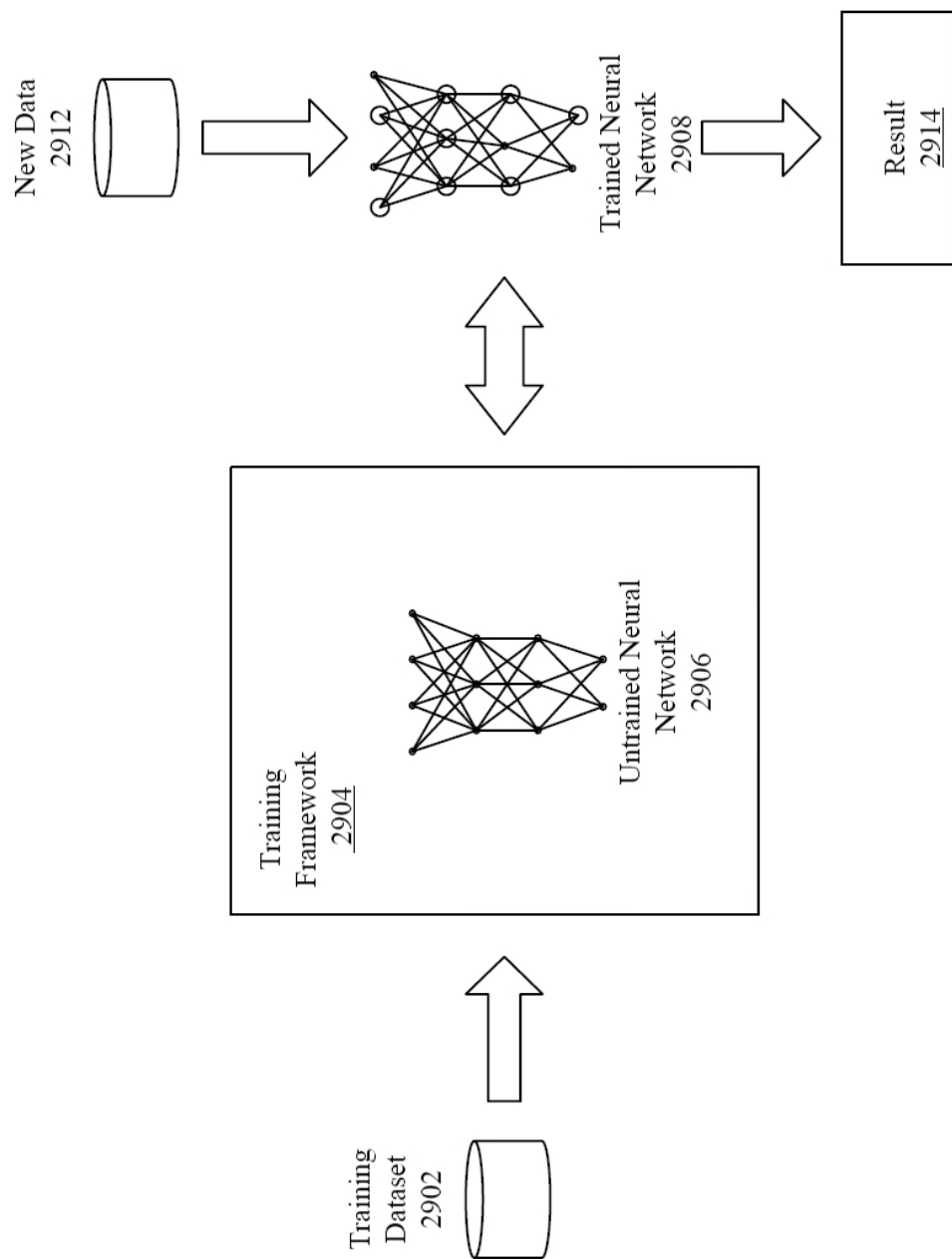


FIG. 29

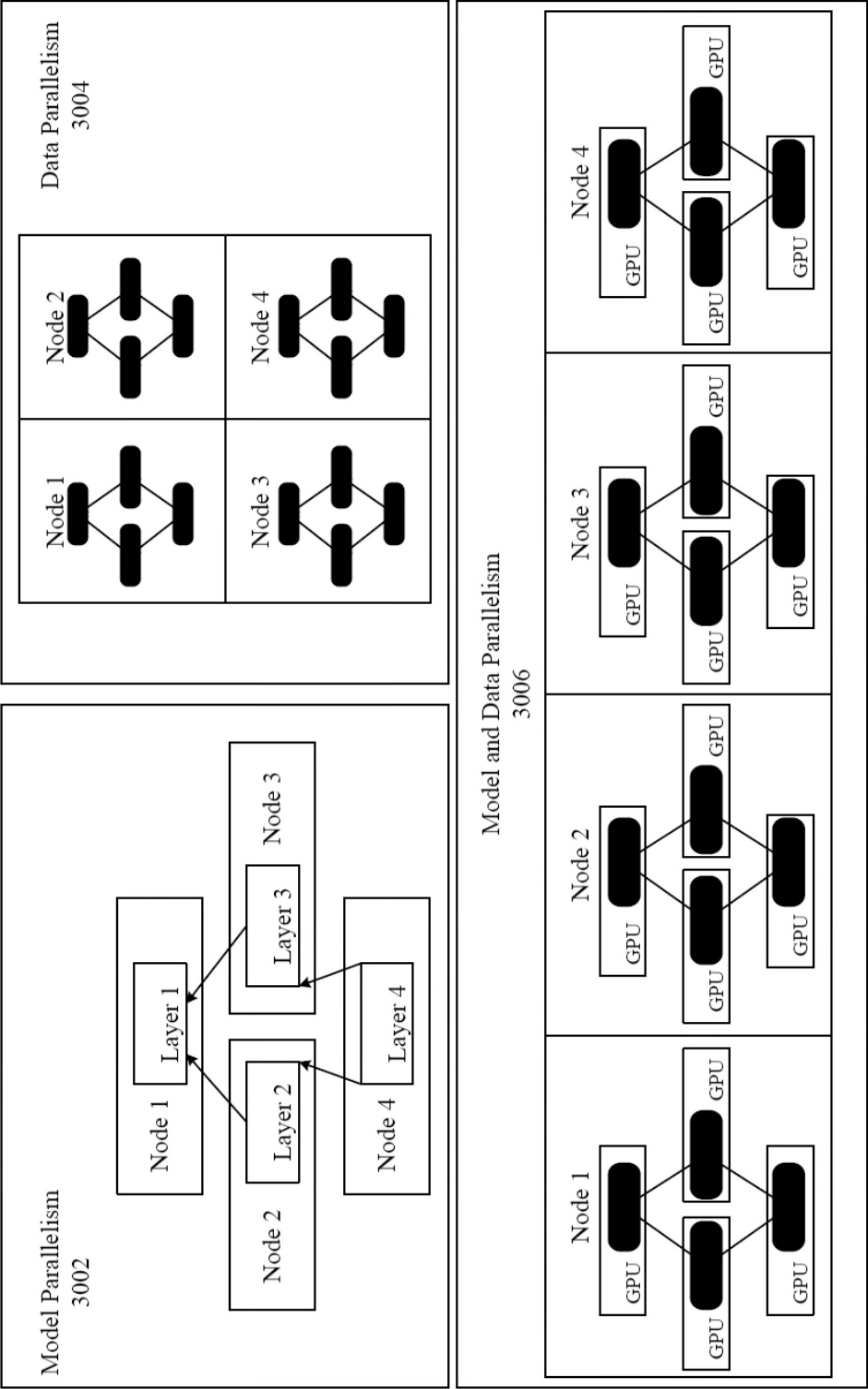


FIG. 30A

3100

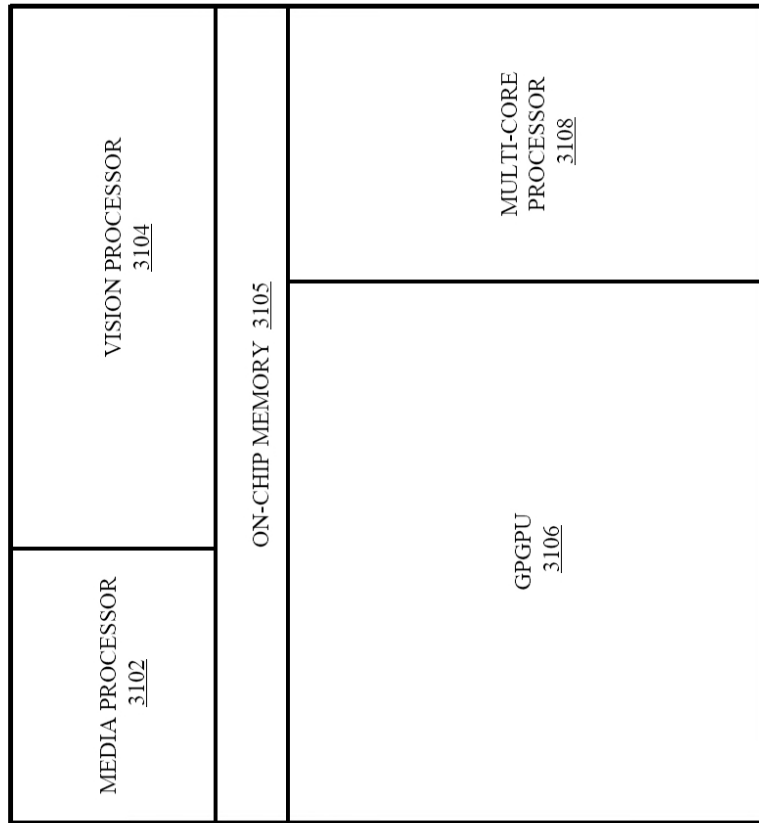


FIG. 30B

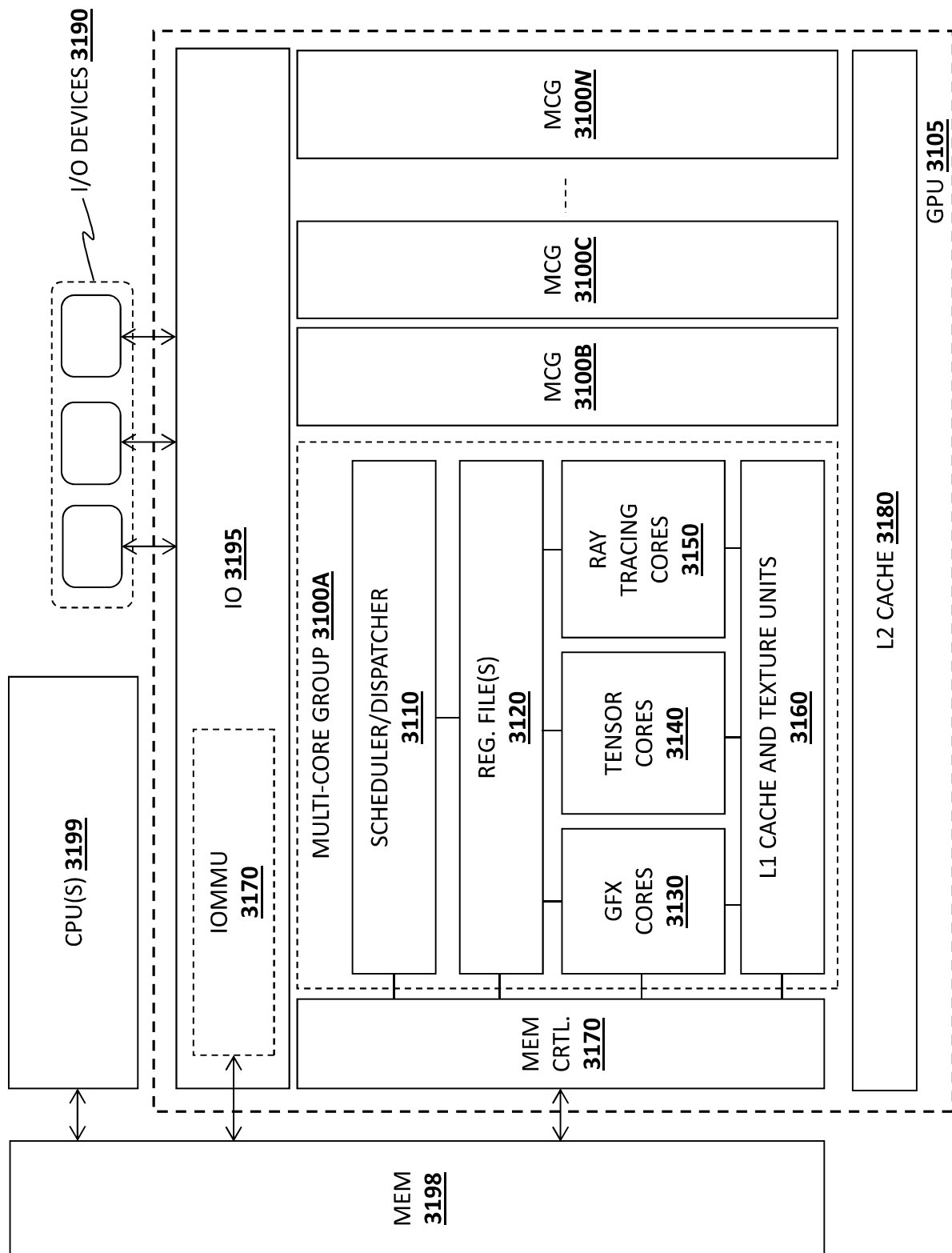


FIG. 31

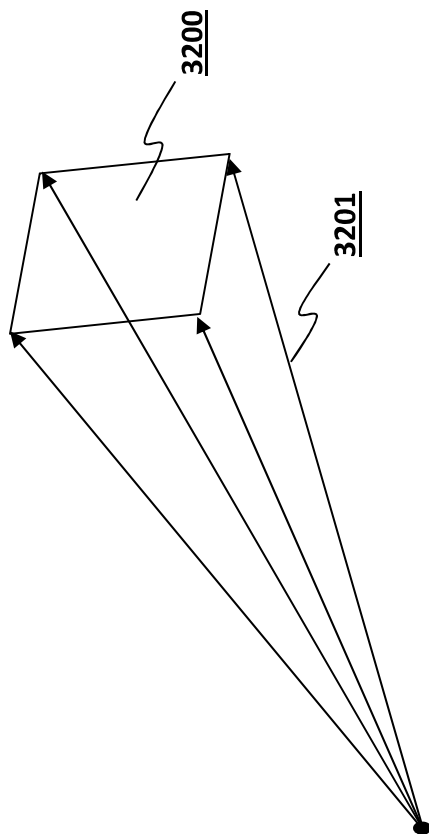


FIG. 32

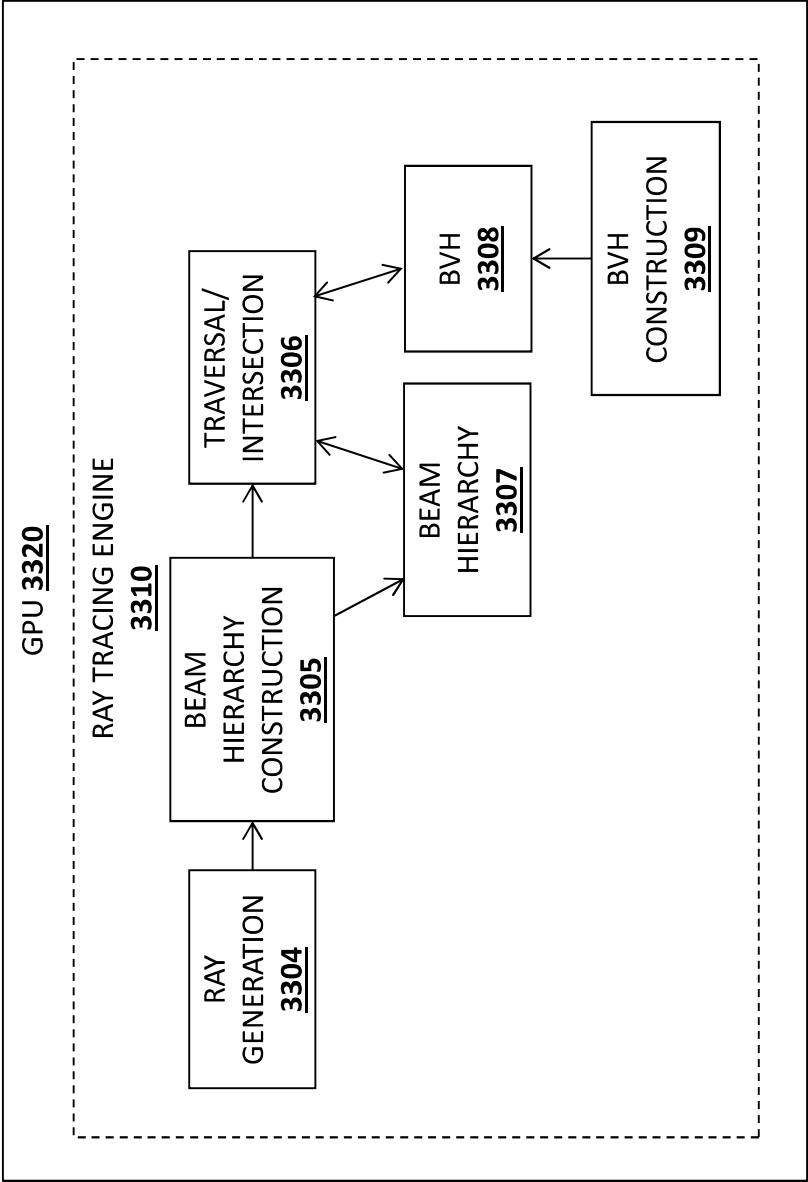


FIG. 33

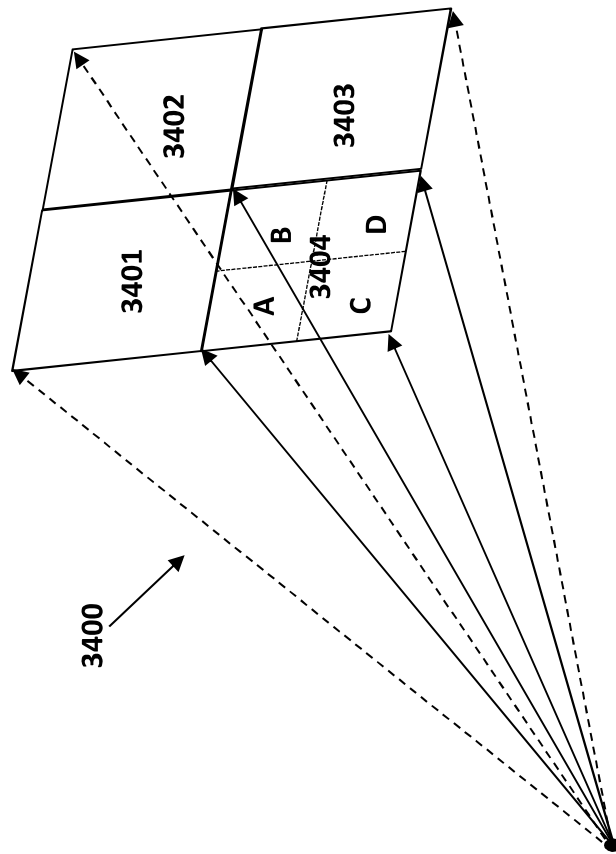


FIG. 34

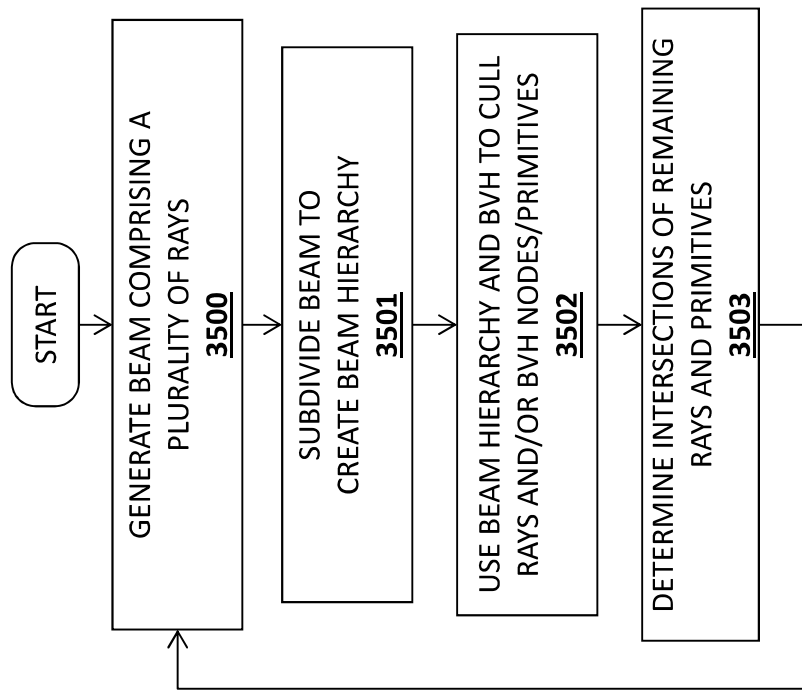


FIG. 35

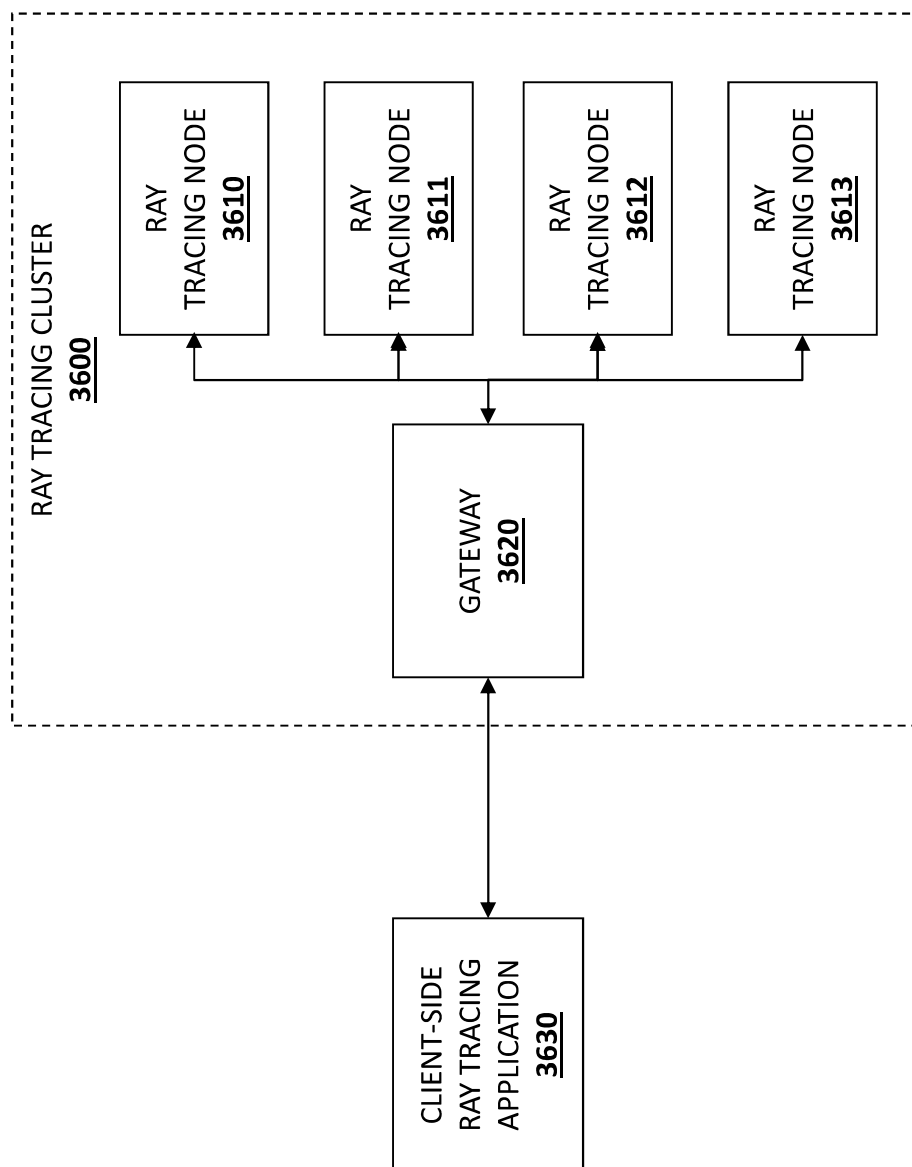


FIG. 36

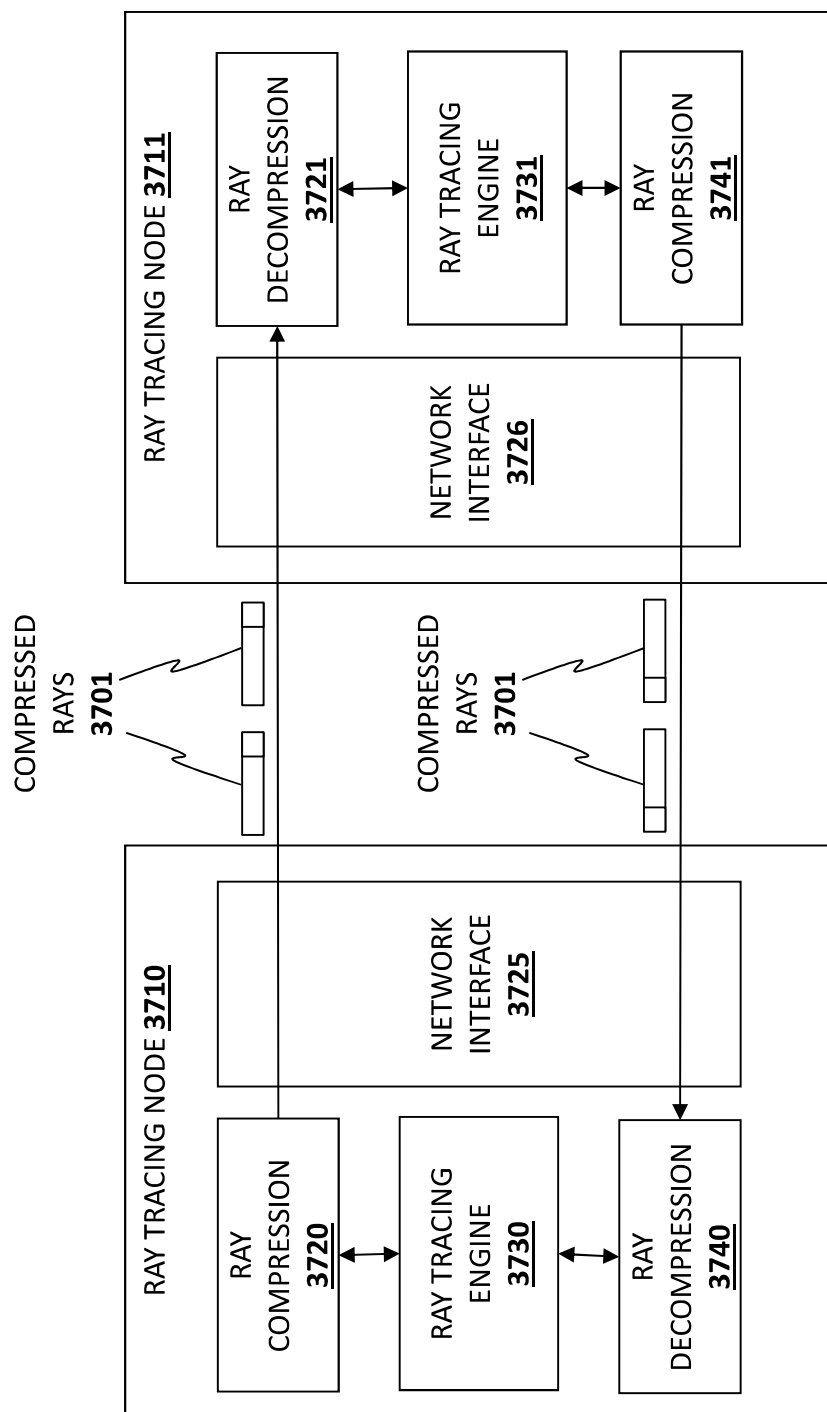


FIG. 37

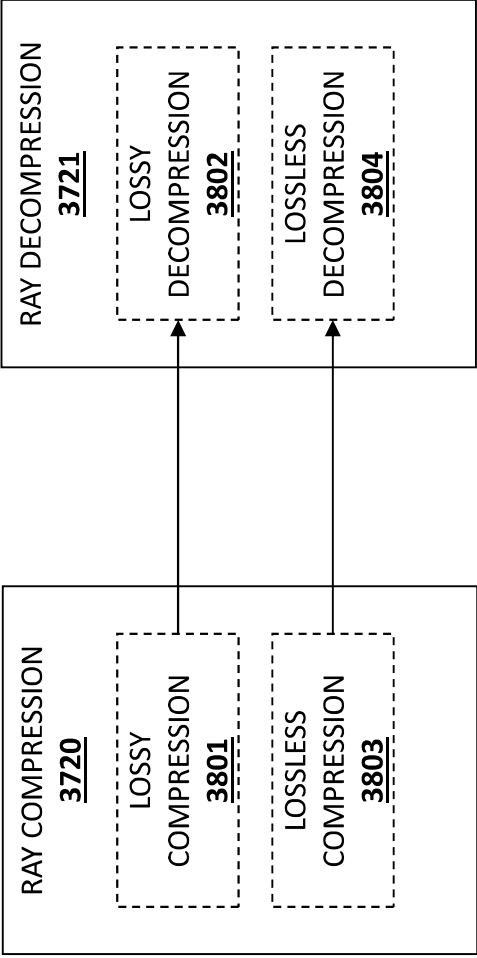


FIG. 38

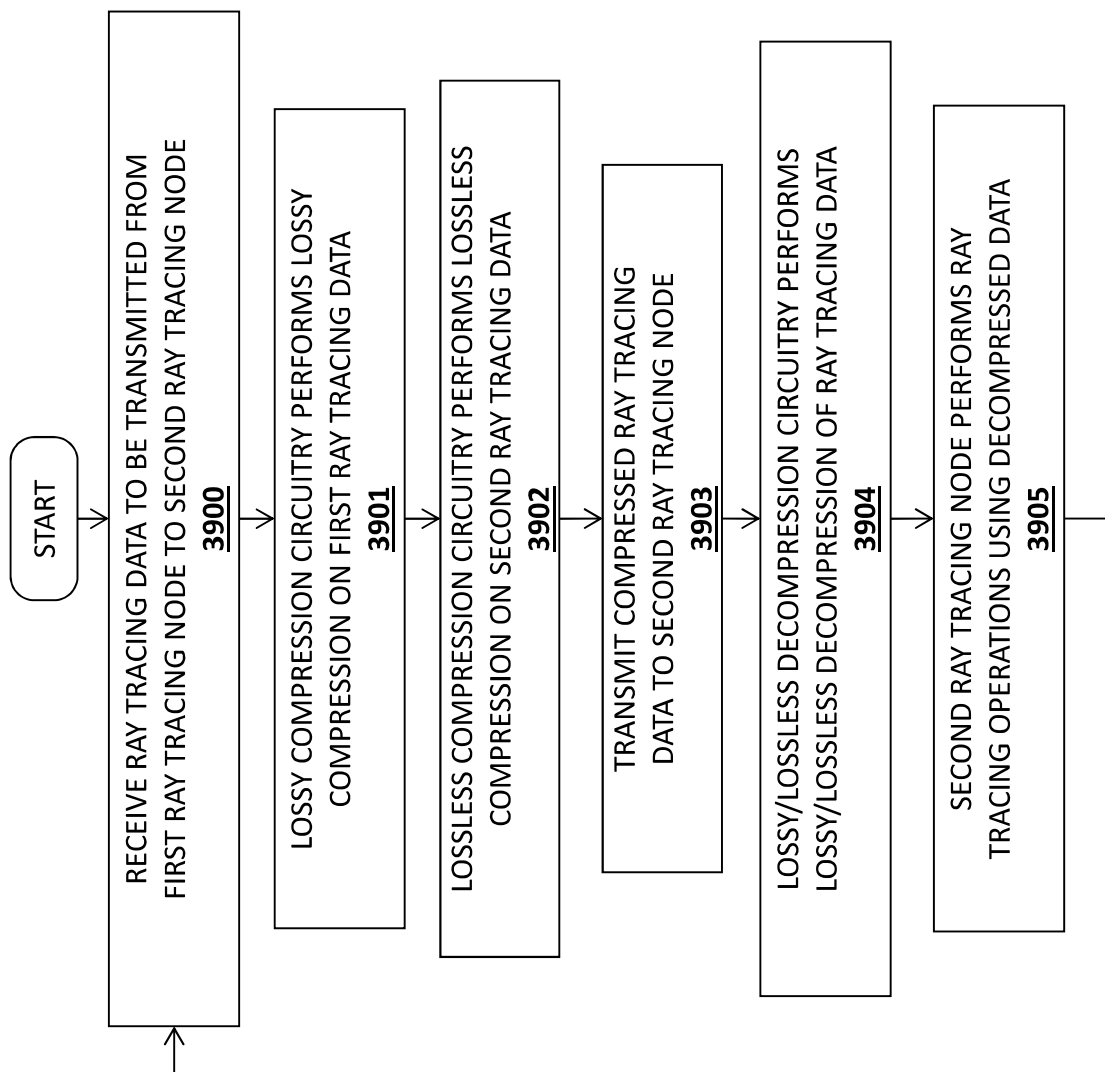


FIG. 39

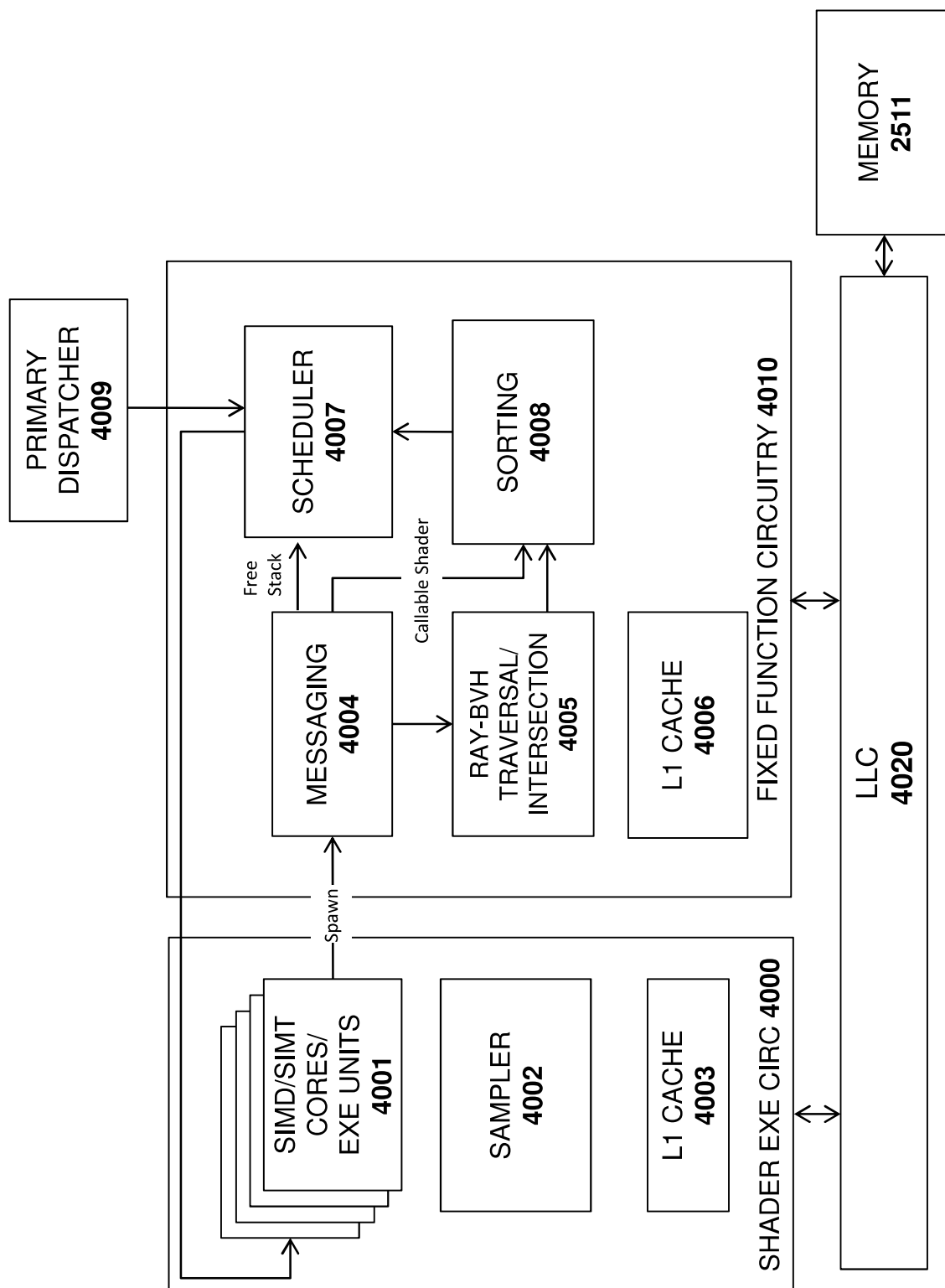
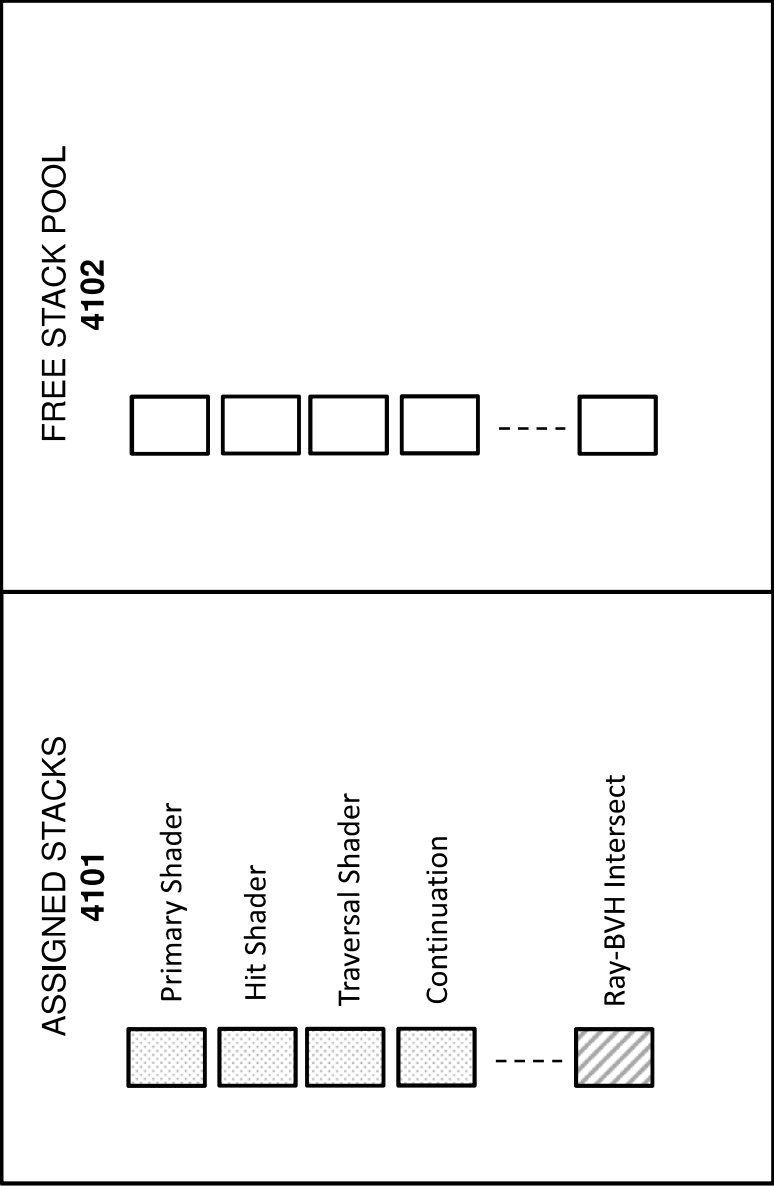


FIG. 40



CALL STACK REFERENCES

FIG. 41

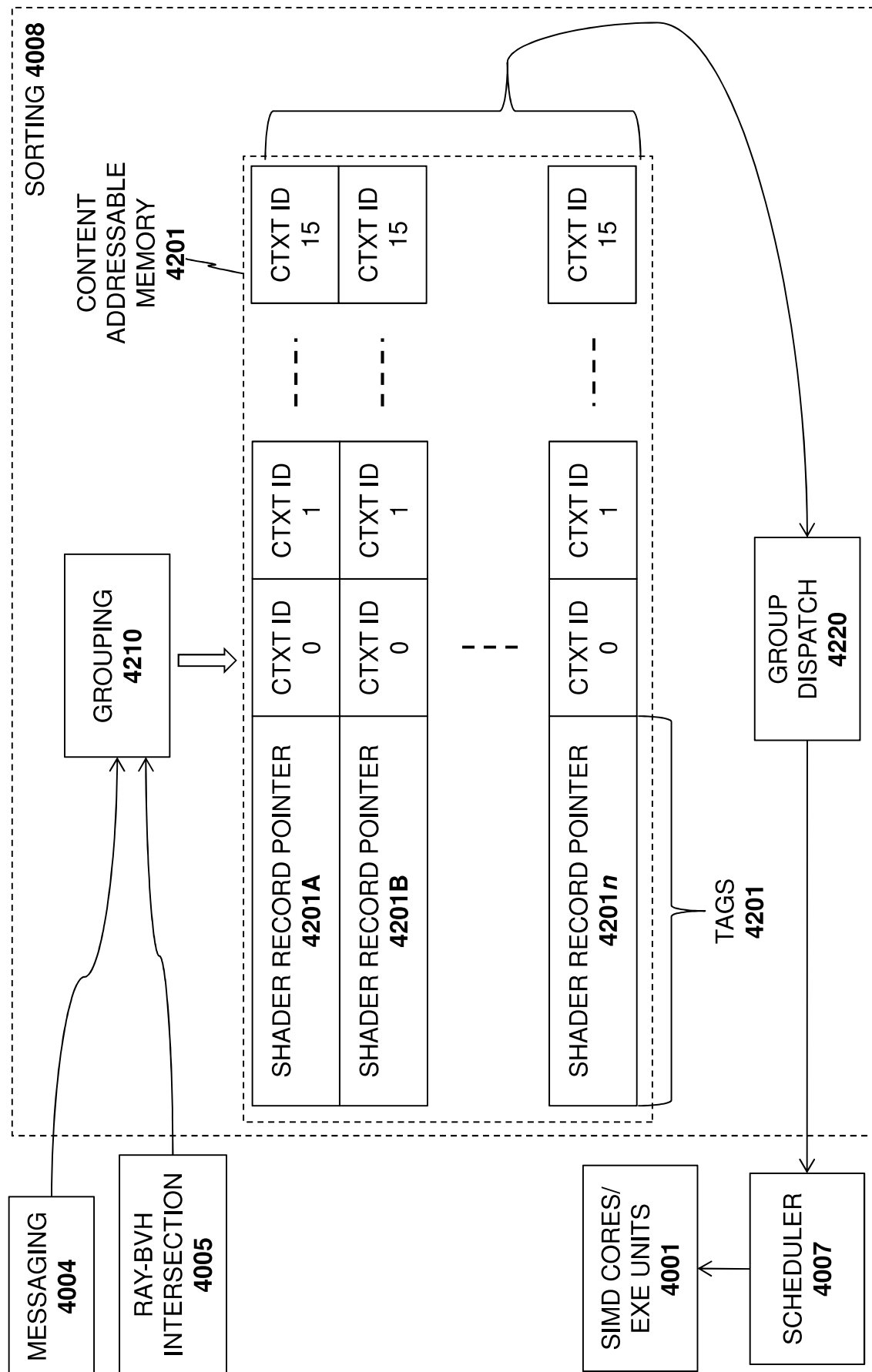


FIG. 42

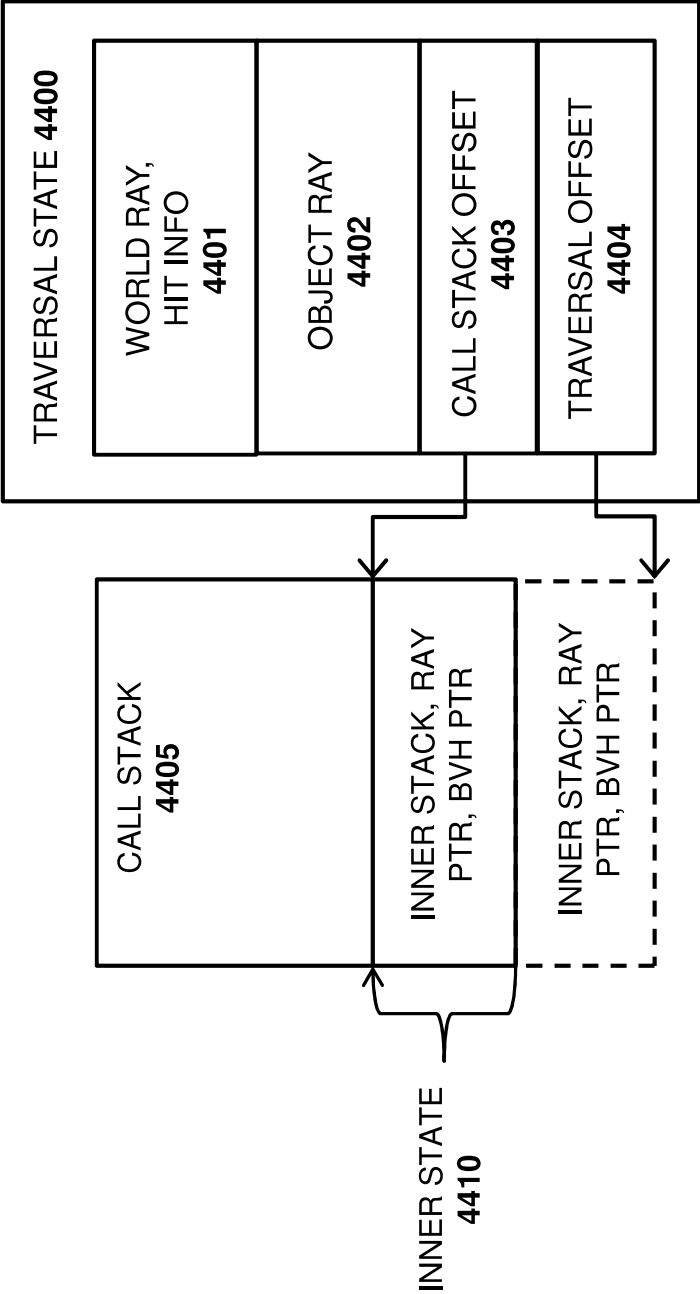


FIG. 44

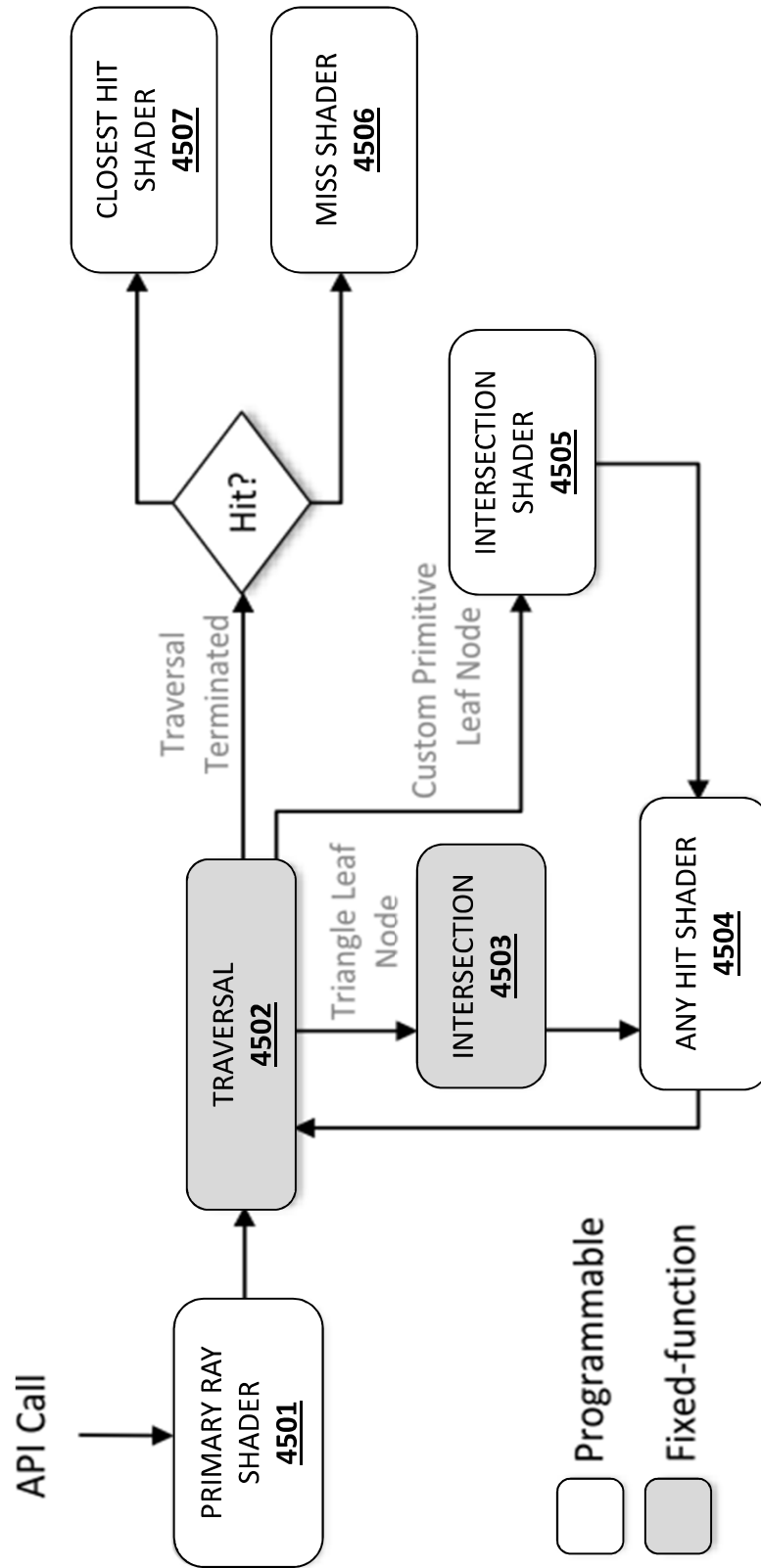


FIG. 45

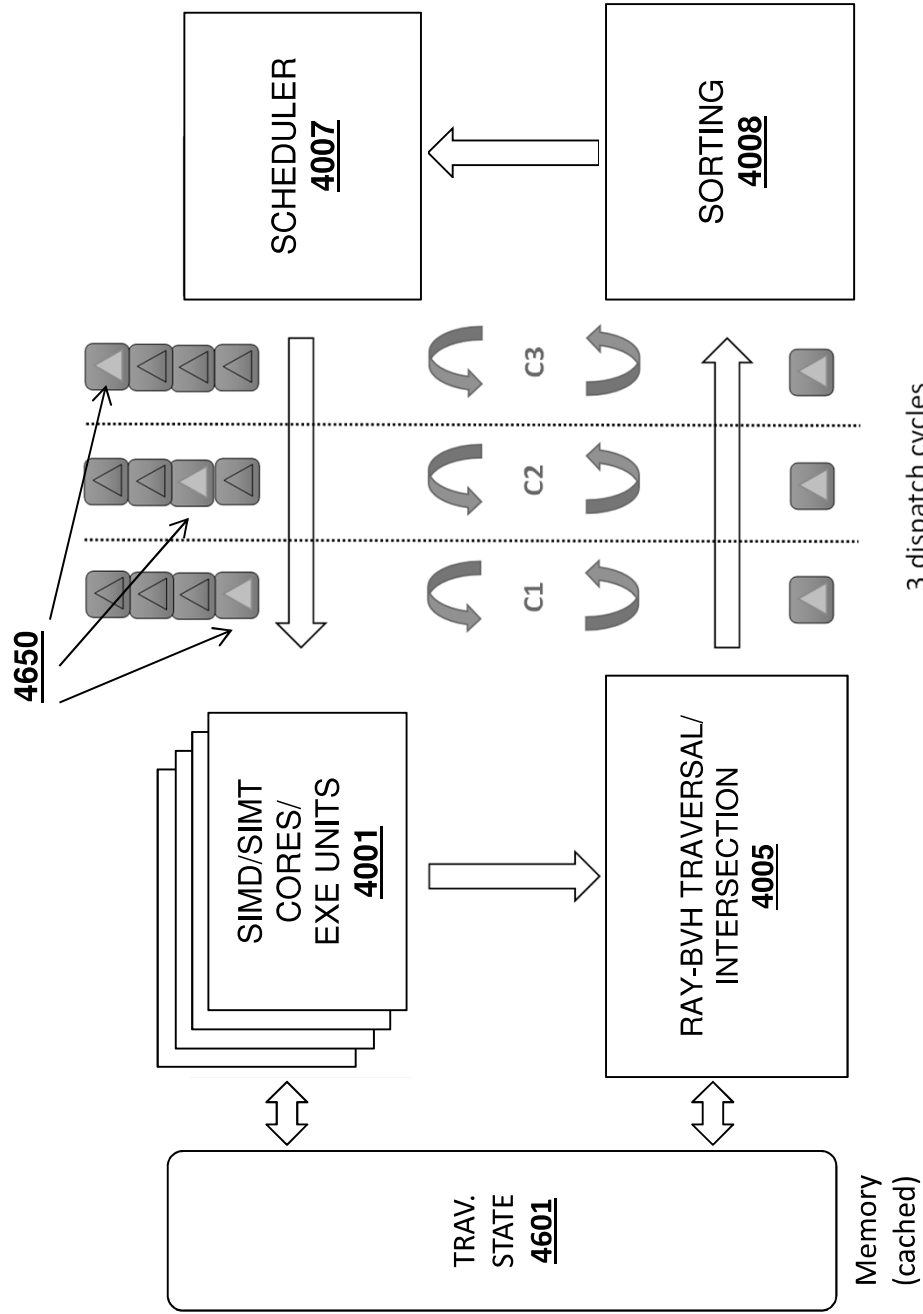
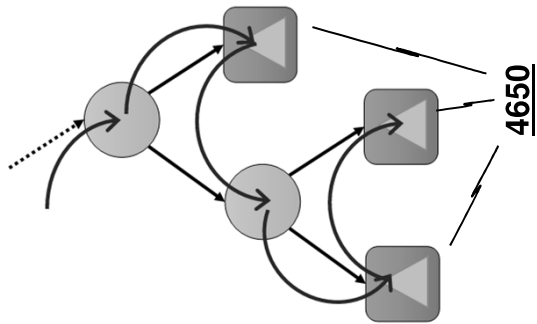


FIG. 46B

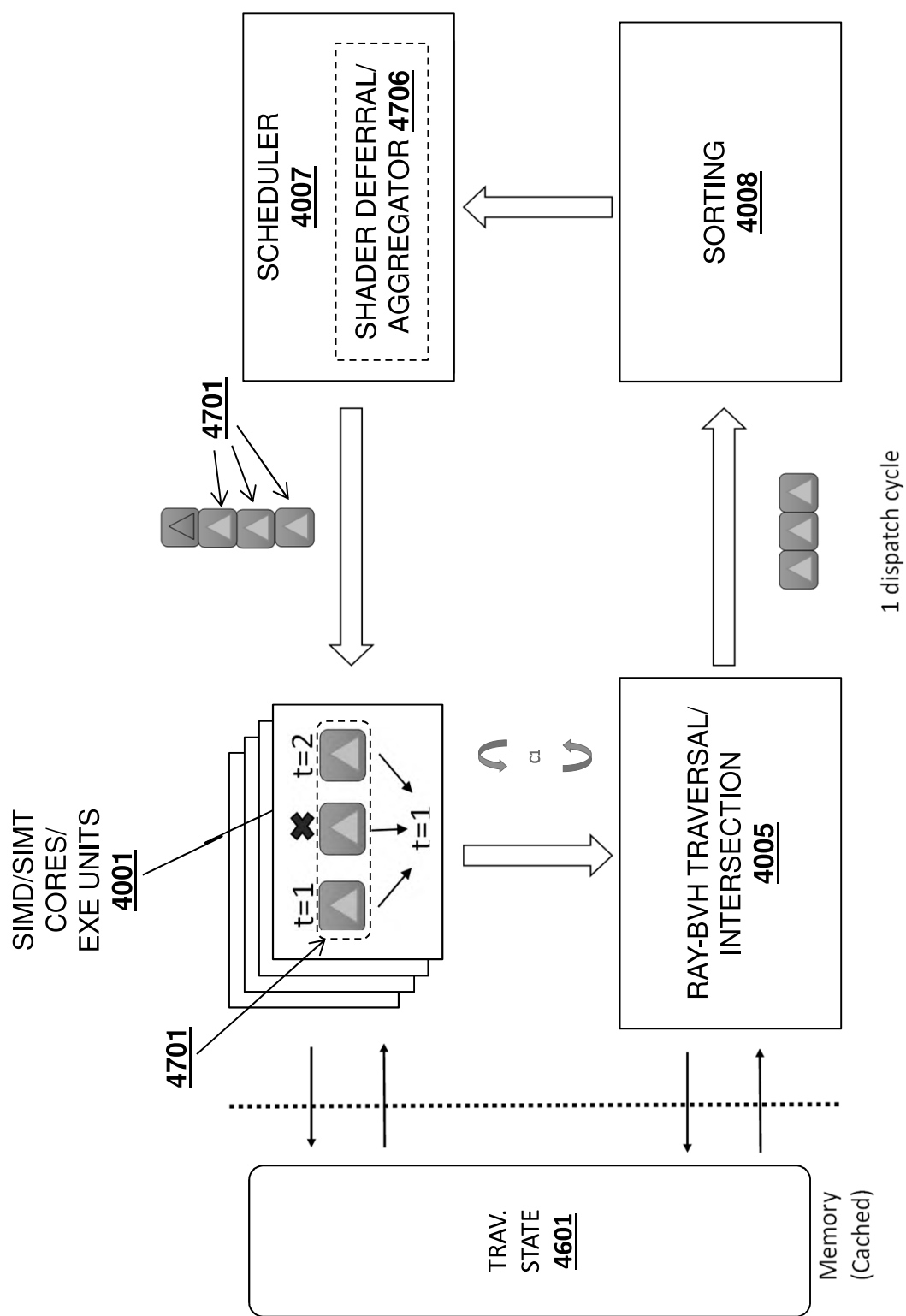


FIG. 47

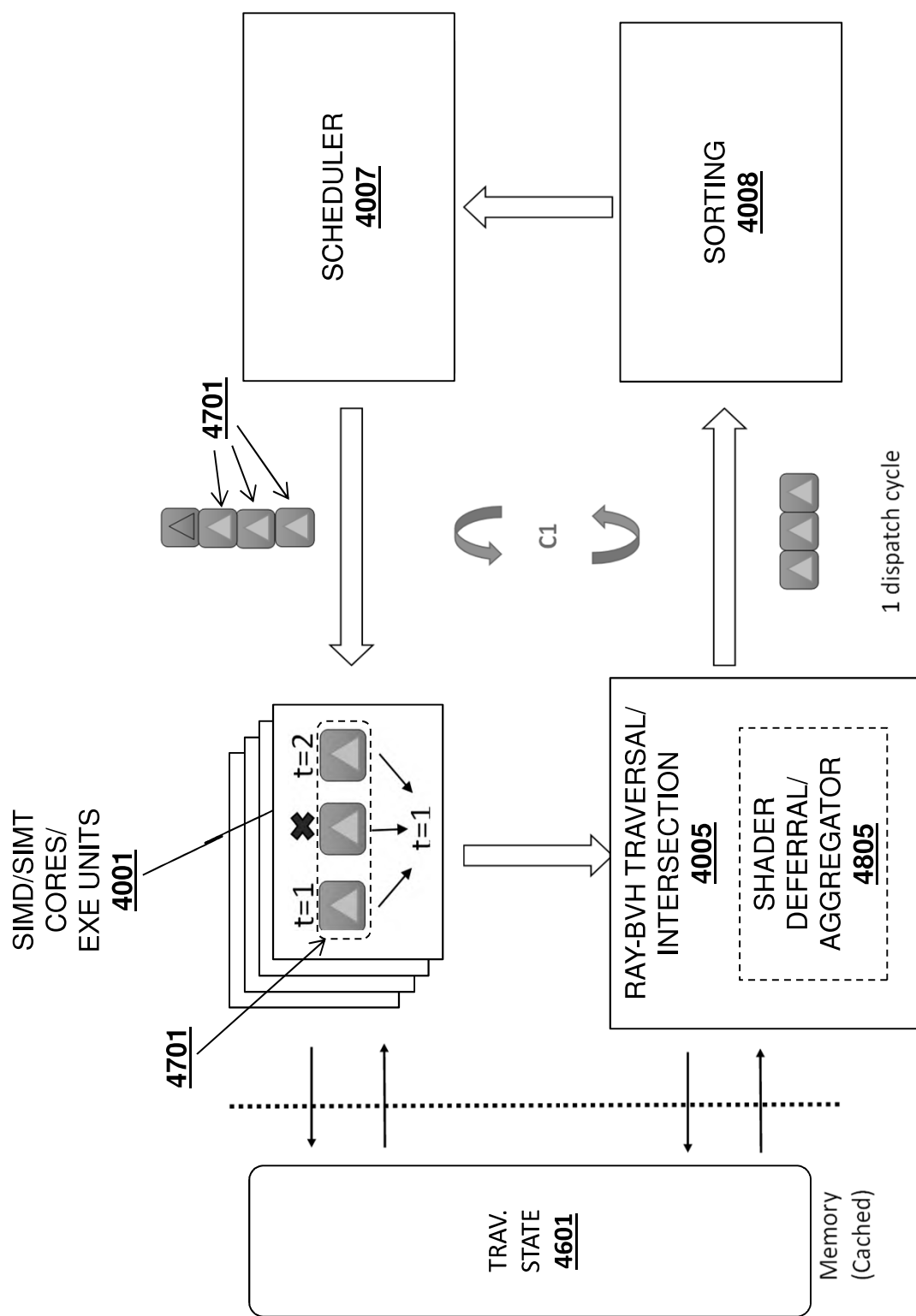


FIG. 48

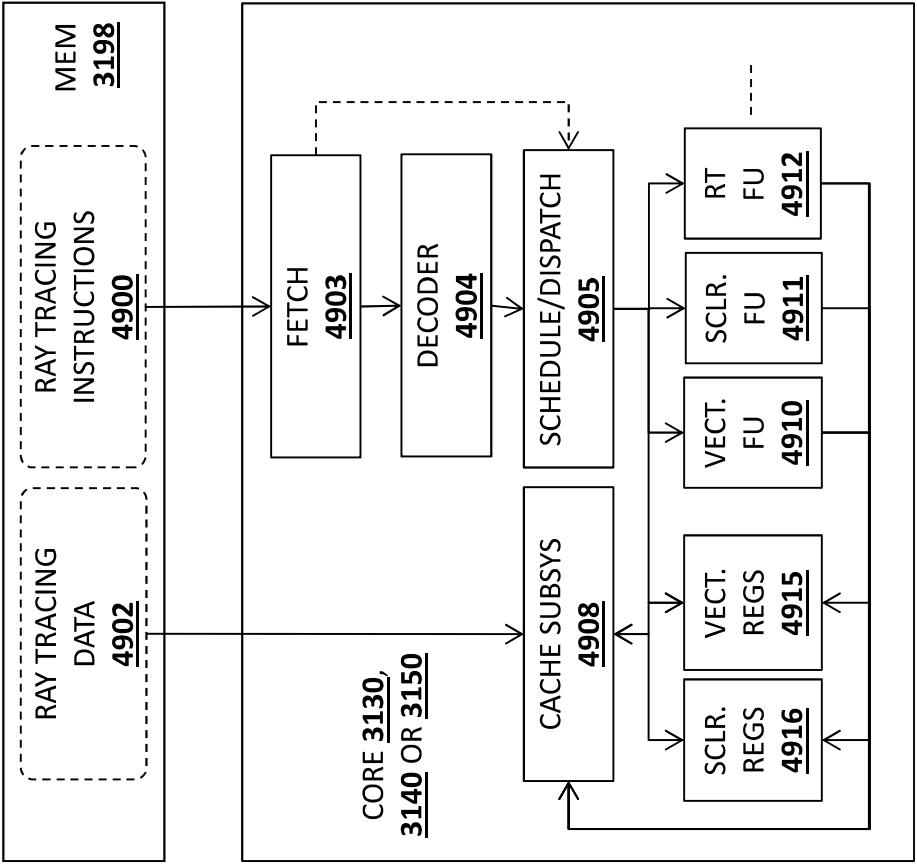


FIG. 49

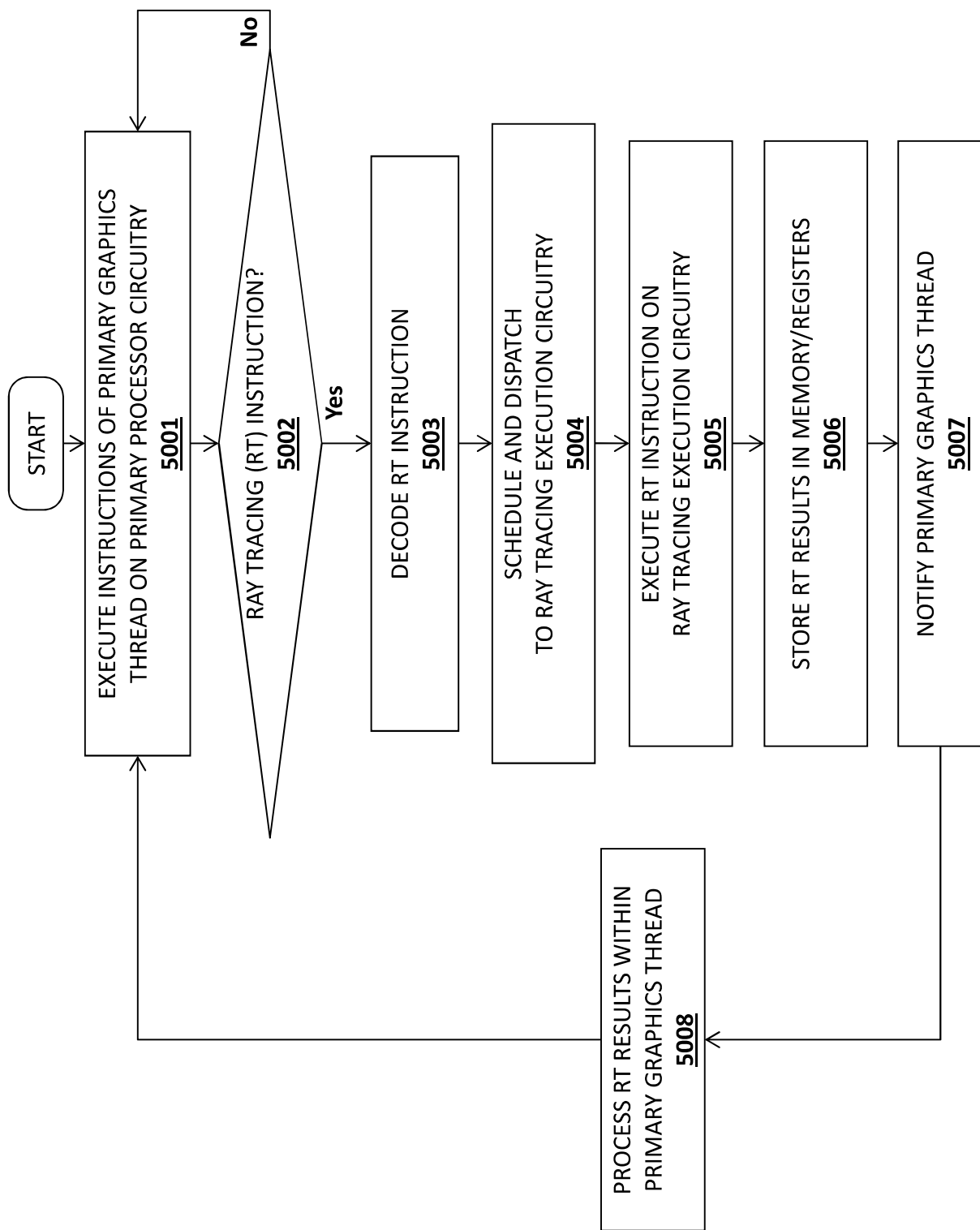


FIG. 50

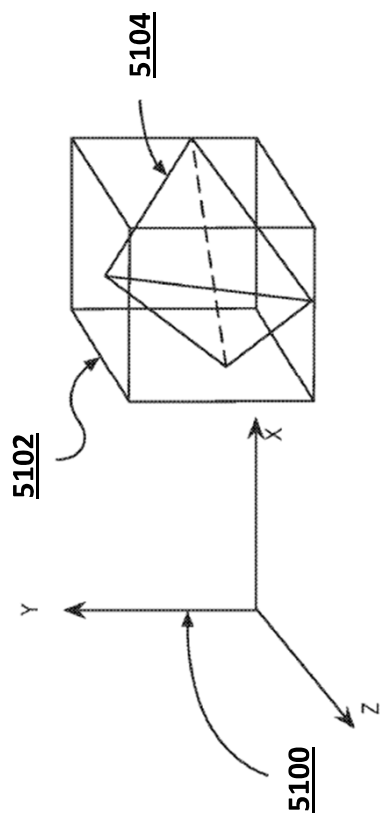


FIG. 51

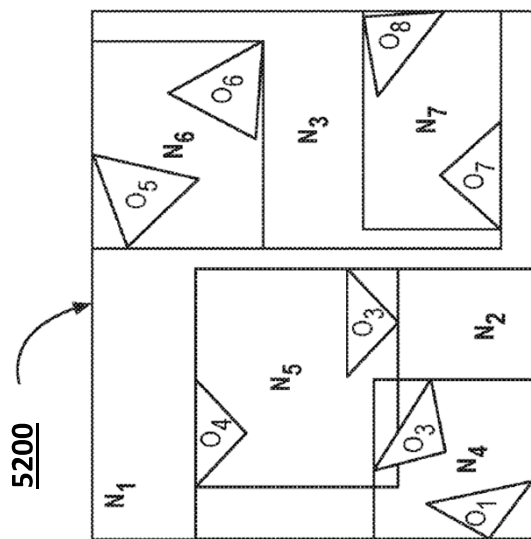


FIG. 52A

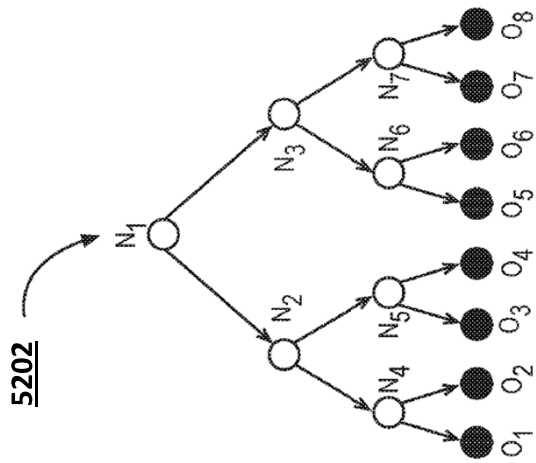


FIG. 52B

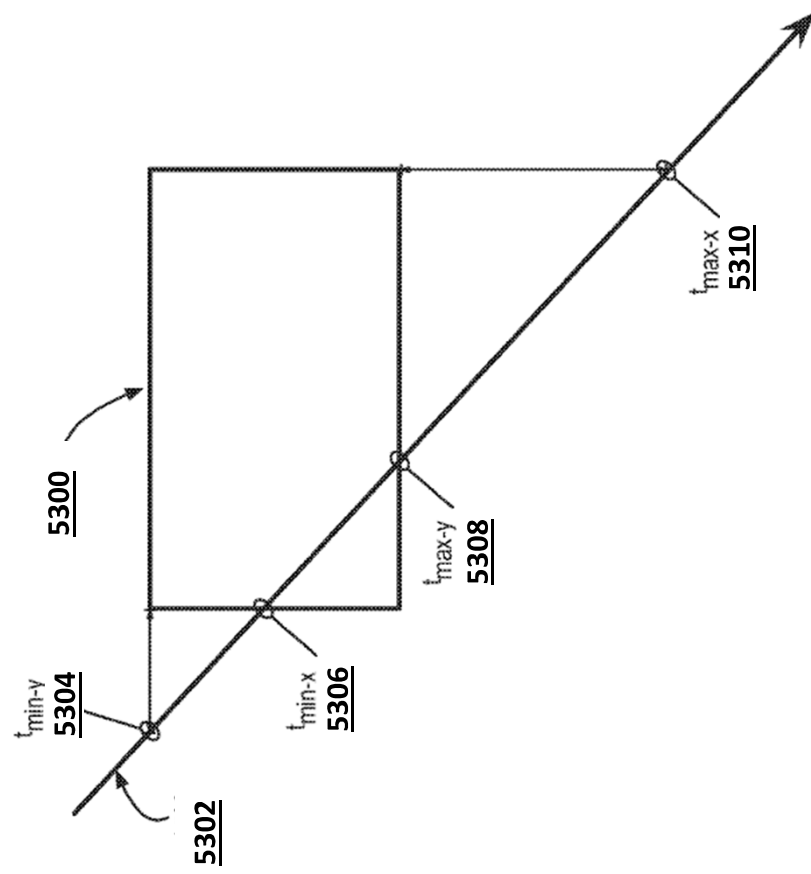


FIG. 53

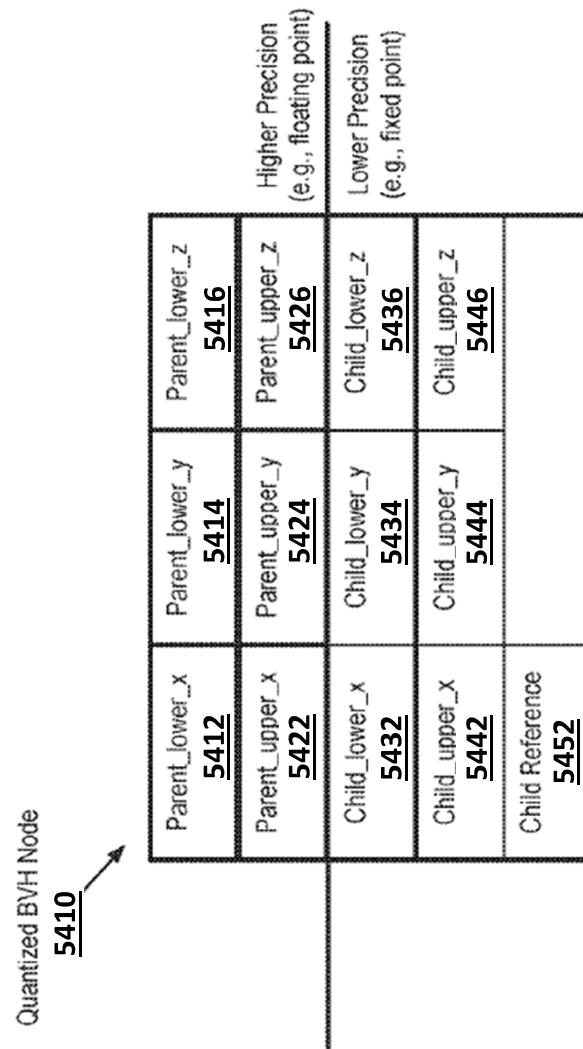
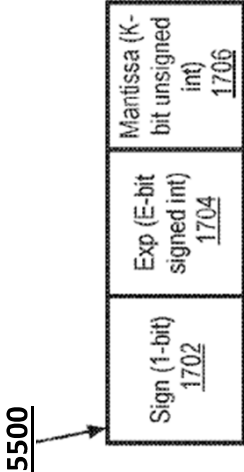


FIG. 54

Composite Floating Point Data Block



Quantized BVH Node

5510 →

			Higher Precision (e.g., CFP)	Lower Precision (e.g., fixed point)
Parent_lower_x <u>5512</u>	Parent_lower_y <u>5514</u>	Parent_lower_z <u>5516</u>		
Exp_x <u>5522</u>	Child_lower_x <u>5524</u>	Child_upper_x <u>5526</u>		
Exp_y <u>5532</u>	Child_lower_y <u>5534</u>	Child_upper_y <u>5536</u>		
Exp_z <u>5542</u>	Child_lower_z <u>5544</u>	Child_upper_z <u>5546</u>		
Child Reference <u>5552</u>				

FIG. 55

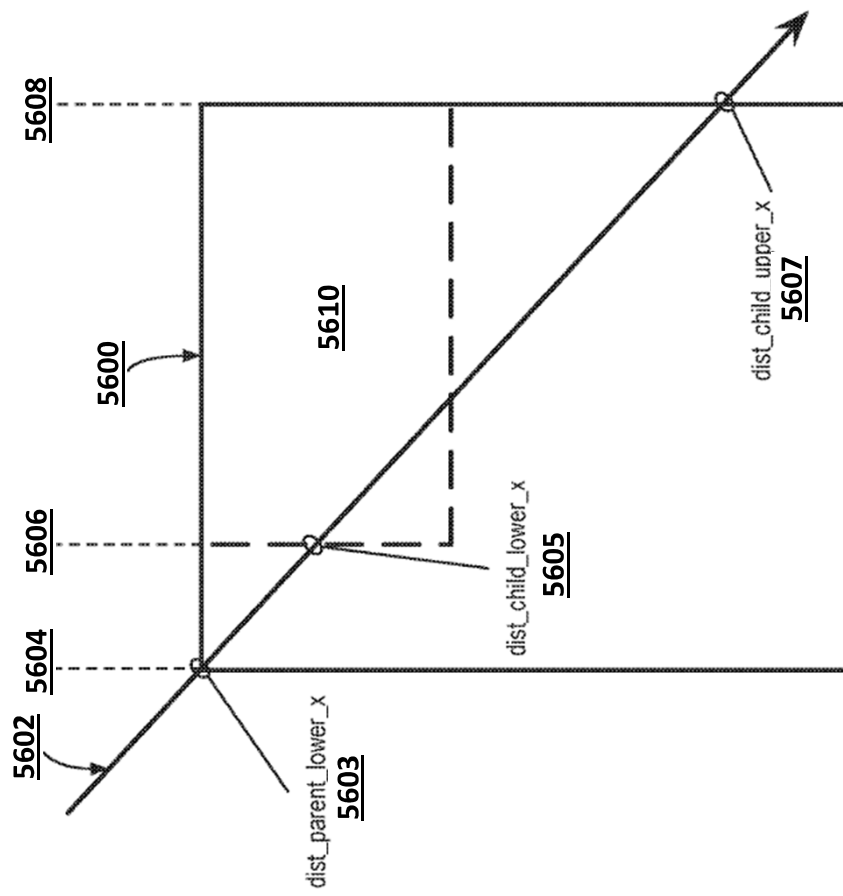


FIG. 56

BVH Decompression and Traversal Logic - 5700

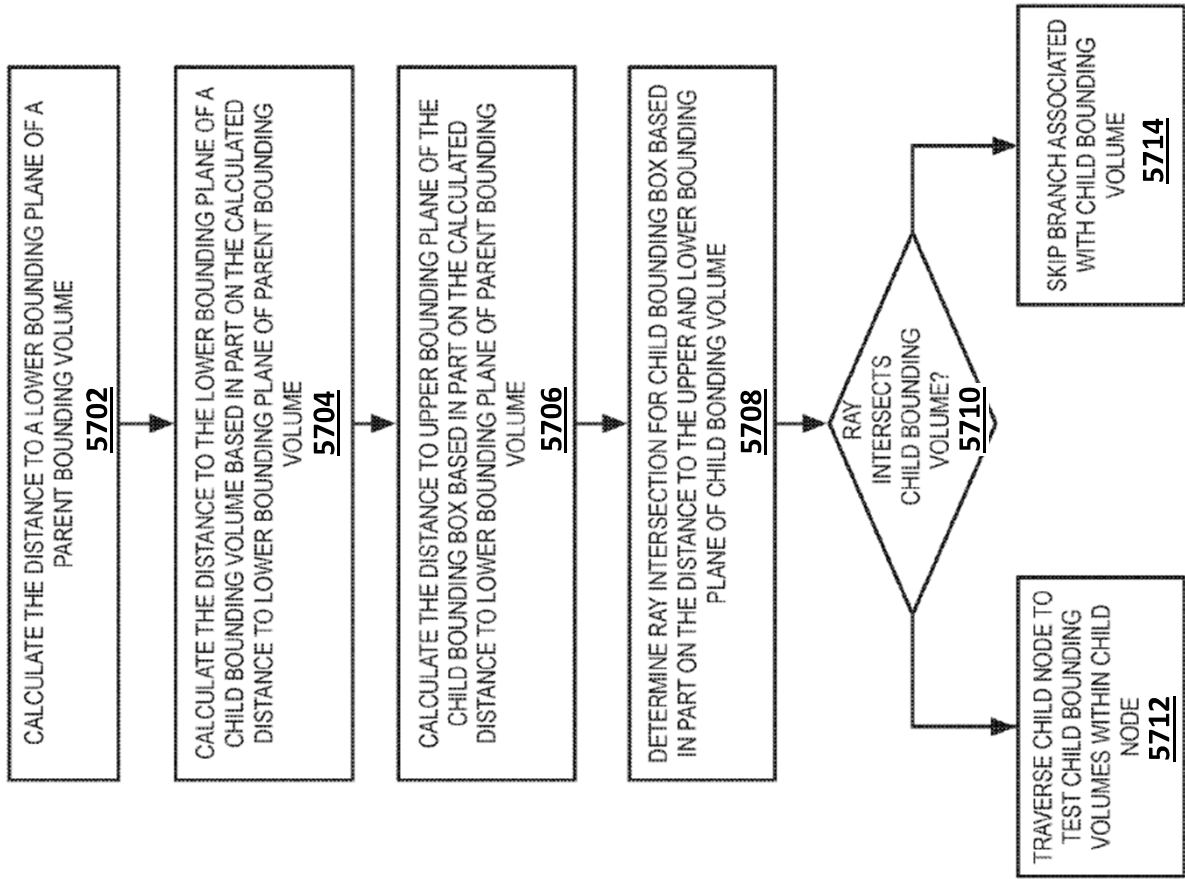


FIG. 57

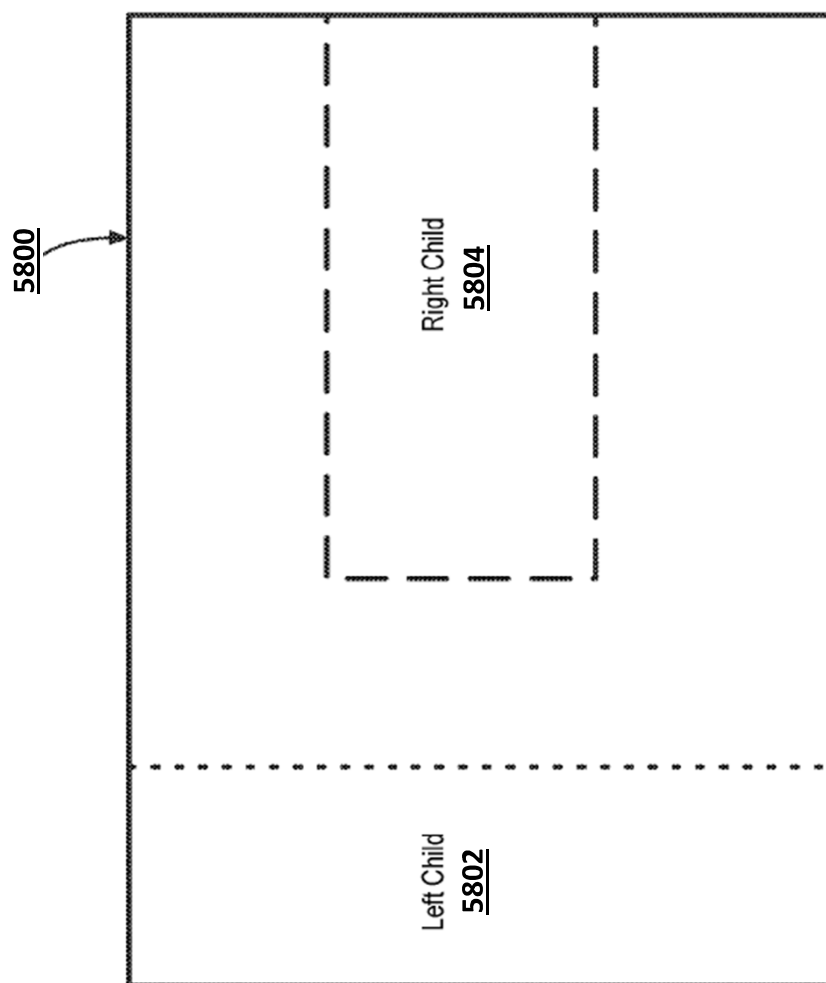


FIG. 58

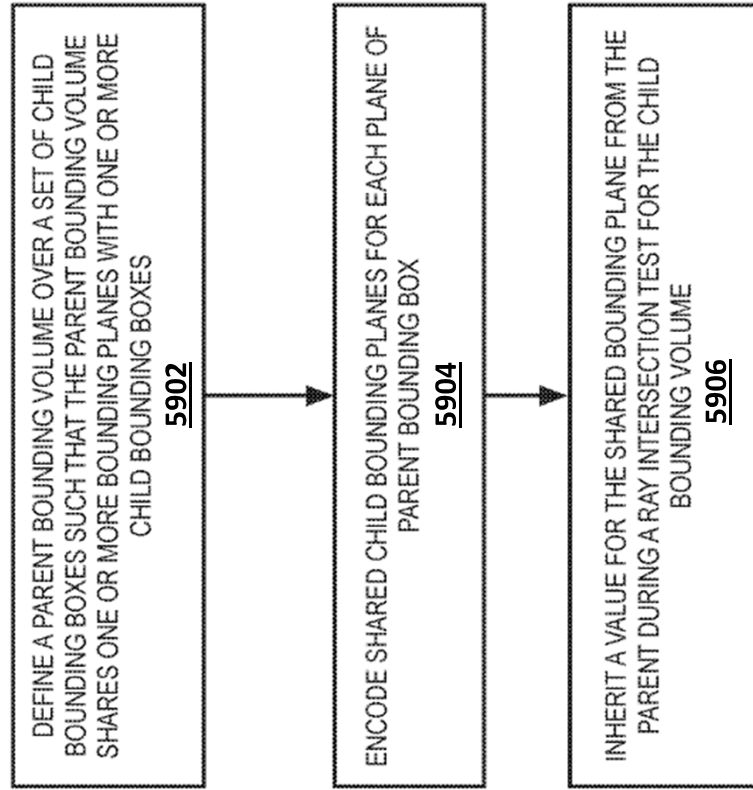


FIG. 59

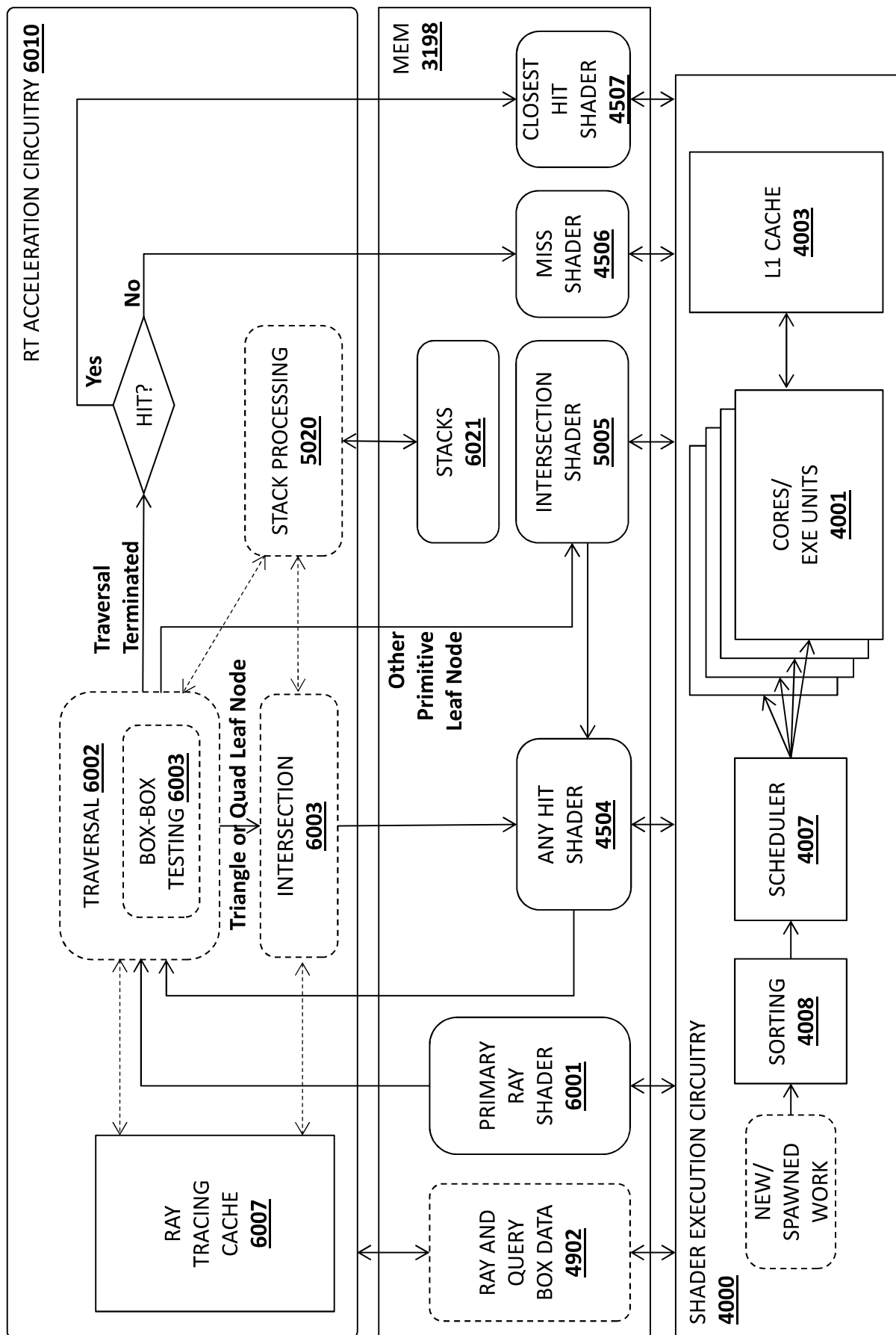


FIG. 60

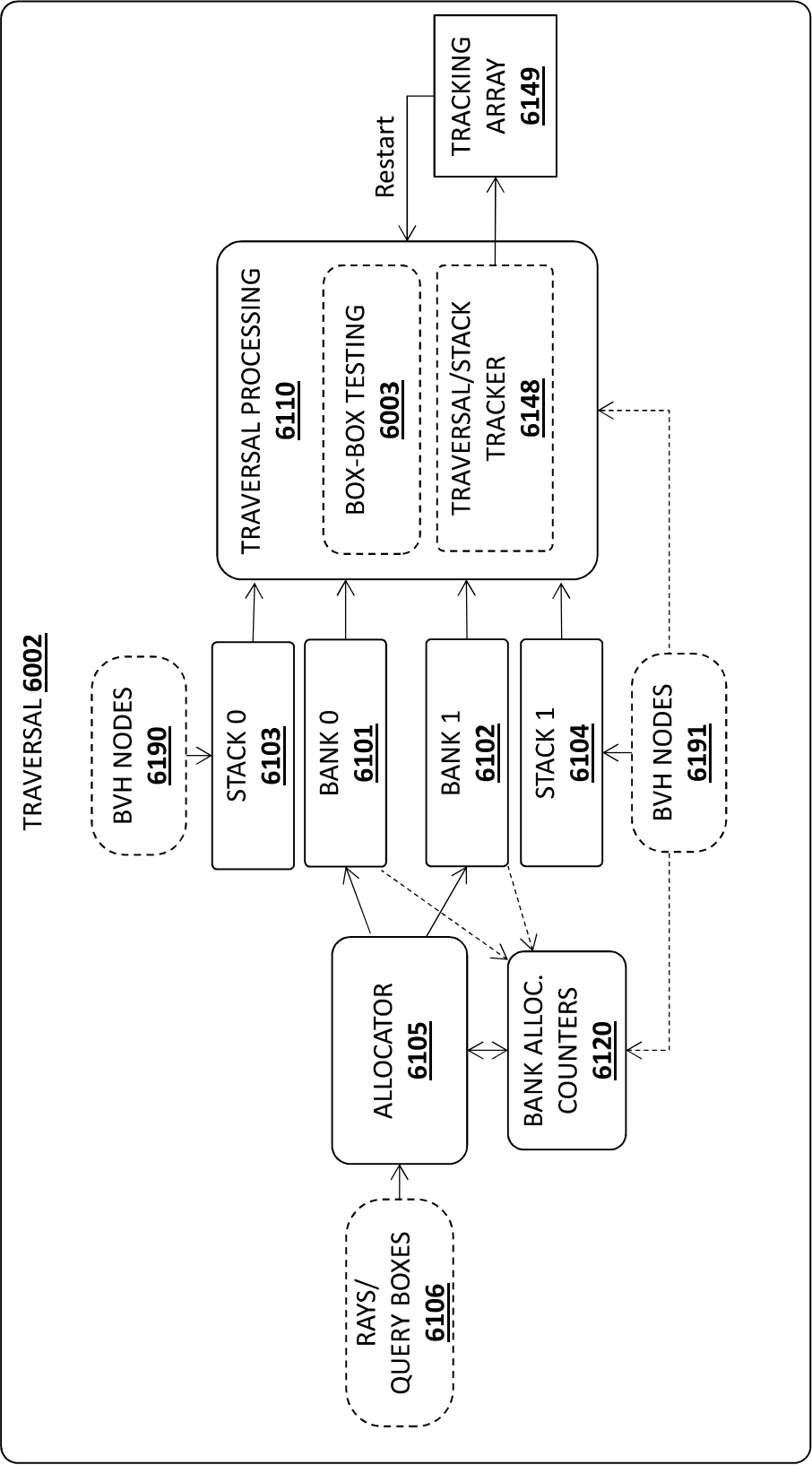


FIG. 61

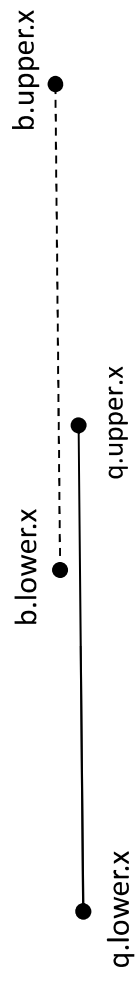


FIG. 62A

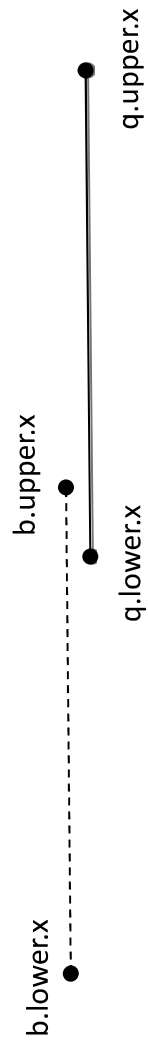


FIG. 62B

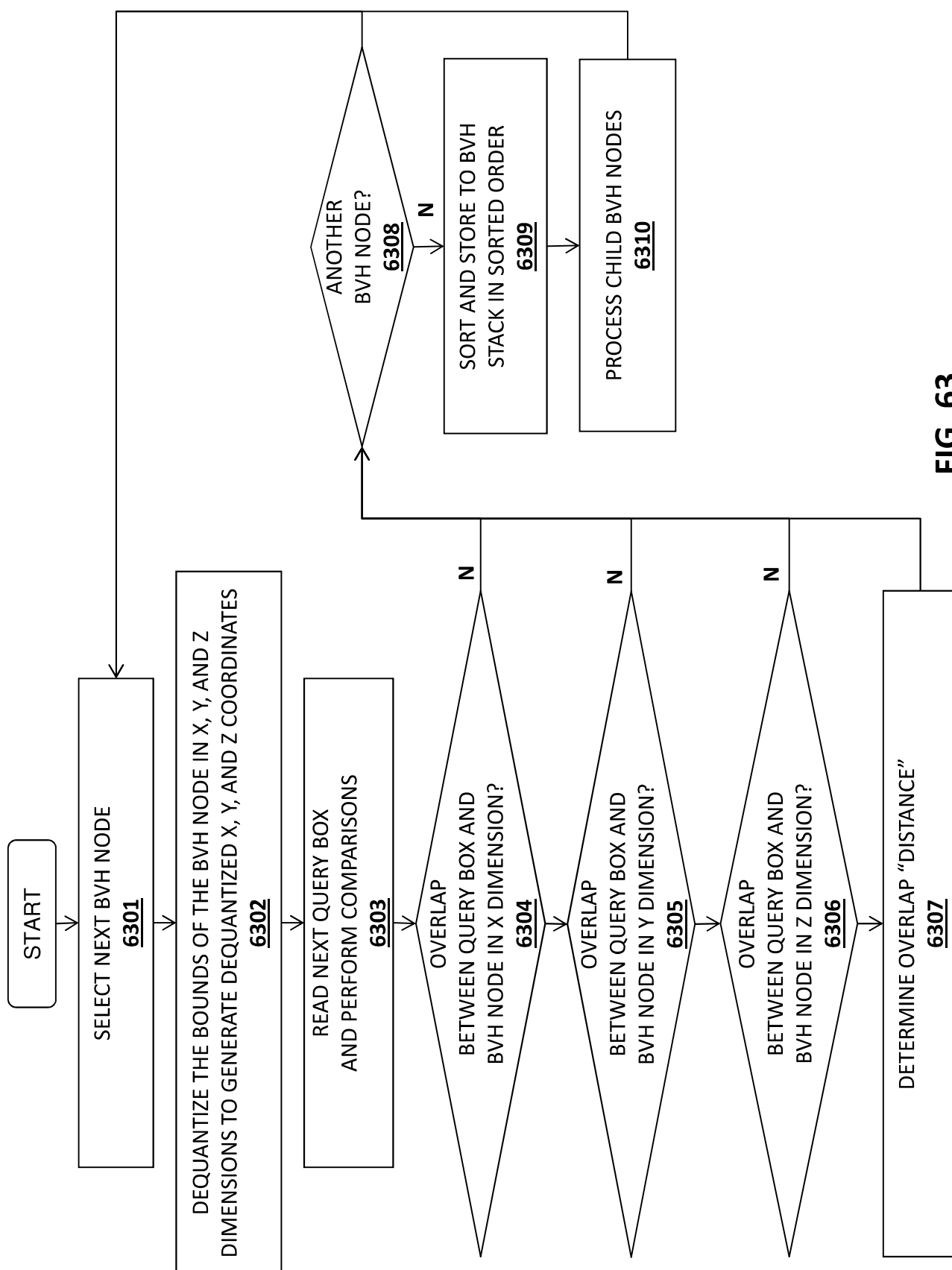


FIG. 63