



ABSTRACT OF THE DISCLOSURE

Disclosed is a multiplier comprising a first and second squaring circuits each having a differential input terminal pair whose outputs are connected in common. A first input terminal of the first squaring circuit is applied with a first input voltage and a second input terminal thereof is applied with a second input voltage opposite in phase to the first input voltage. A first input terminal of the second squaring circuit is applied with the second input voltage and a second input terminal thereof is applied with the first input voltage. The first and second squaring circuits each includes two sets of unbalanced differential transistor pairs which are arranged so that their inputs are opposite in phase and their outputs are connected in common. Said each unbalanced differential transistor pair has a different emitter size from each other. Two transistors having different emitter sizes constituting each differential transistor pair may be connected with an emitter resistor having a resistant value inversely proportional to the emitter size ratio to the both or one of them. The two transistors constituting said each differential transistor

pair may be equal in emitter size. In this case, only one transistor thereof has an emitter resistor connected. Also, in case of being equal in emitter size, one transistor thereof may have a Darlington connection.

This Sheet Has Been Replaced

