CLAIMS

WHAT IS CLAIMED IS:

1. A surface-mount structure comprising:

a sub-module, the sub-module comprising:

a dielectric layer;

at least one semiconductor device attached to the dielectric layer, with each of the at least one semiconductor device including a substrate composed of a semiconductor material;

a first level metal interconnect structure electrically coupled to the at least one semiconductor device, the metal interconnect structure extending through vias formed through the dielectric layer so as to be connected to the at least one semiconductor device; and

a second level input/output (I/O) connection electrically coupled to the first level metal interconnect structure and formed on the dielectric layer on a side opposite the at least one semiconductor device, the second level I/O connection configured to connect the sub-module to an external circuit;

a multi-layer substrate structure having a first surface and a second surface, wherein the at least one semiconductor device of the sub-module is attached to the first surface of the multi-layer substrate; and

one or more dielectric materials positioned between the dielectric layer and the first surface of the multi-layer substrate structure and at least partially about the at least one semiconductor device of the sub-module, the one or more dielectric materials configured to fill in gaps in the surface-mount structure and provide additional structural integrity thereto.

2. The surface-mount structure of claim 1 wherein the multi-layer substrate structure comprises:

a ceramic insulating layer;

a first metallic layer positioned on one side of the insulating layer to form the first surface of the multi-layer substrate structure; and

a second metallic layer positioned on another side of the insulating layer to form the second surface of the multi-layer substrate structure.

3. The surface-mount structure of claim 2 wherein the first and second metallic layers comprise first and second direct bond copper (DBC) layers.

4. The surface-mount structure of claim 3 wherein the first DBC layer comprises a patterned DBC layer and the second DBC layer comprises a patterned or unpatterned DBC layer.

5. The surface-mount structure of claim 3 wherein a volume of the second DBC layer is greater than a volume of the first DBC layer.

6. The surface-mount structure of claim 5 wherein the volume of the second DBC layer is between 1 and 2.5 times the volume of the first DBC layer.

7. The surface-mount structure of claim 5 wherein a thickness or area of the second DBC layer, and the corresponding volume, is controlled based on at least one of a thickness and material properties of the one or more dielectric materials, a density, thickness, and spacing of the at least one semiconductor device, and a thickness and material properties of the ceramic insulating layer.

8. The surface-mount structure of claim 7 wherein the material properties of the one or more dielectric materials and the ceramic insulating layer include at least one of an elastic modulus, coefficient of thermal expansion (CTE), and fracture stress and toughness.

9. The surface-mount structure of claim 5 wherein a volume ratio between the second DBC layer and the first DBC layer provides a stress balanced surface-mount packaging and interconnect structure that minimizes warpage and thermal stresses therein.

10. The surface-mount structure of claim 1 wherein the one or more dielectric materials comprises an underfill material, encapsulant, silicone or molding compound positioned between the dielectric layer and the first surface of the multi-layer substrate structure.

11. The surface-mount structure of claim 1 wherein one or more dielectric materials comprises:

a ceramic or dielectric sheet positioned between the dielectric layer and the first surface of the multi-layer substrate structure, the ceramic or dielectric sheet having cut-outs formed therein to receive the at least one semiconductor device; and

a dielectric filler material positioned between the ceramic or dielectric sheet and the first surface of the multi-layer substrate structure so as to fill-in gaps between the ceramic or dielectric sheet and the multi-layer substrate structure.

12. The surface-mount structure of claim 1 wherein the second level I/O connection comprises one of land grid array (LGA) solder bumps and ball grid array (BGA) solder bumps.

13. The surface-mount structure of claim 12 further comprising one of a solder material, a conductive adhesive, or sintered metal joint positioned between the multi-layer substrate structure and the sub-module to secure the sub-module to the multi-layer substrate structure.

14. The surface-mount structure of claim 1 wherein the sub-module comprises a power overlay (POL) sub-module.

15. The surface-mount structure of claim 1 wherein the at least one semiconductor device comprises a plurality of semiconductor devices attached to the dielectric layer.

CLAIMS

WHAT IS CLAIMED IS:

1. A surface-mount structure comprising:

a sub-module, the sub-module comprising:

a dielectric layer;

at least one semiconductor device attached to the dielectric layer, with each of the at least one semiconductor device including a substrate composed of a semiconductor material;

a first level metal interconnect structure electrically coupled to the at least one semiconductor device, the metal interconnect structure extending through vias formed through the dielectric layer so as to be connected to the at least one semiconductor device; and

a second level input/output (I/O) connection electrically coupled to the first level metal interconnect structure and formed on the dielectric layer on a side opposite the at least one semiconductor device, the second level I/O connection configured to connect the sub-module to an external circuit;

a multi-layer substrate structure having a first surface and a second surface, wherein the at least one semiconductor device of the sub-module is attached to the first surface of the multi-layer substrate; and

one or more dielectric materials positioned between the dielectric layer and the first surface of the multi-layer substrate structure and at least partially about the at least one semiconductor device of the sub-module, the one or more dielectric materials configured to fill in gaps in the surface-mount structure and provide additional structural integrity thereto.

2. The surface-mount structure of claim **1** wherein the multi-layer substrate structure comprises:

a ceramic insulating layer;

a first metallic layer positioned on one side of the insulating layer to form the first surface of the multi-layer substrate structure; and

a second metallic layer positioned on another side of the insulating layer to form the second surface of the multi-layer substrate structure.

3. The surface-mount structure of claim **2** wherein the first and second metallic layers comprise first and second direct bond copper (DBC) layers.

4. The surface-mount structure of claim **3** wherein the first DBC layer comprises a patterned DBC layer and the second DBC layer comprises a patterned or unpatterned DBC layer.

5. The surface-mount structure of claim **3** wherein a volume of the second DBC layer is greater than a volume of the first DBC layer.

6. The surface-mount structure of claim **5** wherein the volume of the second DBC layer is between 1 and 2.5 times the volume of the first DBC layer.

7. The surface-mount structure of claim **5** wherein a thickness or area of the second DBC layer, and the corresponding volume, is controlled based on at least one of a thickness and material properties of the one or more dielectric materials, a density, thickness, and spacing of the at least one semiconductor device, and a thickness and material properties of the ceramic insulating layer.

8. The surface-mount structure of claim **7** wherein the material properties of the one or more dielectric materials and the ceramic insulating layer include at least one of an elastic modulus, coefficient of thermal expansion (CTE), and fracture stress and toughness.

9. The surface-mount structure of claim **1** wherein the one or more dielectric materials comprises an underfill material, encapsulant, silicone or molding compound positioned between the dielectric layer and the first surface of the multi-layer substrate structure.

10. The surface-mount structure of claim **1** wherein one or more dielectric materials comprises:

a ceramic or dielectric sheet positioned between the dielectric layer and the first surface of the multi-layer substrate structure, the ceramic or dielectric sheet having cut-outs formed therein to receive the at least one semiconductor device; and

a dielectric filler material positioned between the ceramic or dielectric sheet and the first surface of the multi-layer substrate structure so as to fill-in gaps between the ceramic or dielectric sheet and the multi-layer substrate structure.

11. The surface-mount structure of claim **1** wherein the second level I/O connection comprises one of land grid array (LGA) solder bumps and ball grid array (BGA) solder bumps.

12. The surface-mount structure of claim **11** further comprising one of a solder material, a conductive adhesive, or sintered metal joint positioned between the multi-layer substrate structure and the sub-module to secure the sub-module to the multi-layer substrate structure.

13. The surface-mount structure of claim **1** wherein the sub-module comprises a power overlay (POL) sub-module.

14. A method of manufacturing a surface-mount packaging and interconnect structure comprising:

constructing a sub-module including at least one semiconductor device and a packaging structure formed thereabout, wherein constructing the sub-module comprises:

attaching the at least one semiconductor device to a dielectric layer;

forming a first-level metallic interconnect structure over the dielectric layer, the first-level metallic interconnect structure extending through vias in the dielectric layer to electrically connect to the at least one semiconductor device; and

forming a second level input/output (I/O) connection on the dielectric layer on a side opposite the at least one semiconductor device, the second level I/O connection configured to connect the sub-module to an external circuit;

forming a substrate structure that includes a center substrate layer and first and second metallic layers on opposing sides of the center substrate layer, such that the first and second metallic layers form a first surface and a second surface, respectively, of the substrate structure;

attaching the sub-module to the first surface of the substrate structure; and

providing a dielectric filler material between the dielectric layer and the first surface of the substrate structure, the dielectric filler material being provided at least partially about the at least one semiconductor device of the sub-module.

15. The method of claim **14** wherein forming the substrate structure further comprises:

determining a desired volume ratio of the second metallic layer to the first metallic layer; and

forming the second metallic layer to have a thickness and area that provides the desired volume ratio of the second metallic layer to the first metallic layer.

16. The method of claim **15** wherein determining the desired volume ratio of the second metallic layer to the first metallic layer is based on at least one of a thickness and material properties of the dielectric filler material; a density, thickness, and spacing of the at least one semiconductor device; and a thickness and material properties of the center substrate layer.

17. The method of claim **16** wherein the material properties of the dielectric filler material and the center substrate layer include at least one of an elastic modulus, coefficient of thermal expansion (CTE), and fracture stress and toughness.

18. The method of claim **15** wherein the desired volume ratio of the second metallic layer to the first metallic layer is between 1 and 2.5.

19. The method of claim **15** wherein the desired volume ratio of the second metallic layer to the first metallic layer provides a stress balanced surface-mount packaging and interconnect structure that minimizes warpage and thermal stresses therein.

20. The method of claim **14** wherein providing the dielectric filler material comprises:

providing a ceramic or dielectric sheet positioned between the dielectric layer and the first surface of the substrate structure, the ceramic or dielectric sheet having cut-outs formed therein to receive the at least one semiconductor device; and

providing an underfill material or molding compound positioned between the ceramic or dielectric sheet and the first surface of the substrate structure so as to fill-in gaps between the ceramic or dielectric sheet and the substrate structure.

21. A power overlay (POL) packaging structure comprising:

a POL sub-module, the POL sub-module comprising:

a dielectric layer;

a plurality of semiconductor devices attached to the dielectric layer;

a first level interconnect structure electrically coupled to the plurality of semiconductor devices, the first level interconnect structure extending through vias formed through the dielectric layer so as to be connected to the plurality of semiconductor devices; and

a second level interconnect structure to electrically couple the POL sub-module to an external circuit structure, the second level interconnect structure comprising a plurality of solder bumps formed over the dielectric layer and first level interconnect structure and configured to make an interconnection to the external circuit structure;

a multi-layer substrate structure having a first surface and a second surface, wherein the plurality of semiconductor devices of the POL sub-module is attached to the first surface of the multi-layer substrate structure, and wherein the multi-layer substrate structure includes:

a first direct bond copper (DBC) layer forming the first surface of the multi-layer substrate structure;

a second DBC layer forming the second surface of the multi-layer substrate structure; and

a ceramic layer sandwiched between the first and second DBC layers; and

a dielectric filler material positioned between the dielectric layer and the first surface of the multi-layer substrate structure and at least partially about the plurality of semiconductor devices of the sub-module.

22. The POL packaging structure of claim **21** wherein there is a volume imbalance between the first DBC layer and the second DBC layer, with the second DBC layer having a greater volume than the first DBC layer; and

wherein the volume of the second DBC layer is determined based on at least one of a thickness and material properties of the dielectric filler material, a density, thickness, and spacing of the plurality of semiconductor devices, and a thickness and material properties of the ceramic layer, with the material properties of the dielectric filler material and the ceramic layer comprising at least one of an elastic modulus, coefficient of thermal expansion (CTE), and fracture stress and toughness.

23. The POL packaging structure of claim **22** wherein the volume imbalance between the first DBC layer and the second DBC layer is between 1 and 2.5.

24. The POL packaging structure of claim **21** wherein the dielectric filler material comprises an underfill material, encapsulate, silicone or a molding compound, or a combination of a ceramic or dielectric sheet and a dielectric filler material.