

Abstract

5 An integrated circuit (IC 100) includes circuitry for generating a clock signal (CLOCK) during both a normal mode of operation and a test mode of operation. During the normal mode, an input clock signal is delayed via a skew corrector (135). In test mode, an input test clock signal (TEST CLOCK) bypasses the skew corrector via a clock signal source selector (150). The clock signal source selector is controlled automatically by a mode detector
10 (140) that responds to the input clock signals to determine the mode of operation of the IC.

This Sheet Has Been Replaced

