

ABSTRACT

DISTRIBUTED CLOCK SIGNAL AND CLOCK SIGNAL INTERRUPT

A clock distribution system and clock interrupt system for an integrated circuit device. Ignoring effects associated with the matched stages, the present invention includes a clock distribution and interrupt system for providing clock signals with less than 100 picoseconds of skew to various components of an integrated circuit device. The present invention utilizes several stages of drivers to evenly supply the distributed clock signals and each stage has RC matched input lines. The present invention advantageously locates the matched stages and clock drivers within the power supply ring of the integrated circuit located on the periphery of the microprocessor topology. This is done in order to better predict the topology surrounding these lines to match the capacitance of these lines. Further, this metal level offers a larger width dimension line (since as a top layer it may be thicker) having less resistance per unit area and also generally avoids spatial competition with other IC components and circuitry. The present invention additionally offers the capability of selectively powering down various components within the integrated device with a power management unit and enable network that is included as a component of the clock distribution system.

(Figure 3)

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