

DESCRIPTION

SEMICONDUCTOR DEVICE AND

METHOD FOR PRODUCING SAME

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device which has been formed using an oxide semiconductor and a method for fabricating such a device, and more particularly relates to an active-matrix substrate for use in a liquid crystal display device or an organic EL display device and a method for fabricating such a substrate. In this description, the "semiconductor devices" include an active-matrix substrate and a display device which uses the active-matrix substrate.

BACKGROUND ART

[0002] An active-matrix substrate for use in a liquid crystal display device and other devices includes switching elements such as thin-film transistors (which will be simply referred to herein as "TFTs"), each of which is provided for an associated one of pixels. An active-matrix substrate

including TFTs as switching elements is called a "TFT substrate".

[0003] As for TFTs, a TFT which uses an amorphous silicon film as its active layer (and will be referred to herein as an "amorphous silicon TFT") and a TFT which uses a polysilicon film as its active layer (and will be referred to herein as a "polysilicon TFT") have been used extensively.

[0004] Recently, people have proposed that an oxide semiconductor be used as a material for the active layer of a TFT instead of amorphous silicon or polysilicon. Such a TFT will be referred to herein as an "oxide semiconductor TFT". Since an oxide semiconductor has higher mobility than amorphous silicon, the oxide semiconductor TFT can operate at higher speeds than an amorphous silicon TFT. Also, such an oxide semiconductor film can be formed by a simpler process than a polysilicon film.

[0005] Patent Document No. 1 discloses a method for fabricating a TFT substrate including oxide semiconductor TFTs. According to the method disclosed in Patent Document No. 1, a TFT substrate can be fabricated in a reduced number

of manufacturing process steps by forming a pixel electrode with the resistance of the oxide semiconductor layer locally decreased.

[0006] Recently, as the definition of liquid crystal display devices and other devices has become higher and higher, a decrease in pixel aperture ratio has become an increasingly serious problem. In this description, the "pixel aperture ratio" refers herein to the ratio of the combined area of pixels (e.g., the combined area of regions which transmit light that contributes to a display operation in a transmissive liquid crystal display device) to the overall display area. In the following description, the "pixel aperture ratio" will be simply referred to herein as an "aperture ratio".

[0007] Among other things, a medium to small sized transmissive liquid crystal display device to be used in a mobile electronic device has so small a display area that each of its pixels naturally has a very small area and the aperture ratio will decrease particularly significantly when the definition is increased. On top of that, if the aperture

ratio of a liquid crystal display device to be used in a mobile electronic device decreases, the luminance of the backlight needs to be increased to achieve an intended brightness, thus causing an increase in power dissipation, too.

[0008] To achieve a high aperture ratio, the combined area occupied by a TFT, a storage capacitor, and other elements of a non-transparent material in each pixel may be decreased. However, naturally, the TFT and the storage capacitor should have their minimum required size to perform their function. When oxide semiconductor TFTs are used as TFTs, the TFTs can have a smaller size than when amorphous silicon TFTs are used, which is advantageous. It should be noted that in order to maintain a voltage that has been applied to the liquid crystal layer of a pixel (which is called a "liquid crystal capacitor" electrically), the "storage capacitor" is provided electrically in parallel with the liquid crystal capacitor. In general, at least a portion of the storage capacitor is arranged so as to overlap with the pixel.

CITATION LIST

PATENT LITERATURE

[0009]

Patent Document No. 1: Japanese Laid-Open Patent

Publication No. 2011-91279

SUMMARY OF INVENTION

TECHNICAL PROBLEM

[0010] However, demands for increased aperture ratios are too huge to satisfy just by using oxide semiconductor TFTs. Meanwhile, as the prices of display devices have become lower and lower year after year, development of a technology for manufacturing high-aperture-ratio display devices at a lower cost is awaited.

[0011] Thus, a primary object of an embodiment of the present invention is to provide a TFT substrate which can be fabricated by a simpler process and which can contribute to realizing a display device with higher definition and a higher aperture ratio than conventional ones and also provide a method for fabricating such a TFT substrate.

SOLUTION TO PROBLEM

[0012] A semiconductor device according to an embodiment of the present invention includes: a substrate; a gate electrode formed on the substrate; a gate insulating layer formed over the gate electrode; an oxide semiconductor layer formed on the gate insulating layer; source and drain electrodes electrically connected to the oxide semiconductor layer; a first transparent electrode electrically connected to the drain electrode; a dielectric layer formed over the source and drain electrodes; and a second transparent electrode formed on the dielectric layer. At least a portion of the second transparent electrode overlaps with the first transparent electrode with the dielectric layer interposed between them. At least one of upper and lower surfaces of the first transparent electrode contacts with a reducing insulating layer which has a property of reducing an oxide semiconductor included in the oxide semiconductor layer. The reducing insulating layer does not contact with a channel region of the oxide semiconductor layer. And the oxide semiconductor layer and the first transparent electrode are formed out of the same

oxide film.

[0013] In one embodiment, the dielectric layer includes the reducing insulating layer and an oxide insulating layer which contacts with the channel region of the oxide semiconductor layer.

[0014] In one embodiment, the gate insulating layer includes the reducing insulating layer and an oxide insulating layer which contacts with a lower surface of the oxide semiconductor layer.

[0015] In one embodiment, the drain electrode is formed on the first transparent electrode, and the first transparent electrode contacts directly with the drain electrode.

[0016] In one embodiment, when viewed along a normal to the substrate, an end portion of the reducing insulating layer overlaps with the drain electrode.

[0017] In one embodiment, the oxide film includes In, Ga and Zn.

[0018] In one embodiment, the oxide semiconductor layer includes an In-Ga-Zn-O based semiconductor.

[0019] A method for fabricating a semiconductor device

according to an embodiment of the present invention includes the steps of: (a) providing a substrate; (b) forming a gate electrode and a gate insulating layer on the substrate; (c) forming an oxide semiconductor film on the gate insulating layer; (d) forming source and drain electrodes on the oxide semiconductor film; (e) forming a dielectric layer over the source and drain electrodes; and (f) forming, either before or after the step (c), a reducing insulating layer which contacts with a portion of the oxide semiconductor film and which has a property of reducing an oxide semiconductor included in the oxide semiconductor film, thereby turning a portion of the oxide semiconductor film which contacts with the reducing insulating layer into a first transparent electrode and also turning the rest of the oxide semiconductor film which has not been reduced into an oxide semiconductor layer; and (g) forming a second transparent electrode on the dielectric layer, at least a portion of the second transparent electrode overlapping with the first transparent electrode with the dielectric layer interposed between them.

[0020] In one embodiment, the step (f) is included in the

step (b).

[0021] In one embodiment, the step (f) is included in the step (e).

[0022] In one embodiment, at least one of the dielectric layer and the gate insulating layer includes an oxide insulating layer, and the oxide insulating layer contacts with the oxide semiconductor layer.

[0023] In one embodiment, when viewed along a normal to the substrate, an end portion of the reducing insulating layer overlaps with the drain electrode.

[0024] In one embodiment, the oxide semiconductor film includes an In-Ga-Zn-O based semiconductor.

ADVANTAGEOUS EFFECTS OF INVENTION

[0025] An embodiment of the present invention provides a TFT substrate which can be fabricated by a simpler process and which can contribute to realizing a display device with higher definition and a higher aperture ratio than conventional ones and also provides a method for fabricating such a TFT substrate.

BRIEF DESCRIPTION OF DRAWINGS

[0026]

[FIG. 1] (a) is a schematic plan view illustrating a TFT substrate 100A according to an embodiment of the present invention. (b) is a schematic cross-sectional view of the TFT substrate 100A as viewed on the plane A1-A1' shown in (a). And (c) is a schematic cross-sectional view of a liquid crystal display device 500 including the TFT substrate 100A.

[FIG. 2] (a) is a graph showing a gate voltage (V_g) - drain current (I_d) curve of an oxide semiconductor TFT in which an oxide insulating layer contacts directly with an oxide semiconductor layer). (b) is a graph showing a gate voltage (V_g) - drain current (I_d) curve of an oxide semiconductor TFT in which a reducing insulating layer 8a contacts directly with the oxide semiconductor layer.

[FIG. 3] (a) is a schematic plan view illustrating a TFT substrate 100A' as a modified example. (b) is a schematic cross-sectional view of the TFT substrate 100A' as viewed on the plane A2-A2' shown in (a).

[FIG. 4] (a) through (e) are schematic cross-sectional views illustrating an exemplary manufacturing process for fabricating a TFT substrate 100A according to an embodiment of the present invention.

[FIG. 5] A schematic cross-sectional view of a TFT substrate 100B according to another embodiment of the present invention.

[FIG. 6] (a) and (b) are schematic cross-sectional views illustrating respective manufacturing process steps to fabricate the TFT substrate 100B according to the embodiment of the present invention.

[FIG. 7] A schematic cross-sectional view of a TFT substrate 100C according to still another embodiment of the present invention.

[FIG. 8] A schematic cross-sectional view illustrating a manufacturing process step to fabricate the TFT substrate 100C according to the embodiment of the present invention.

[FIG. 9] A schematic cross-sectional view of a TFT substrate 100D according to yet another embodiment of the present invention.

DESCRIPTION OF EMBODIMENTS

[0027] Hereinafter, a semiconductor device according to an embodiment of the present invention will be described with reference to the accompanying drawings. A semiconductor device according to this embodiment includes a thin-film transistor which has an active layer made of an oxide semiconductor (and which will be referred to herein as an "oxide semiconductor TFT"). A semiconductor device according to this embodiment just needs to include an oxide semiconductor TFT and may be implemented broadly as an active-matrix substrate or any of various kinds of display devices and electronic devices.

[0028] In the following description, a semiconductor device according to an embodiment of the present invention will be described as being applied to an oxide semiconductor TFT for use in a liquid crystal display device.

[0029] FIG. 1(a) is a schematic plan view illustrating a TFT substrate 100A according to this embodiment. FIG. 1(b) is a schematic cross-sectional view of the semiconductor device

(TFT substrate) 100A as viewed on the plane A1-A1' shown in FIG. 1(a). And FIG. 1(c) is a schematic cross-sectional view of a liquid crystal display device 500 including the TFT substrate 100A. In FIG. 1(c), the dotted arrows indicate the directions of an electric field.

[0030] This TFT substrate 100A includes: a substrate 2; a gate electrode 3 which has been formed on the substrate 2; a gate insulating layer 4 which has been formed over the gate electrode 3; an oxide semiconductor layer 5 which has been formed on the gate insulating layer 4; an oxide insulating layer which contacts with the channel region of the oxide semiconductor layer 5; source and drain electrodes 6s, 6d which are electrically connected to the oxide semiconductor layer 5; a first transparent electrode 7 which is electrically connected to the drain electrode 6d; a dielectric layer 8 which has been formed over the source and drain electrodes 6s, 6d; and a second transparent electrode 9 which has been formed on the dielectric layer 8. At least a portion of the second transparent electrode 9 overlaps with the first transparent electrode 7 with the dielectric layer 8 interposed between

them. At least one of the upper and lower surfaces of the first transparent electrode 7 contacts with a reducing insulating layer 8a with the property of reducing an oxide semiconductor included in the oxide semiconductor layer 5. The oxide semiconductor layer 5 and the first transparent electrode 7 are formed out of the same oxide film. And the reducing insulating layer 8a does not contact with a channel region of the oxide semiconductor layer 5.

[0031] In this TFT substrate 100A, at least a portion of the second transparent electrode 9 overlaps with the first transparent electrode 7 with the dielectric layer 8 interposed between them, thereby forming a storage capacitor there. That is why the storage capacitor this TFT substrate 100A has is transparent (i.e., transmits visible light), and therefore, does not decrease the aperture ratio. Consequently, this TFT substrate 100A can have a higher aperture ratio than a TFT substrate, of which the storage capacitor includes a non-transparent electrode that has been formed out of a metal film (i.e., either a gate metal layer or a source metal layer) as in a conventional structure. In addition, since the aperture

ratio is not decreased by the storage capacitor, the capacitance value of the storage capacitor (i.e., the area of the storage capacitor) can be increased as needed, which is also beneficial.

[0032] Furthermore, it is preferred that the drain electrode 6d be formed on, and contact directly with, the first transparent electrode 7. By adopting such a structure, the first transparent electrode 7 can be extended to reach approximately an end portion of the drain electrode 6d. As a result, this TFT substrate 100A can have a higher aperture ratio than the TFT substrate disclosed in Patent Document No. 1.

[0033] In this TFT substrate 100A, the dielectric layer 8 includes a reducing insulating layer 8a and an insulating protective layer 8b. The reducing insulating layer 8a has been formed over the first transparent electrode 7, and the insulating protective layer 8b has been formed over the reducing insulating layer 8a.

[0034] Hereinafter, the respective components of this TFT substrate 100A will be described in detail one by one.

[0035] The substrate 2 is typically a transparent substrate and may be a glass substrate, for example, but may also be a plastic substrate. Examples of the plastic substrates include a substrate made of either a thermosetting resin or a thermoplastic resin and a composite substrate made of these resins and an inorganic fiber (such as glass fiber or a non-woven fabric of glass fiber). A resin material with thermal resistance may be polyethylene terephthalate (PET), polyethylene naphthalate (PEN), polyether sulfone (PES), an acrylic resin, or a polyimide resin, for example. Also, when used in a reflective liquid crystal display device, the substrate 2 may also be a silicon substrate.

[0036] The gate electrode 3 is electrically connected to a gate line 3'. The gate electrode 3 and the gate line 3' may have a multilayer structure, of which the upper layer is a W (tungsten) layer and the lower layer is a TaN (tantalum nitride) layer, for example. Alternatively, the gate electrode 3 and the gate line 3' may also have a multilayer structure consisting of Mo (molybdenum), Al (aluminum) and Mo layers or may even have a single-layer structure, a double

layer structure, or a multilayer structure consisting of four or more layers. Still alternatively, the gate electrode 3a may be made of an element selected from the group consisting of Cu (copper), Al, Cr (chromium), Ta (tantalum), Ti (titanium), Mo and W or an alloy or metal nitride which is comprised mostly of any of these elements. The gate electrode 3 may have a thickness of approximately 420 nm, for example. The thickness of the gate electrode 3 suitably falls within the range of about 50 nm to about 600 nm, for example.

[0037] The gate insulating layer 4 includes a lower gate insulating layer 4a and an upper gate insulating layer 4b. The upper gate insulating layer 4b that contacts with the oxide semiconductor layer 5 suitably includes an oxide insulating layer. If the oxide insulating layer directly contacts with the oxide semiconductor layer 5, oxygen included in the oxide insulating layer will be supplied to the oxide semiconductor layer 5, thus preventing oxygen deficiencies of the oxide semiconductor layer 5 from deteriorating the properties of the semiconductor. The upper gate insulating layer 4b may be an SiO₂ (silicon dioxide)

layer, for example. The lower gate insulating layer 4a may be an SiN_x (silicon nitride) layer, for example. In this embodiment, the lower gate insulating layer 4a may have a thickness of approximately 325 nm, the upper gate insulating layer 4b may have a thickness of approximately 50 nm, and the gate insulating layer 4 may have an overall thickness of approximately 375 nm, for example. Alternatively, the gate insulating layer 4 may also be a single layer or a multilayer structure of SiO_2 (silicon dioxide), SiN_x (silicon nitride), SiO_xN_y (silicon oxynitride, where $x > y$), SiN_xO_y (silicon nitride oxide, where $x > y$), Al_2O_3 (aluminum oxide), or tantalum oxide (Ta_2O_5). The thickness of the gate insulating layer 4 suitably falls within the range of about 50 nm to about 600 nm. To prevent impurities from diffusing from the substrate 2, the lower gate insulating layer 4a is suitably made of SiN_x or SiN_xO_y (silicon oxynitride, where $x > y$). Moreover, to prevent the semiconductor properties of the oxide semiconductor layer 5 from deteriorating, the upper gate insulating layer 4b is suitably made of either SiO_2 or SiO_xN_y (silicon nitride oxide, where $x > y$). Furthermore, to form a

dense gate insulating layer 4 which causes little gate leakage current at low temperatures, the gate insulating layer 4 is suitably formed using a rare gas of Ar (argon), for example.

[0038] The oxide semiconductor layer 5 may include an In-Ga-Zn-O based semiconductor (which will be referred to herein as an "IGZO based semiconductor"), for example. In this case, the IGZO based semiconductor is a ternary oxide of In (indium), Ga (gallium) and Zn (zinc). The ratios (i.e., mole fractions) of In, Ga and Zn are not particularly limited. For example, In: Ga: Zn = 2: 2: 1, In: Ga: Zn = 1: 1: 1 or In: Ga: Zn = 1: 1: 2 may be satisfied. The IGZO based semiconductor may be either amorphous or crystalline. If the IGZO based semiconductor is a crystalline one, a crystalline IGZO based semiconductor of which the c axis is substantially perpendicular to the layer plane is suitably used. The crystal structure of such an IGZO based semiconductor is disclosed, for example, in Japanese Laid-Open Patent Publication No. 2012-134475, the entire disclosure of which is hereby incorporated by reference.

[0039] The oxide semiconductor material that makes the

oxide semiconductor layer 5 does not have to be an IGZO based semiconductor, but may also be a Zn-O based semiconductor (ZnO), an In-Zn-O based semiconductor (IZO™), a Zn-Ti-O based semiconductor (ZTO), a Cd-Ge-O based semiconductor, a Cd-Pb-O based semiconductor, CdO (cadmium oxide), an Mg-Zn-O based semiconductor, an In-Sn-Zn-O based semiconductor (such as In₂O₃-SnO₂-ZnO) or an In-Ga-Sn-O based semiconductor, for example. Furthermore, the oxide semiconductor layer 5 may also be ZnO in an amorphous state, a polycrystalline state, or a microcrystalline state (which is a mixture of amorphous and polycrystalline states) to which one or multiple dopant elements selected from the group consisting of Group I, Group XIII, Group XIV, Group XV and Group XVII elements have been added, or may even be ZnO to which no dopant elements have been added at all. If an amorphous oxide semiconductor layer is used as the oxide semiconductor layer 5, the semiconductor device can be fabricated at a low temperature and can achieve high mobility. The oxide semiconductor layer 5 may have a thickness of approximately 50 nm, for example. The thickness of the oxide semiconductor layer 5 suitably falls within the

range of about 30 nm to about 100 nm, for example.

[0040] The source and drain electrodes 6s and 6d may have a multilayer structure comprised of Ti, Al and Ti layers, for example. Alternatively, the source and drain electrodes 6s and 6d may also have a multilayer structure comprised of Mo, Al and Mo layers or may even have a single-layer structure, a double layer structure or a multilayer structure consisting of four or more layers. Furthermore, the source and drain electrodes 6s and 6d may also be made of an element selected from the group consisting of Al, Cr, Ta, Ti, Mo and W, or an alloy or metal nitride comprised mostly of any of these elements. The source and drain electrodes 6s and 6d may have a thickness of approximately 350 nm, for example. The thicknesses of the source and drain electrodes 6s and 6d suitably fall within the range of about 50 nm to about 600 nm.

[0041] The dielectric layer 8 includes an insulating protective layer 8b, and is arranged between the first and second transparent electrodes 7 and 9 to form a storage capacitor there. If a storage capacitor is formed of those transparent electrodes 7 and 9 and the transparent dielectric

layer 8 in this manner, a display panel with a high aperture ratio can be fabricated when this TFT substrate 100A is used to make a display panel.

[0042] Next, the reducing insulating layer 8a will be described with reference to FIG. 2. When in contact with an oxide semiconductor layer, the reducing insulating layer 8a has the function of lowering its electrical resistance. FIG. 2(a) is a graph showing a gate voltage (V_g) - drain current (I_d) curve of an oxide semiconductor TFT having a configuration in which an oxide insulating layer (of SiO_2 , for example) has been formed so as to contact with the entire lower surface of an oxide semiconductor layer (active layer). On the other hand, FIG. 2(b) is a graph showing a gate voltage (V_g) - drain current (I_d) curve of an oxide semiconductor TFT having a configuration in which a reducing insulating layer (of SiN_x , for example) has been formed so as to contact with the entire lower surface of an oxide semiconductor layer (active layer).

[0043] As can be seen from FIG. 2(a), an oxide semiconductor TFT in which an oxide insulating layer contacts

directly with an oxide semiconductor layer has a good TFT characteristic.

[0044] On the other hand, as can be seen from FIG. 2(b), an oxide semiconductor TFT in which a reducing insulating layer contacts directly with an oxide semiconductor layer does not have a TFT characteristic, and the oxide semiconductor layer is turned into a conductor by the reducing insulating layer.

[0045] As can be seen from the foregoing description, if the reducing insulating layer 8a contacts with the oxide semiconductor layer, the electrical resistance of the oxide semiconductor layer decreases. This is probably because the reducing insulating layer 8a will include a lot of hydrogen and will reduce the oxide semiconductor layer 5 by contacting with the oxide semiconductor layer 5, thus lowering the resistance of the oxide semiconductor film. That is why if such a reducing insulating layer 8a is formed to directly contact with the oxide semiconductor layer 5, the resistance of the oxide semiconductor layer 5 can be lowered even without performing any special resistance lowering process (such as a

hydrogen plasma treatment). In the manufacturing process of the TFT substrate 100A of this embodiment, if the reducing insulating layer 8a is arranged to contact with a portion of the oxide semiconductor film, an electrode can be formed with the resistance of the oxide semiconductor film lowered partially. On the other hand, the rest of the oxide semiconductor film, of which the resistance has not been lowered, can be used as an active layer for TFTs. Consequently, the manufacturing process can be simplified and the manufacturing cost can be cut down.

[0046] The reducing insulating layer 8a may be made of SiN_x , for example. The reducing insulating layer 8a may be deposited at a substrate temperature of about 100 °C to about 250 °C (e.g., at 220 °C) and with the flow rates adjusted so that the SiH_4 - NH_3 mixed gas flow rate (in sscm) ratio (i.e., the ratio of the SiH_4 flow rate to the NH_3 flow rate) falls within the range of 4 to 20. The reducing insulating layer 8a may have a thickness of about 100 nm, for example. The thickness of the reducing insulating layer 8a suitably falls within the range of about 50 nm to about 300 nm.

[0047] The insulating protective layer 8b has been formed to contact with the channel region of the oxide semiconductor layer 5. The insulating protective layer 8b is suitably made of an insulating oxide (such as SiO₂). If the insulating protective layer 8b is made of an insulating oxide, it is possible to prevent the oxygen deficiencies of the oxide semiconductor layer 5 from deteriorating the semiconductor properties as described above. Alternatively, the insulating protective layer 8b may also be made of SiON (which may be either silicon oxynitride or silicon nitride oxide), Al₂O₃ or Ta₂O₅, for example. The insulating protective layer 8b may have a thickness of about 265 nm. The thickness of the insulating protective layer 8b suitably falls within the range of about 50 nm to about 300 nm, for example.

[0048] The first transparent electrode 7 may be a conductive layer including an In-Ga-Zn-O based oxide (which will be referred to herein as an "IGZO based oxide"), for example. The first transparent electrode 7 may have a thickness of about 50 nm, for example. The thickness of the first transparent electrode 7 suitably falls within the range

of about 20 nm to about 200 nm, for example. As will be described in detail later, the first transparent electrode 7 and the oxide semiconductor layer 5 are formed out of the same transparent oxide film. If the first transparent electrode 7 and the oxide semiconductor layer 5 are formed out of the same oxide film, the manufacturing process can be simplified and the manufacturing cost can be cut down. As the oxide film, a film including an IGZO based oxide such as an IGZO based semiconductor film may be used, for example. As mentioned above, in this description, an IGZO based oxide with semiconductor properties will be referred to herein as an "IGZO based semiconductor".

[0049] The second transparent electrode 9 is formed out of a transparent conductive film (of ITO (indium tin oxide) or IZO, for example). The second transparent electrode 9 may have a thickness of about 100 nm, for example. The thickness of the second transparent electrode 9 suitably falls within the range of about 20 nm to about 200 nm, for example.

[0050] As shown in FIG. 1(c), the TFT substrate 100A may be used in a fringe field switching (FFS) mode liquid crystal

display device 500, for example. In this case, the first transparent electrode 7 that forms the lower layer is used as a pixel electrode (to which a display signal voltage is applied) and the second transparent electrode 9 that forms the upper layer is used as a common electrode (to which either a common voltage or a counter voltage is applied). At least one slit is cut through the second transparent electrode 9. An FFS mode liquid crystal display device 500 with such a configuration is disclosed in Japanese Laid-Open Patent Publication No. 2011-53443, for example, the entire disclosure of which is hereby incorporated by reference.

[0051] This liquid crystal display device 500 includes a TFT substrate 100A, a counter substrate 200, and a liquid crystal layer 50 interposed between the TFT substrate 100A and the counter substrate 200. In this liquid crystal display device 500, no counter electrode such as a transparent electrode of ITO, for example, is arranged on the surface of the counter substrate 200 to face the liquid crystal layer 50. Instead, a display operation is carried out by controlling the alignments of liquid crystal molecules

in the liquid crystal layer 50 with a lateral electric field which has been generated by the first and second transparent electrodes (i.e., the pixel electrode and the common electrode) 7 and 9 that have been formed on the TFT substrate 100A.

[0052] The TFT substrate 100A may be modified into the TFT substrate 100A' shown in FIG. 3. FIG. 3(a) is a schematic plan view illustrating a TFT substrate 100A' as a modified example. FIG. 3(b) is a schematic cross-sectional view of the TFT substrate 100A' as viewed on the plane A2-A2' shown in FIG. 3(a).

[0053] The TFT substrate 100A' shown in FIGS. 3(a) and 3(b) includes an oxide semiconductor layer 5 which overlaps with a gate line 3' and has a structure in which when viewed along a normal to the substrate 2, the gate line 3' and the source and drain electrodes 6s, 6d overlap with each other, which is a difference from the TFT substrate 100A. In this TFT substrate 100A', the gate line 3' functions as a gate electrode 3. The TFT substrate 100A' can have an even higher aperture ratio than the TFT substrate 100A.

[0054] However, this TFT substrate 100A' has a higher gate-drain parasitic capacitance (C_{gd}) than the TFT substrate 100A, which is one of drawbacks of the TFT substrate 100A'. As is well known, if the gate-drain parasitic capacitance (C_{gd}) is large, then the feedthrough voltage rises. The feedthrough voltage would cause an image persistence phenomenon or flickers. To lower the feedthrough voltage, the ratio of the gate-drain parasitic capacitance (C_{gd}) to the overall capacitance of the pixel (i.e., liquid crystal capacitance C_{lc} + storage capacitance C_s + gate-drain parasitic capacitance C_{gd}) needs to be decreased. This TFT substrate 100A' has a transparent storage capacitor with a transparent electrode, and therefore, can have its capacitance value increased by increasing the area of the storage capacitor without causing a decrease in aperture ratio. That is to say, even by adopting such a structure in which the gate-drain parasitic capacitance (C_{gd}) becomes as high as in this TFT substrate 100A', the feedthrough voltage can be reduced sufficiently.

[0055] Moreover, if a pixel's overall capacitance is

large, it means that a lot of electric charges are needed to apply a predetermined voltage to the pixel. This TFT substrate 100A' includes oxide semiconductor TFTs which have higher current supplying ability than conventional amorphous silicon TFTs. That is why the display quality will never be debased by an increase in the pixel's capacitance.

[0056] Next, it will be described how to fabricate the TFT substrate 100A.

[0057] A method for fabricating a semiconductor device 100A according to an embodiment of the present invention includes the steps of: (a) providing a substrate 2; (b) forming a gate electrode 3 and a gate insulating layer 4 on the substrate 2; (c) forming an oxide semiconductor film 5' on the gate insulating layer 4; (d) forming source and drain electrodes 6s, 6d on the oxide semiconductor film 5'; (e) forming a dielectric layer 8 over the source and drain electrodes 6s, 6d; (f) forming, either before or after the step (c), a reducing insulating layer 8a which contacts with a portion of the oxide semiconductor film 5' and which has the property of reducing an oxide semiconductor included in the

oxide semiconductor film 5', thereby turning a portion of the oxide semiconductor film 5' which contacts with the reducing insulating layer 8a into a first transparent electrode 7 and also turning the rest of the oxide semiconductor film which has not been reduced into an oxide semiconductor layer 5; and (g) forming a second transparent electrode 9 on the dielectric layer 8, at least a portion of the second transparent electrode 9 overlapping with the first transparent electrode 7 with the dielectric layer 8 interposed between them.

[0058] Such a method for fabricating a semiconductor device is a simplified one, and therefore, can contribute to cutting down the manufacturing cost.

[0059] Hereinafter, an exemplary method for fabricating the TFT substrate 100A will be described in detail with reference to FIG. 4.

[0060] FIGS. 4(a) through 4(e) are schematic cross-sectional views illustrating an exemplary method for fabricating the TFT substrate 100A.

[0061] First of all, as shown in FIG. 4(a), a gate electrode 3 is formed on a substrate 2. As the substrate 2, a

transparent insulating substrate such as a glass substrate, for example, may be used. The gate electrode 3 may be formed by depositing a conductive film on the substrate 2 by sputtering process and then patterning the conductive film by photolithographic process. In this example, a multilayer film with a double layer structure consisting of a TaN film (with a thickness of about 50 nm) and a W film (with a thickness of about 370 nm) that have been stacked one upon the other in this order on the substrate 2 is used as the conductive film. As this first conductive film, a single-layer film of Ti, Mo, Ta, W, Cu, Al or Cr, a multilayer film or alloy film including any of these elements in combination, or a metal nitride film thereof may be used.

[0062] Next, as shown in FIG. 4(b), a lower gate insulating layer 4a and an upper gate insulating layer 4b are formed by CVD (chemical vapor deposition) process to cover the gate electrode 3. In this example, the lower gate insulating layer 4a is formed out of an SiN_x film (with a thickness of about 325 nm) and the upper gate insulating layer 4b is formed out of an SiO₂ film (with a thickness of about 50 nm). The upper

gate insulating layer 4b may be made of SiO_2 , SiO_xN_y (silicon oxynitride, where $x > y$), SiN_xO_y (silicon nitride oxide, where $x > y$), Al_2O_3 , or Ta_2O_5 , for example. The lower gate insulating layer 4a may be made of SiN_x , SiO_2 , SiO_xN_y (silicon oxynitride, where $x > y$), SiN_xO_y (silicon nitride oxide, where $x > y$), Al_2O_3 , or Ta_2O_5 , for example.

[0063] Subsequently, as shown in FIG. 4(c), an oxide semiconductor film 5' is formed by sputtering process on the upper gate insulating layer 4b. As the oxide semiconductor film 5', an IGZO based semiconductor film may be used, for example. The oxide semiconductor film 5' may have a thickness of about 50 nm.

[0064] Thereafter, a conductive film (not shown) to be source and drain electrodes 6s and 6d is formed by sputtering process over the oxide semiconductor film 5'. Next, the conductive film and the oxide semiconductor film 5' are patterned simultaneously by photolithographic process using a half-tone mask, dry etching process and ashing process, thereby turning the oxide semiconductor film 5' into an intended shape and forming source and drain electrodes 6s and

6d. Since the source and drain electrodes 6s and 6d can be formed and the oxide semiconductor film 5' can be patterned in this manner using a single photomask, the manufacturing process can be simplified and the manufacturing cost can be cut down. The source and drain electrodes 6s and 6d may have a multilayer structure consisting of Ti, Al and Ti layers, for example. The lower Ti layer may have a thickness of about 50 nm, the Al layer may have a thickness of about 200 nm, and the upper Ti layer may have a thickness of about 100 nm.

[0065] Subsequently, as shown in FIG. 4(d), a reducing insulating layer 8a is formed by CVD and photolithographic processes so as not to cover the channel region of the oxide semiconductor film 5'. In this embodiment, the reducing insulating layer 8a is deposited under the condition including a substrate temperature of about 100 °C to about 250 °C (e.g., about 220 °C) and an SiH₄/NH₃ mixed gas flow rate ratio (i.e., the ratio of the SiH₄ flow rate to the NH₃ flow rate) of 4 to 20. When viewed along a normal to the substrate 2, an end portion of the reducing insulating layer 8a may overlap with the drain electrode 6d. If the reducing insulating layer 8a

is formed in this manner, the first transparent electrode 7 (to be described later) can be formed to reach the vicinity of the end portion of the drain electrode 6d which is located opposite from the channel region. As a result, the aperture ratio of the pixel can be increased. The reducing insulating layer 8a may be made of SiN_x and may have a thickness of about 100 nm.

[0066] A portion of the oxide semiconductor film 5' which contacts with the reducing insulating layer 8a is reduced by hydrogen, for example, included in the reducing insulating layer 8a, thereby forming a first transparent electrode 7. In addition, another portion of the oxide semiconductor film 5' which is located under the drain electrode 6d may also have its resistance lowered by that hydrogen diffusing and may form part of the first transparent electrode 7, too. Meanwhile, the rest of the oxide semiconductor film 5' which has not had its resistance lowered turns into an oxide semiconductor layer 5.

[0067] Next, as shown in FIG. 4(e), an insulating protective layer 8b is deposited by CVD process over the first

transparent electrode 7 so as to contact with the channel region of the oxide semiconductor layer 5. In this embodiment, the reducing insulating layer 8a and the insulating protective layer 8b together form a dielectric layer 8. The insulating protective layer 8b may be made of SiO_2 , for example. The insulating protective layer 8b may have a thickness of about 265 nm. A contact hole (not shown) has been cut through the insulating protective layer 8b by a known method. Optionally, after the insulating protective layer 8b has been formed, a heat treatment (annealing process) may be carried out at a temperature (of about 300 °C, for example) that is equal to or higher than the deposition temperature at which the insulating protective layer 8b has been deposited. By conducting the heat treatment, hydrogen included in the reducing insulating layer 8a can be diffused through the oxide semiconductor film 5' and the electrical resistance of the first transparent electrode 7 can be further lowered.

[0068] Subsequently, as shown in FIG. 1(b), a transparent conductive film is deposited by sputtering process, for

example, over the insulating protective layer 8b and then patterned, thereby forming a second transparent electrode 9. At least a portion of the second transparent electrode 9 overlaps with the first transparent electrode 7 with the dielectric layer 8 interposed between them. The second transparent electrode 9 may be made of ITO, for example, and may have a thickness of about 100 nm.

[0069] Although not shown, the transparent conductive film to be patterned into this second transparent electrode 9 may be used as not only a common electrode but also an extended line to be electrically connected to a source metal layer that has been formed out of the same conductive film as a source line (source bus line) or a gate metal layer that has been formed out of the same conductive film as a gate line (gate bus line). As a result, a TFT substrate including an integrated driver can be formed and a display device of high quality can be fabricated.

[0070] Hereinafter, a TFT substrate 100B according to another embodiment of the present invention will be described with reference to FIG. 5, which is a schematic cross-sectional

view of the TFT substrate 100B and which corresponds to the cross-sectional view of the TFT substrate 100A shown in FIG. 1(b). In FIG. 5, any component also included in the TFT substrate 100A and having substantially the same function as its counterpart is identified by the same reference numeral and its description will be omitted herein to avoid redundancies.

[0071] In the TFT substrate 100B shown in FIG. 5, the reducing insulating layer 8a of the TFT substrate 100A has not been formed over the first transparent electrode 7 and the first transparent electrode 7 contacts with the lower gate insulating layer 4a. In this TFT substrate 100B, instead of forming the reducing insulating layer 8a over the first transparent electrode 7, the lower gate insulating layer 4a which is located under the first transparent electrode 7 is made to function as the reducing insulating layer 8a and the lower gate insulating layer 4a is brought into contact with the first transparent electrode 7. That is why the lower gate insulating layer 4a is made of the material of the reducing insulating layer 8a and the oxide semiconductor layer 5 does

not contact with the lower gate insulating layer 4a. In this TFT substrate 100B, the dielectric layer 8 includes an insulating protective layer 8b but does not include the reducing insulating layer 8a.

[0072] Hereinafter, an exemplary method for fabricating this TFT substrate 100B will be described with reference to FIG. 6. Specifically, FIGS. 6(a) and 6(b) are schematic cross-sectional views illustrating respective manufacturing process steps to fabricate the TFT substrate 100B.

[0073] As shown in FIG. 6(a), a gate electrode 3, a lower gate insulating layer 4a and an upper gate insulating layer 4b are formed by known methods on a substrate 2. In this process step, the lower gate insulating layer 4a is made of the material of the reducing insulating layer 8a described above. Also, the upper gate insulating layer 4b is patterned to expose the lower gate insulating layer 4b partially.

[0074] Next, an oxide semiconductor film 5' is formed over the upper and lower gate insulating layers 4a, 4b and source and drain electrodes 6s and 6d are formed on the oxide semiconductor film 5' by the methods described above.

[0075] As shown in FIG. 6(b), a portion of the oxide semiconductor film 5' which contacts with the lower gate insulating layer 4a has its resistance lowered through the reduction reaction described above to turn into the first transparent electrode 7. On the other hand, the rest of the oxide semiconductor film which has not had its resistance lowered turns into an oxide semiconductor layer 5. The oxide semiconductor layer 5 is formed so as to contact with the upper gate insulating layer 4b.

[0076] Subsequently, an insulating protective layer 8b is formed on the first transparent electrode 7 by the method described above so as to contact with the channel region of the oxide semiconductor layer 5, thereby forming a dielectric layer 8. Thereafter, a first transparent electrode 9 is formed on the insulating protective layer 8b to complete the TFT substrate 100B shown in FIG. 5.

[0077] Hereinafter, a TFT substrate 100C according to still another embodiment of the present invention will be described with reference to FIG. 7, which is a schematic cross-sectional view of the TFT substrate 100C and which

corresponds to FIG. 1(b). In FIG. 7, any component also included in the TFT substrate 100A and having substantially the same function as its counterpart is identified by the same reference numeral and its description will be omitted herein to avoid redundancies.

[0078] In the TFT substrate 100C shown in FIG. 7, a reducing insulating layer 8a has been formed on the first transparent electrode 7 of the TFT substrate 100B. Thus, in this TFT substrate 100C, the first transparent electrode 7 contacts with the reducing insulating layer 8a and the lower gate insulating layer 4a which is made of the material of the reducing insulating layer 8a. In this TFT substrate 100C, the dielectric layer 8 includes the reducing insulating layer 8a and an insulating protective layer 8b. Also, in this TFT substrate 100C, the lower gate insulating layer 4a is made of the material of the reducing insulating layer 8a.

[0079] Hereinafter, an exemplary method for fabricating this TFT substrate 100C will be described with reference to FIG. 8, which is a schematic cross-sectional view illustrating a manufacturing process step to fabricate the TFT substrate

100C.

[0080] A gate electrode 3, a lower gate insulating layer 4a, an upper gate insulating layer 4b, an oxide semiconductor film 5' and source and drain electrodes 6s, 6d are formed as described above on a substrate 2 (see FIGS. 6(a) and 6(b)).

[0081] Subsequently, as shown in FIG. 8, a reducing insulating layer 4a is formed on the oxide semiconductor film 5' by the method described above. The reducing insulating layer 4a is formed so as not to contact with the channel region of the oxide semiconductor film 5'. Also, when viewed along a normal to the substrate 2, an end portion of the reducing insulating layer 4a preferably overlaps with the drain electrode 6d.

[0082] A portion of the oxide semiconductor film 5' which contacts with either the lower gate insulating layer 4a or the reducing insulating layer 4a has its resistance lowered to turn into the first transparent electrode 7. On the other hand, the rest of the oxide semiconductor film 5' which has not had its resistance lowered turns into an oxide semiconductor layer 5.

[0083] Subsequently, an insulating protective layer 8b is formed on the reducing insulating layer 8a so as to contact with the channel region of the oxide semiconductor layer 5 and a second transparent electrode 9 is formed on the insulating protective layer 8b as described above to complete the TFT substrate 100C shown in FIG. 7.

[0084] Hereinafter, a TFT substrate 100D according to yet another embodiment of the present invention will be described with reference to FIG. 9, which is a schematic cross-sectional view of the TFT substrate 100D and which corresponds to FIG. 1(b). In FIG. 9, any component also included in the TFT substrate 100A and having substantially the same function as its counterpart is identified by the same reference numeral and its description will be omitted herein to avoid redundancies.

[0085] The TFT substrate 100D shown in FIG. 9 includes a gate electrode 3 on a substrate 2, a gate insulating layer 4 which has been formed on the gate electrode 3, a reducing insulating layer 8a and an oxide semiconductor layer 5 which have been formed over the gate insulating layer 4, source and

drain electrodes 6s, 6d which have been formed on the oxide semiconductor layer 5, a dielectric layer 8 which has been formed over the source and drain electrodes 6s, 6d, and a second transparent electrode 9 which has been formed on the dielectric layer 8.

[0086] In this TFT substrate 100D, the reducing insulating layer 8a has been formed under the first transparent electrode 7. The reducing insulating layer 8a contacts with the first transparent electrode 7 but does not contact with the oxide semiconductor layer 5. The gate insulating layer 4 is made of the material of the upper gate insulating layer 4b described above. The dielectric layer 8 includes the insulating protective layer 8b described above but does not include the reducing insulating layer 8a. In this example, the dielectric layer 8 may include the reducing insulating layer 8a. The gate insulating layer 4 and the insulating protective layer 8b contact with the oxide semiconductor layer 5.

[0087] As can be seen from the foregoing description, embodiments of the present invention provide a semiconductor

device which can contribute to fabricating a display panel of high display quality with the manufacturing cost cut down and also provide a method for fabricating such a semiconductor device.

INDUSTRIAL APPLICABILITY

[0088] The present invention is applicable broadly to various types of devices that use a thin-film transistor. Examples of such devices include circuit boards such as an active-matrix substrate, display devices such as a liquid crystal display, an organic electroluminescence (EL) display, and an inorganic electroluminescence display, image capture devices such as an image sensor, and electronic devices such as an image input device and a fingerprint scanner.

REFERENCE SIGNS LIST

[0089]

- 2 substrate
- 3 gate electrode
- 4 gate insulating layer

4a	lower gate insulating layer
4b	upper gate insulating layer
5	oxide semiconductor layer
6s	source electrode
6d	drain electrode
7	first transparent electrode
8	dielectric layer
8a	reducing insulating layer
8b	insulating protective layer
9	second transparent electrode
50	liquid crystal layer
100A	semiconductor device (TFT substrate)
200	counter substrate
500	liquid crystal display device

CLAIMS

1. A semiconductor device comprising:

- a substrate;
- a gate electrode formed on the substrate;
- a gate insulating layer formed over the gate electrode;
- an oxide semiconductor layer formed on the gate insulating layer;
- source and drain electrodes electrically connected to the oxide semiconductor layer;
- a first transparent electrode electrically connected to the drain electrode;
- a dielectric layer formed over the source and drain electrodes; and
- a second transparent electrode formed on the dielectric layer,

wherein at least a portion of the second transparent electrode overlaps with the first transparent electrode with the dielectric layer interposed between them,

at least one of upper and lower surfaces of the first transparent electrode contacts with a reducing insulating

layer which has a property of reducing an oxide semiconductor included in the oxide semiconductor layer,

the reducing insulating layer does not contact with a channel region of the oxide semiconductor layer, and

the oxide semiconductor layer and the first transparent electrode are formed out of the same oxide film.

2. The semiconductor device of claim 1, wherein the dielectric layer includes the reducing insulating layer and an oxide insulating layer which contacts with the channel region of the oxide semiconductor layer.

3. The semiconductor device of claim 1 or 2, wherein the gate insulating layer includes the reducing insulating layer and an oxide insulating layer which contacts with a lower surface of the oxide semiconductor layer.

4. The semiconductor device of one of claims 1 to 3, wherein the drain electrode is formed on the first transparent electrode, and

the first transparent electrode contacts directly with the drain electrode.

5. The semiconductor device of one of claims 1 to 4, wherein when viewed along a normal to the substrate, an end portion of the reducing insulating layer overlaps with the drain electrode.

6. The semiconductor device of one of claims 1 to 5, wherein the oxide film includes In, Ga and Zn.

7. A method for fabricating a semiconductor device, the method comprising the steps of:

- (a) providing a substrate;
- (b) forming a gate electrode and a gate insulating layer on the substrate;
- (c) forming an oxide semiconductor film on the gate insulating layer;
- (d) forming source and drain electrodes on the oxide semiconductor film;

(e) forming a dielectric layer over the source and drain electrodes; and

(f) forming, either before or after the step (c), a reducing insulating layer which contacts with a portion of the oxide semiconductor film and which has a property of reducing an oxide semiconductor included in the oxide semiconductor film, thereby turning a portion of the oxide semiconductor film which contacts with the reducing insulating layer into a first transparent electrode and also turning the rest of the oxide semiconductor film which has not been reduced into an oxide semiconductor layer; and

(g) forming a second transparent electrode on the dielectric layer, at least a portion of the second transparent electrode overlapping with the first transparent electrode with the dielectric layer interposed between them.

8. The method of claim 7, wherein the step (f) is included in the step (b).

9. The method of claim 7 or 8, wherein the step (f) is

included in the step (e).

10. The method of one of claims 7 to 9, wherein at least one of the dielectric layer and the gate insulating layer includes an oxide insulating layer, and

the oxide insulating layer contacts with the oxide semiconductor layer.

11. The method of one of claims 7 to 10, wherein when viewed along a normal to the substrate, an end portion of the reducing insulating layer overlaps with the drain electrode.

12. The semiconductor device of one of claims 1 to 6, wherein the oxide semiconductor layer includes an In-Ga-Zn-O based semiconductor.

13. The method of one of claims 7 to 11, wherein the oxide semiconductor film includes an In-Ga-Zn-O based semiconductor.