

POWER EFFICIENT MEMORY AND CARDS

FIELD

The present invention relates generally to memories and in particular the
5 present invention relates to low power consumption memories.

BACKGROUND

The memory devices used on cards such as flash cards in cameras and for
transportable storage require voltages that are much higher than the supply voltages (V_{cc})
10 available. One such type of memory device today is NAND type flash memory. These types
of memory devices require voltages as high as 20 Volts. The V_{cc} range of operation for
these devices is also dropping with every new generation of device. This is in part because
end systems are lowering power requirements and this is one way they achieve that goal. In
order to supply sufficient voltages for operation of the devices, internal pumps are used to
15 pump the supply voltages up to a suitable operating voltage. However, the internal pumps
used for NAND memory devices are increasingly inefficient. For example, at a supply
voltage of 1.6 Volts (which is typical in current devices), to generate even 5 to 6 volts, the
efficiency of the charge pumps are about 15 per cent (%). For the pump to generate 1 mA, it
must draw on the order of 7 mA from the supply voltage source.

20 NAND devices are meant to be stand alone memory devices that need to operate
from a single power supply, so manufacturers and assemblers have accepted low efficiency to
maintain the standards to which industry expects. Typical pumps used on memory devices
are Dixon pumps. These types of pumps have been around for years, and use capacitors and
diodes to pump a supply voltage to higher voltages than the internal power supply available.
25 There are other types of pumps that use inductors that are much more efficient. Those types
of pumps have efficiencies that approach 80%. Therefore, one can see that such use could
make power efficiency of the cards on which the devices are used much greater. However,
this requires an external inductor which is not a part of the NAND stand-alone memory.

Since the NAND device needs to be stand alone to comply with industry standards
30 and to allow it to be used across multiple platforms and by multiple manufacturers, the
maintenance of standard efficiency pumps and common pin configurations for devices is

desirable. However, on the cards used, there may be other voltages available for the card, other systems of the card, or the memory subsystem.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for flash memories and flash memory cards having lower power consumption.

SUMMARY

The above-mentioned problems with power consumption and inefficiencies and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

In one embodiment, a memory device includes an array of memory cells, control circuitry to read, write and erase the memory cells, address circuitry to latch address signals provided on address input connections, an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device, and a detection mechanism to detect a presence of an external component to supply a voltage for the voltage pump.

In another embodiment, a memory card includes a number of pins for connection of the memory card to a device using the memory card, and a memory device on the memory card. The memory device includes an array of memory cells, control circuitry to read, write and erase the memory cells, address circuitry to latch address signals provided on address input connections, an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device, and a detection mechanism to detect a presence of an external component to supply a voltage for the voltage pump

In yet another embodiment, a memory device includes an array of memory cells, control circuitry to read, write and erase the memory cells, address circuitry to latch address signals provided on address input connections, an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device, and a detection circuit connected to a connect pin of the memory device to detect whether to provide the internal supply voltage to the voltage pump or to use an external component to provide an external supply voltage to the voltage pump.

In still another embodiment, a processing system includes a processor, and a memory coupled to the processor to store data provided by the processor and to provide data

to the processor. The memory includes an array of memory cells, control circuitry to read, write and erase the memory cells, address circuitry to latch address signals provided on address input connections, an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device, and a detection mechanism to detect a presence of an external component to supply a voltage for the voltage pump.

In another embodiment, a method of operating a dual mode memory card includes operating in a normal mode when no external power supply is provided to operate an internal pump of the memory card, and operating in a power efficient mode when an external voltage is provided to operate the internal pump.

In yet another embodiment, a method of operating a memory device includes receiving a command from a memory controller indicating which of a plurality of voltage supplies to use to operate an internal pump of the memory device, and operating the internal pump from the commanded voltage supply.

Other embodiments are described and claimed.

BRIEF DESCRIPTION OF DRAWINGS

Figure 1 is a block diagram of a memory card on which embodiments of the present invention may be practiced;

Figure 2 is a block diagram of a memory card having a power efficient circuit of one embodiment of the present invention;

Figure 3 is a block diagram of a memory card according to another embodiment of the present invention; and

Figure 4 is a block diagram of a memory on which embodiments of the present invention may be practiced.

DETAILED DESCRIPTION

In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the

invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

As is described in further detail below, a dual mode capable memory device or memory card is provided in various embodiments. The memory looks like, and can be operated like and connected like a standard stand-alone memory. However, if the memory is connected so that certain pins that are normally "no connect" pins are connected to a specific signal, voltage, or combination thereof, the memory operates in a second more efficient mode. Generally, the memory device or memory card operates off of a standard internal supply voltage except when a detection mechanism, detection signal, command signal or the like is provided or detected by the memory device or memory card. Upon a receipt of such a signal or upon a determination to use an external voltage or different internal voltage, or an external voltage in combination with an external inductor, the memory device and memory card embodiments of the present invention operate from the other voltage source, inductor, or combination thereof, alone or in conjunction with the standard internal supply voltage source.

In the embodiments of the present invention and the appended claims, a stand-alone memory device is defined as a memory that is configured with a pin out configuration substantially similar to an industry standard pin out configuration, and operates in a traditional operating manner when connected to an industry standard system. Such devices have certain pins that are present in the industry standard system but are not connected to any internal components of the memory. These are typically referred to as "no connect" pins. Such stand-alone memories include by way of example only and not by way of limitation, DRAM and SDRAM memories, flash memories, NAND type flash memories, and the like, that have a standard or substantially standard configuration of pins that connect the device to a system or the like.

One embodiment of a memory card 100 is shown in Figure 1. Memory card 100 has a plurality of pins that are used for connection of the card 100 to a device such as a digital camera, a printer, a cellular telephone, or the like. Memory card 100 has a standard pin out configuration so that it is capable of use with systems that do not have extra power efficiencies. Two pins of the standard pin out configuration, here labeled 102 and 104, are

traditionally "no connect" pins in a standard memory card. In the memory card 100, however, these pins 102 and 104 are connected internally in this embodiment to a detection circuit that detects whether a non-standard voltage is to be used with the card to increase efficiency of the internal voltage pump 106 of the card 100.

For example, if the memory card 100 is used in a cellular telephone memory that runs on 1.6 volts, but also contains a liquid crystal display (LCD) or the like that operates on a higher voltage, such as 3.0 volts, this higher voltage is in various embodiment supplied to the internal pump, which makes the memory or the memory card more efficient. Alternatively, a higher voltage is supplied through one of the two pins 102 or 104, while a signal indicating whether or not to use the external voltage is supplied on the other of the two pins 102 or 104.

In another embodiment shown in Figure 2, a memory card 200 is shown. Memory card 200 is configured with a pin out configuration that works with standard memory cards as well. An additional pin, 202, which is a "no connect" pin in a standard configuration, is used by this embodiment for power efficiency changes to the pump configuration of the memory card 200. In this embodiment, a hardware detection mechanism 206 is used to detect whether the memory card 200 is connected to some external power supply, external inductor, or combination thereof, that can be used for improved pump efficiency, or whether the standard internal pump configuration should be used.

Hardware detection system 206 comprises in one embodiment a pair of transistors 208 and 210 and a pull down resistor 212. The pull down resistor 212 is optional. The hardware detection system 206 is connected to pin 202, which is in turn either connected to an external voltage or not. The pin 202 is connected through resistor 212 to node 214. Node 214 is connected to the gate of n-type transistor 208 and to the gate of p-type transistor 210. If no external voltage device is connected to pin 202, or the pin is floating, then the voltage at node 214, through the resistor 212, will be substantially zero, indicating that no external device is connected to the pin 202. In this situation, the memory card 200 is configured to operate on its internal power supply V_{cc} , since transistor 210 is on and transistor 208 is off, providing supply voltage V_{cc} to pump 216. If pin 202 is connected to an external voltage, then the voltage at node 214 is sufficiently high to turn transistor 210 off and turn transistor 208 on, feeding the voltage at pin 202 to the pump 216.

It should be understood that the hardware detection mechanisms described herein can easily be varied to control which voltage is supplied to the internal pump. It should also be understood that in certain memories or memory cards, more than two possible voltages are selectively connectable to the internal pump, and that in other embodiments, a plurality of potential voltages are detected and the highest or most suitable voltage for operation of the pump is supplied to the pump. Selection of the voltage to be supplied to the pump is made in various embodiments through hardware, firmware, software, or through the use of a command signal provided by the memory controller. The hardware detection mechanism of this embodiment can also detect the presence on another pin of an external inductor, and can reconfigure the operation of the device to use the external inductor alone or in combination with the external voltage, to provide higher efficiencies. In one embodiment, when both an external voltage and an external inductor are detected, the external voltage is used to boost the efficiency of the internal voltage pump, and the external inductor is used with the pumped voltage to even further increase efficiency.

In another embodiment 300 shown in Figure 3, external pin 302 is used as a detection mechanism only, and the pin 304 is tied to either an external voltage or to an inductor. In this embodiment, the card 300 ties the detection pin 302 to a low signal if the internal pump 306 is to be used. There are two external options possible in this embodiment that are tied to pin 304. If one of the two external options is to be used, the card 300 ties pin 302 to a high signal. The memory then know from the high signal at the detection pin 302 that some external form of assistance is to be used. Then, a voltage detection mechanism can be used to determine which type of assistance device is tied to the pin 304.

If the voltage detection mechanism detects a high, it concludes that a power supply is connected to the pin, and uses that pin as the new supply for the pump making the pump more efficient and improving power performance of the card. If there is simply an inductor hanging off the pin, there is no voltage to detect and the memory concludes that there is an inductor on the pin. The memory device of the present embodiment then re-configures its pump to use the inductor instead of the internal pump, again giving the system much better power efficiency, or to run the internal pump from the inductor in another embodiment. In another embodiment, the external inductor is used along with an internal voltage higher than the supply voltage.

In yet another embodiment, two traditionally “no connect” pins are connectable to an external voltage and an external inductor. The memory still has a standard pin out configuration and is operable as a stand alone traditional memory when it is connected in a traditional system. Upon detection of the presence of one or the other on the external pins, the device operates using the one external element connected as has been described above with respect to each component individually. However, when both an external inductor and an external voltage are connected to the pins, both are used. In one embodiment, the external voltage is provided to the internal pump to provide a higher efficiency pumped voltage, and then that voltage is used with the external inductor to provide an even more efficient operation.

The embodiments of the present invention use a memory having standard pin out connections, but which has extra features that are enabled allowing the memory to be run more efficiently while not losing its standard references when an external voltage or other voltage supplying component is connected to the system.

In the various configurations of memory cards described above, when the card includes a standard pin configuration with two extra, traditionally “no connect” pins, a resistive pulldown can be used as described. If there is a pullup pin on the system, that pin connected to the resistive pulldown is internally low, and the memory card operates in a normal mode of operation like any other NAND memory card. Because the cards operate with a normal pin out configuration, they are usable in standard systems not configured to use a higher voltage supply for the internal pump. The two extra pins are “no connects” on the system. However, in systems that are configured to use an external or different internal power supply, the cards can be so used.

Alternatively, a single external power assistance mechanism or voltage is tied to the pin 304, and once the detection pin 302 is tied to a high signal, the single assistance mechanism tied to pin 304 is used to provide a starting voltage for the pump 306.

The embodiments of the present invention are all capable of being connected to and of running in standard systems, since the only components that affect behavior are on “no connect” pins in a standard configuration for memories and memory cards. It is only when a command or indication is sent to the memory or memory card, or when an external voltage is connected to or detected by the pins of the various embodiments that operation is commenced in the new modes.

In all of the embodiments of the present invention, a combination of external assistance and the internal supply voltage V_{cc} may be used without departing from the scope of the invention. In yet another embodiment, a voltage higher than the supply voltage V_{cc} may be present to operate other components of the system in which a memory card such as cards 100, 200 or 300 are to be used. Such other voltages include, but are not limited to, a display screen voltage supply, an internal battery supplying power, or the like. In such a configuration, it is a simple matter to modify the circuits and embodiments of the present invention to provide the other internal voltage to the internal pump, or to use an externally connected inductor in combination with the other internal voltage. Such modifications will be understood by those skilled in the art, and are within the scope of the present invention and embodiments.

The memory devices of the various embodiments of the present invention are configurable through a command from the controller during initial setup. This command in another embodiment is supplied right before a programming or an erase operation. The command in one embodiment tells the memory device to use either a supply from outside the card or to use an externally connected inductor instead of the internal pump.

Still further embodiments of the present invention include memory devices that use the concepts herein. For example, a memory suitable for use with the embodiments of the present invention is shown in Figure 4, which is a functional block diagram of a memory device 400, such as a flash memory device, of one embodiment of the present invention, which is coupled to a processor 410. The memory device 400 and the processor 410 may form part of an electronic system 420. The memory device 400 has been simplified to focus on features of the memory that are helpful in understanding the present invention. The memory device includes an array of memory cells 430. The memory array 430 is arranged in banks of rows and columns.

An address buffer circuit 440 is provided to latch address signals provided on address input connections A0-Ax 442. Address signals are received and decoded by row decoder 444 and a column decoder 446 to access the memory array 430. It will be appreciated by those skilled in the art, with the benefit of the present description, that the number of address input connections depends upon the density and architecture of the memory array. That is, the number of addresses increases with both increased memory cell counts and increased bank and block counts.

The memory device reads data in the array 430 by sensing voltage or current changes in the memory array columns using sense/latch circuitry 450. The sense/latch circuitry, in one embodiment, is coupled to read and latch a row of data from the memory array. Data input and output buffer circuitry 460 is included for bi-directional data communication over a plurality of data (DQ) connections 462 with the processor 410, and is connected to write circuitry 455 and read/latch circuitry 450 for performing read and write operations on the memory 400. Command control circuit 470 decodes signals provided on control connections 472 from the processor 410. These signals are used to control the operations on the memory array 430, including data read, data write, and erase operations.

The flash memory device has been simplified to facilitate a basic understanding of the features of the memory. A more detailed understanding of internal circuitry and functions of flash memories are known to those skilled in the art. Detection circuit 490 is used in one embodiment to detect whether to use an internal voltage pump (not shown) or to use an external voltage supply or inductor as has been described above in the various embodiments of the present invention. The embodiments described above are used in various embodiments in the basic memory array or system structure described in Figure 4.

Conclusion

The various embodiments of the invention include a memory with an internal detection mechanism to detect the presence of either an external component of an external voltage on some no connect pins, allowing a change in the configuration of the internal voltage pumps based on those detections, or which can be used as a standard device as well. The embodiments allow the system to lower its card power consumption depending upon availability of other voltage sources in the system or available components such as inductors to provide internal voltages more efficiently.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement, which is calculated to achieve the same purpose, may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed:

1. A stand-alone memory device comprising:
 - an array of memory cells;
 - control circuitry to read, write and erase the memory cells;
 - address circuitry to latch address signals provided on address input connections;
 - an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device; and
 - a detection mechanism connected to at least one connect pin that is a no connect pin in an industry standard pin out configuration to detect a presence of an external component to supply a voltage for the voltage pump, wherein the detection mechanism comprises:
 - a first n-type transistor gate connected to the connect pin, the first transistor passing the internal supply voltage to the voltage pump when no external voltage is connected to the connect pin; and
 - a second p-type transistor gate connected to the connect pin, the second transistor passing an external voltage to the voltage pump when an external voltage is connected to the connect pin.
2. The memory device of claim 1, wherein the second transistor only passes the external voltage to the voltage pump when the external voltage exceeds the internal supply voltage.
3. The memory device of claim 1, and further comprising:
 - a pull down resistor connected between the connect pin and the gates of the first and the second transistors.
4. A stand-alone memory device comprising:
 - an array of memory cells;
 - control circuitry to read, write and erase the memory cells;
 - address circuitry to latch address signals provided on address input connections
 - an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device; and

a detection mechanism connected to at least one connect pin that is a no connect pin in an industry standard pin out configuration to detect a presence of an external component to supply a voltage for the voltage pump, wherein the detection mechanism comprises:

a detection pin and a supply pin that are each no connect pins in an industry standard pin out configuration, the detection pin connectable to an enable signal, and the supply pin connectable to an external voltage component, the enable signal indicating whether to use the internal supply voltage or an external component connected to the second supply pin.

5. The memory device of claim 4, wherein the external component is a voltage supply or an inductor.

6. A stand-alone memory device comprising:

an array of memory cells;

control circuitry to read, write and erase the memory cells;

address circuitry to latch address signals provided on address input connections;

an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device; and

a detection mechanism connected to at least one connect pin that is a no connect pin in an industry standard pin out configuration to detect a presence of an external component to supply a voltage for the voltage pump, wherein the detection mechanism comprises:

a first external component pin and a second external component pin that are each no connect pins in an industry standard pin out configuration, the first external component pin connectable to an external voltage component, and the second external component pin connectable to an external inductor, to operate the internal pump using one or both of the external voltage component and the external inductor.

7. A stand-alone memory card, comprising:

a plurality of pins for connection of the memory card to a device using the memory card;

a memory device on the memory card, the memory device comprising:

- an array of memory cells;
- control circuitry to read, write and erase the memory cells;
- address circuitry to latch address signals provided on address input connections;

- an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device; and

- a detection mechanism to detect a presence of an external component to supply a voltage for the voltage pump, wherein the detection mechanism comprises:

- a connect pin;

- a first n-type transistor gate connected to the connect pin, the first transistor passing the internal supply voltage to the voltage pump when no external voltage is connected to the connect pin;

- a second p-type transistor gate connected to the connect pin, the second transistor passing an external voltage to the voltage pump when an external voltage is connected to the connect pin.

8. The memory card of claim 7, wherein the second transistor only passes the external voltage to the voltage pump when the external voltage exceeds the internal supply voltage.

9. The memory card of claim 7, and further comprising: a pull down resistor connected between the connect pin and the gates of the first and the second transistors.

10. A stand-alone memory card, comprising:

- a plurality of pins for connection of the memory card to a device using the memory card;

- a memory device on the memory card, the memory device comprising:

- an array of memory cells;
 - control circuitry to read, write and erase the memory cells;
 - address circuitry to latch address signals provided on address input connections;

an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device; and

a detection mechanism to detect a presence of an external component to supply a voltage for the voltage pump, wherein the detection mechanism comprises:

a detection pin and a supply pin, the detection pin connectable to an enable signal, and the supply pin connectable to an external voltage component, the enable signal indicating whether to use the internal supply voltage or an external component connected to the second supply pin.

11. The memory card of claim 10, wherein the external component is a voltage supply or an inductor.

12. A memory device comprising:

an array of memory cells;

control circuitry to read, write and erase the memory cells;

address circuitry to latch address signals provided on address input connections;

an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device;

a pin out configuration substantially similar to an industry standard pin out configuration; and

a detection circuit connected to a connect pin of the memory device, the connect pin being a no-connect pin in the industry standard pin put configuration, to detect whether to provide the internal supply voltage to the voltage pump or to use an external component to provide an external supply voltage to the voltage pump, wherein the detection circuit comprises:

a first n-type transistor gate connected to the connect pin, the first transistor passing the internal supply voltage to the voltage pump when no external voltage is connected to the connect pin;

a second p-type transistor gate connected to the connect pin, the second transistor passing an external voltage to the voltage pump when an external voltage is connected to the connect pin.

13. The memory device of claim 12, wherein the second transistor only passes the external voltage to the voltage pump when the external voltage exceeds the internal supply voltage.
14. A processing system, comprising:
a processor; and
a stand-alone memory coupled to the processor to store data provided by the processor and to provide data to the processor, the memory comprising:
an array of memory cells;
control circuitry to read, write and erase the memory cells;
address circuitry to latch address signals provided on address input connections;
an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device; and
a detection mechanism connected to at least one connect pin that is a no connect pin in an industry standard pin out configuration to detect a presence of an external component to supply a voltage for the voltage pump, wherein the detection mechanism comprises:
a first n-type transistor gate connected to the connect pin, the first transistor passing the internal supply voltage to the voltage pump when no external voltage is connected to the connect pin;
a second p-type transistor gate connected to the connect pin, the second transistor passing an external voltage to the voltage pump when an external voltage is connected to the connect pin.
15. The system of claim 14, wherein the second transistor only passes the external voltage to the voltage pump when the external voltage exceeds the internal supply voltage.
16. The system of claim 14, and further comprising:
a pull down resistor connected between the connect pin and the gates of the first and the second transistors.

17. A processing system, comprising:
a processor; and
a stand-alone memory coupled to the processor to store data provided by the processor and to provide data to the processor, the memory comprising:
an array of memory cells;
control circuitry to read, write and erase the memory cells;
address circuitry to latch address signals provided on address input connections;
an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device; and
a detection mechanism connected to at least one connect pin that is a no connect pin in an industry standard pin out configuration to detect a presence of an external component to supply a voltage for the voltage pump, wherein the detection mechanism comprises:
a detection pin and a supply pin, the detection pin connectable to an enable signal, and the supply pin connectable to an external voltage component, the enable signal indicating whether to use the internal supply voltage or an external component connected to the second supply pin.
18. The system of claim 17, wherein the external component is a voltage supply or an inductor.
19. A stand-alone memory device, comprising:
an array of memory cells;
control circuitry to read, write and erase the memory cells;
address circuitry to latch address signals provided on address input connections;
an internal voltage pump to provide a higher voltage than an internal supply voltage for the memory device; and
first and second connection pins, each of the first and the second connection pins being a no-connect pin in a pin out configuration substantially similar to an industry standard pin out configuration, the first connection pin connectable to an external voltage component,

and the second connection pin connectable to an external inductor, to operate the internal pump using one or both of the external voltage component and the external inductor.