PROCESS FOR PREPARATION OF SEPARABLE SEMICONDUCTOR ASSEMBLIES, PARTICULARLY TO FORM SUBSTRATES FOR ELECTRONICS, OPTOELECTRONICS AND OPTICS

DESCRIPTION

This invention relates in general to the manufacture of semi conducting substrates, particularly for the electronics, optoelectronics or optics industry.

Substrates composed of a film or thin layer on a thicker support are known.

Electronic, optoelectronic or optical components are made in the thin film of such a substrate, this thin film being intended to be separated from the support and if necessary applied onto another support, after at least some of the steps in its manufacture.

In order to achieve this, techniques have recently been developed for separating a useful thin layer from its support. Thus, the "epitaxial lift off" technique is well known in the domain of elements in groups III and V of the classification, and consists of inserting another thin

layer between a support and a thin layer, the other thin layer being called the sacrificial layer, and this sacrificial layer being made by epitaxy.

In practice, the sacrificial layer is made on the support by a first epitaxy operation, and the useful thin layer is also made by epitaxy.

The sacrificial layer is made so that it can be etched selectively with respect to the support and the useful thin layer; for example, an AlAs sacrificial layer is made between a GaAs support and a useful layer of AlGaAs.

In this known technique, the sacrificial thin layer obtained by hetero-epitaxy is monocrystalline and is thin. Its nature depends on the material of the support from which growth takes place.

The epitaxial lift off technique was described particularly in the "Ultra-high efficiency light-emitting diodes through epitaxial lift-off packaging" article by M. Sickmiller et al., International Symposium on Microelectronics, 1998, and its feasibility has been demonstrated for support surfaces and thin layers with and area of the order of a few square centimetres.

However, complementary tests have cast doubt on the feasibility of this technique for significantly larger areas, for example areas of the order of a few hundred cm^2 used in substrates for industry.

Another solution for making a separable bond could consist of molecular bonding between a support and a thin layer, and then making the separation at the bonding interface at the right time.

Bond forces obtained during this type of bonding vary depending on the different parameters (mainly the roughness of the surfaces, hydrophilic properties of surfaces, the chemical affinity between materials, their creepability, temperature, etc.). In some cases, such a separation could be considered.

However, if the thermal budget applied to the thin layer after this type of bonding is large, which is the case particularly during the manufacture of substrates for LEDs in which the temperatures of some treatments (particularly epitaxy using the MOCVD technique) can reach or significantly exceed 1000 to 1100°C, the effect of this budget on the bonding interface will necessarily be to significantly reinforce the interface, and separation will become more difficult if not impossible.

More particularly, when manufacturing substrates for LEDs, it may be necessary to carry out heat treatments on the support / thin film assembly necessitating such high temperatures, and particularly thermal oxidation steps or surface smoothing steps under hydrogenated atmosphere in order to prepare the surface before nitrides or others are deposited by epitaxy, these steps being done at a temperature of more than 1150°C.

Thus, for example if molecular bonding is done between two oxide layers, for example added on a support and a thin layer made of silicon carbide SiC, such temperatures would considerably increase the bonding forces to make them reach at least 2 Joules/m^2, so that separation would become impossible.

Embodiments of the invention provide a separable bonding interface, particularly for the manufacture of substrates for LEDs such as blue, green or ultraviolet(UV) LEDs, which remain separable even after treatment at high temperatures (1100 to 1150°C or even more).

Thus, this invention according to a first aspect provides a preparation process for a semiconductor based assembly comprising a first layer such as a support layer and a second layer such as a thin layer for applications in electronics, optoelectronics or optics, characterized in that it comprises the following steps:

- forming an interface layer on one only of the two layers,
- bringing the layer provided which the interface layer and the other exposed layer into contact with each other,

the interface layer being chosen as a function of the material in the exposed layer so as to intrinsically form, after the assembly has been exposed to temperatures in a predetermined range, a bonding interface that can be separated under the action of stresses.

In one advantageous embodiment, at least the exposed layer is made of silicon carbide, and in this case the interface layer is made from a material chosen from the group containing silicon oxide and silicon nitride.

One of the layers may form a germ layer for the formation of a substrate by epitaxial growth, and the other layer may form a temporary support layer for the germ layer.

Separation stresses are preferably mechanical stresses.

According to a second aspect, the invention provides a process for preparation of a semiconductor based assembly comprising a support and a thin layer for applications in electronics, optoelectronics or optics, the assembly being intended to be subjected to high temperatures within a given range, characterized in that it comprises a step to make a separable interface between the support and the thin layer by contacting and molecular bonding between two interface materials having an ability to chemically react with each other which is sufficiently low so that, after exposing the assembly to said high temperatures subsequently to said contacting, the bonding interface between the two materials is sufficiently weak bonding so that they can be separated by the application of stresses.

Preferably, the low potential of the interface materials to react chemically with each other is the result of a weak intrinsic mutual chemical affinity of the said interface materials, and / or the low creepability of at least one of the two interface materials.

In a first embodiment, the two interface materials are different and are composed respectively of the material in an interface layer added onto the support and directly by the material in the thin layer. In particular, an "add on layer" means a layer made by deposition or by chemical modification of a superficial thickness of the support, such as oxidation, etc.

In a second embodiment, the two interface materials are different and are composed of the material of an

interface layer added onto the thin layer, and directly by the support material, respectively.

Several possibilities could be considered for the materials:

- the material from which the add on interface layer is made is chosen from the group comprising an semi conducting oxide and a semi conducting nitride, while the different material is a semi conducting carbide, advantageously mono-crystalline,
- the two interface materials are semi conducting nitrides such as Si_3N_4,
- the two interface materials are a semi conducting nitride and a semi conducting oxide respectively.

The semiconductor mentioned above is typically silicon.

Advantageously, at least one of the interface materials has an intrinsically rough surface, in other words the roughness of the surface, in the commercial form of the material without any roughening treatment, is significantly more than 1 Å rms and is typically about 4 to 5 Å rms. This may be the support material itself, or it may be the material of the thin layer itself. A typical example of such an intrinsically rough material is silicon carbide, which at the moment is available commercially with roughnesses rarely less than 4 Å rms. Alternately, an intrinsically rough surface can be obtained by deposition on a surface that is less rough, this type of deposition inherently resulting in an imperfect surface condition with a roughness that can be as high as 4 to 5 Å rms.

In one specific embodiment, the assembly may comprise:

- a silicon carbide substrate,
- a useful layer made of monocrystalline silicon carbide,
- an interface layer made from a material chosen from among the group comprising silicon oxide and silicon nitride, added onto the face of the substrate facing the useful layer or onto the face of the useful layer facing the substrate.

Herein disclosed is a process for preparation of a substrate for making optoelectronic components such as light emitting diodes, and particularly blue LEDs, characterized in that it includes of the implementation the process according to the second aspect of the invention to obtain an assembly comprising a thin layer on a support, the formation of at least one substrate layer by epitaxy on the free surface of the thin layer of the assembly, and the separation of the thin layer provided with the epitaxied layer (s) from the support at the interface of the assembly.

The epitaxied layer (s) is (are) then preferably made from semi conducting materials based on semi conducting metallic nitrides.

According to a third aspect, the invention provides a process for making a semiconductor based structure, comprising a processed thin layer, for applications in electronics, optoelectronics and optics, characterized in that it comprises the following steps:

- preparing a semiconductor based assembly comprising a support and the thin layer, with the provision of an interface between the support and the thin layer by contacting and molecular bonding between two generally planar surfaces, at least one of the surfaces being the surface of a monocrystalline material, a main crystallographic plane of which has a slight inclination relative to the plane of the said surface,

- exposing the assembly to high temperatures in a given range during processes on the thin layer,

- separating the processed thin layer from the support by applying stresses, said slight inclination of said main crystallographic plane between the two interface materials allowing, in an intrinsic manner, a bonding which is sufficiently weak for allowing such separation.

Advantageously, this slight inclination is between 3 and 8° in the case of silicon carbide that is now commercially available. Typically, for such a material, the disorientation of the surface with respect to the (0001) axis of the crystal is preferably made along the (11-20) direction or the (1-100) direction, but other directions are also possible.

Other aspects, purposes and advantages of this invention will become clear after reading the following detailed description of preferred embodiments of the invention, given as non-limitative examples and with reference to the attached drawings, wherein:

Figures 1a-1e illustrate the steps in a process according to a first embodiment of the invention, and

Figures 2a-2e illustrate the steps in a process according to a second embodiment of the invention.

We will now describe example embodiments of the invention including an epitaxy step on a separable substrate. These examples apply to the production of blue, green or UV LEDs and laser diodes in thin layers, for a better extraction of emitted light or for better

dissipation of heat due to the addition of epitaxied layers onto a substrate made from a material that is a good conductor of heat, such as copper or diamond.

In this example, the epitaxial stack considered is based on semiconductors formed from GaN type metallic nitrides and their derivatives such as AlN, GaAlN, GaAlInN, etc., and more generally large gap metallic nitrides.

A first example embodiment is illustrated in Figures 1a-1e. With reference firstly to Figure 1a, the first step is to prepare a solid support 10, for example made of polycrystalline silicon carbide SiC or 4H or 6H monocrystalline SiC, or sapphire. An assembly comprising a donating substrate 20 made of silicon carbide SiC, preferably 4H or 6H monocrystalline, with an interface layer 26 in this case made from silicon oxide SiO_2, is also prepared.

An implantation step for one or several gaseous species is then applied to the substrate 20 at a given average depth, before or after the step making the oxide layer 220. This implantation creates an embrittlement plane 24 delimiting a thin layer 22 adjacent to the oxide layer and the rest of the substrate 20 (Smart-Cut - registered trademark - type technique as described particularly in document FR-A-2 681 472).

Figure 1B shows molecular bonding between the support 10 and the assembly 20, 22, 26 such that the silicon carbide in the support 10 is directly in contact with the oxide layer 26.

In passing, and as explained above, it should be noted that the SiC/SiO_2 bonding interface (at the SiC side) made

in this way with the 4 to 5 Å rms roughness of commercially available SiC, creates a intrinsically rough interface, regardless of whether the bonding is made on the Si face or the C face of a 4H or 6H type SiC. Thus, no roughening treatment of the SiC is necessary.

Furthermore, considering that SiC is only slightly oxidized at temperatures typically below 1150°C, the reactivity of one of the bonding surfaces with respect to the other remains limited (for contact with the Si face and for contact with the C face, even if the reactivity is not the same as will be seen below), and in any case is very much lower than the reactivity obtained for two bonding surfaces both made from SiO_2.

It is thought that reinforcing an SiO_2/SiO_2 bonding interface at high temperatures is explained by the development of Si-O-Si siloxane bonds and also by the creep of surfaces in contact. In the case of an SiC/SiO_2 interface, the chemical stability of the SiC surface means that these bonds do not form very much or do not form at all at the temperatures considered.

However in this respect it should be added that different behaviours may be observed depending on whether the C or the Si face of a 4H or 6H SiC crystal is applied in contact with the oxide, due to the chemical reactivity between the face concerned and SiO_2. Thus, it is preferable to use the Si face which is less sensitive to an oxidation reaction than the C face, and therefore with which bond energies will increase more slowly as a function of the added thermal energy.

Furthermore, the properties of SiC are such that its surface in contact with the SiO_2 layer does not creep (even if SiO_2 itself can creep) and that the chemical reactivity with SiO_2 is limited, which contributes to maintaining the fragility of the bond even when the assembly in Figure 1b is subjected to temperatures of more than 1150°C.

According to one variant embodiment, the donating substrate 20 can be cut such that its face from which the layer 22 will be sampled is slightly inclined with respect to one of the principal crystallographic plans of the structure. This inclination is preferably between 3 and 8°. In this way, the free face of what will be the transferred layer 22 has steps related to the successive offsets of crystals on this face, which contributes to an increase in the roughness which is conducive to the required separable nature.

After bringing into contact as illustrated in Figure 1b, the mass of substrate 20 is eliminated by the application of a thermal budget and/or appropriate mechanical stresses, in a manner known in itself by Smart-Cut and derived techniques, to leave only the thin layer of SiC 22 above the oxide layer 26. Obviously, the thin layer 22 can be made by any other appropriate thinning technique.

A subsequent step consists of depositing a stack 30 of materials such as the above mentioned nitrides on top of this thin layer 22 forming a germ layer, by one or several epitaxy deposition operations, for example in a manner that is conventional in itself to make LEDs.

Consequently, the germ layer 22 is firstly prepared particularly by polishing, annealing, smoothing annealing

(for example under hydrogen), sacrificial oxidation (in which the thin layer of oxide formed is eliminated), etching, smoothing surface treatment, etc.

Among the different materials that can be used to make the stack of epitaxied layers, some of the materials that can be used in particular are gallium nitride GaN, aluminium nitride AlN, aluminium and gallium nitride AlGaN, gallium and indium nitride GaInN, etc., the germ layer 22 being composed for example of monocrystalline SiC, Si(111) sapphire, monocrystalline gallium nitride GaN, neodymium and gallium oxide $NdGaO_2$, or lithium and gallium oxide $LiGaO_2$.

The chosen support material 10 may for example be a polycrystalline or monocrystalline SiC, sapphire, or polycrystalline AlN or GaN.

In term of thicknesses, the support layer 10 may for example be a few hundred micrometers thick (typically 300 μm), while the thickness of the germ layer 22 will be of the order of 0.1 to 1 μm.

The interface layer 26 is of the order of 1 μm thick.

Epitaxies used to make the useful layer may be done using techniques well known to those skilled in the art, and particularly the MBE (Molecular Beam Epitaxy) technique or the MOCVD (Metallo-Organic Chemical Vapour Deposition) technique may be used.

In the first case, the epitaxial growth temperatures rarely exceed 600°C, while they can be as high as 1050 to 1100°C in the second case.

It is important to note here that in the latter case, due to a molecular bonding interface that does not increase

much in strength at temperatures below 1100-1150°C as explained in detail above, this interface maintains a fragility conducive to its subsequent separation as will be seen.

This stack 30 is illustrated in Figure 1d.

Finally with reference to Figure 1e, the assembly composed of the stack 30, the thin layer 22 and the oxide layer 26 is separated from the support 10 at the SiC/SiO_2 interface between the support 10 and the layer 26, this interface involving bonding forces that remain limited as was mentioned above.

In particular, this disassembly may be done by the application of mechanical tension and / or shear and / or bending stresses, for example using a blade, with manual or robot control.

At the end of this process and after an appropriate surface treatment, the support 10 can be reused, and the donating substrate 20 can also be reused and will be subjected to a step to deposit an SiO_2 layer and a step for the implantation of gaseous species as described above.

Figures 2a to 2e illustrate a process similar to the process in Figures 1a to 1e, with the essential difference being that the oxide layer SiO_2 that will participate in the separable interface is made on the support 10 instead of on the source substrate 20; in this case this oxide layer is denoted reference 12. Thus, if the source substrate 20 is made of SiC, molecular bonding between the oxide layer 12 and the source substrate 20 (Figure 2b) has separability properties similar to those obtained between

the oxide layer 26 and the support 10 in the case in Figures 1a-1e.

Figures 2c and 2d illustrate the thinning step and the step to produce a stack by epitaxy similar to those in Figures 1c and 1d.

In this second example, separation occurs between layers 12 and 20, and the resulting product is illustrated in Figure 2e.

Many variants may be made to the invention. In particular, weakened molecular bonds at the separable bonding interface may be obtained by making this bond between two layers of silicon nitride Si_3N_1 deposited on the support 10 and on the source substrate 20 respectively. In particular, with such layers which are necessarily made using a deposition technique (unlike oxide layers that are frequently made by superficial thermal oxidation), this type of deposit necessarily creates a specific roughness intrinsic to the level of the final free surface. Furthermore, Si_3N_4 creeps at higher temperature than SiO_2. Obviously, in this case no polishing treatment that could excessively reduce the roughness should be carried out.

According to another variant, the bond between an SiO_2 layer deposited on the support 10 or the source substrate 20, and a layer of Si_3N_4 deposited on the source substrate 20 or on the support 10, can be made.

Once again, few strong siloxane type or other types of bonds are formed between the two layers, even at high temperatures, and the bond remain separable after the treatments.

According to yet another variant, a layer of SiO_2 will be provided on the support 10 or the source substrate 20, and on the other side a layer with an appropriate intrinsic roughness could be provided such that the bond forces between the SiO_2 layer and the rough layer will only be developed moderately at the required temperatures, without any particular roughness treatment, so that the bond remains separable.

For example, this intrinsically rough layer can be made by deposition of amorphous or polycrystalline silicon.

In this respect, there is no need for the materials at which the bond is made to be different from each other.

For example, a direct bond of SiC on SiC could be made, taking advantage of the intrinsic roughness of the SiC on both sides of the bond, its low creepability and its low ability to react chemically with itself. As a variant, and if necessary, an SiC layer could be deposited on the thin layer or the support layer to increase the intrinsic roughness.

According to another example, a direct Si on Si bond could be made with several possibilities:

- using a polycrystalline Si (particularly for the support) to benefit from its intrinsic roughness related to the existence of grain boundaries;
- additionally, or as a variant, it would be possible to deposit an interface layer of Si either on the support layer or on the thin layer or on both, as described above generating an increased intrinsic roughness.

According to yet another example, a thin layer of SiC could be deposited directly on a sapphire support.

Those skilled in the art will easily be able to imagine other examples based on the description given above.

This invention is applicable to the manufacture of a wide variety of semiconductor-based assemblies in addition to those mentioned above, and particularly gallium arsenide AsGa.

AMENDED CLAIMS

[received by the International Bureau on 27 October 2003 (27.10.03);
original claims 1, 6 and 24 amended; remaining claims unchanged (5 pages)]

1. Preparation process for a semiconductor based assembly comprising a first layer such as a support layer and a second layer such as a thin layer for applications in electronics, optoelectronics or optics, characterized in that it comprises the following steps:

- forming an interface layer on one only of the two layers,

- bringing the layer provided which the interface layer and the other exposed layer into contact with each other,

the interface layer being chosen as a function of the material in the exposed layer so as to intrinsically form, after the assembly has been exposed to temperatures in a predetermined range, a bonding interface that can be separated under the action of stresses.

2. Process according to claim 1, characterized in that at least the exposed layer is made of silicon carbide, and preferably monocrystalline silicon carbide.

3. Process according to claim 2, characterized in that the interface layer is made from a material chosen from the group containing silicon oxide and silicon nitride.

4. Process according to one of claims 1 to 3, characterized in that one of the layers forms a germ layer for the formation of a substrate by epitaxial growth, and the other layer forms a temporary support layer for the germ layer.

5. Process according to one of claims 1 to 4, characterized in that the stresses are mechanical stresses.

6. Process for preparation of a semiconductor based assembly comprising a support and a thin layer for applications in electronics, optoelectronics or optics, the assembly being intended to be subjected to high temperatures within a given range, characterized in that it comprises a step to make a separable interface between the support and the thin layer by contacting and molecular bonding between two interface materials having an ability to chemically react with each other which is sufficiently low so that, after exposing the assembly to said high temperatures subsequently to said contacting, the bonding interface between the two materials is sufficiently weak so that they can be separated by the application of stresses.

7. Process according to claim 6, characterized in that the low ability of the interface materials to react chemically with each other results from a weak intrinsic mutual chemical affinity of said interface materials.

8. Process according to one of claims 6 and 7, characterized in that the low ability of the interface materials to react chemically with each other is the result of a low creepability of at least one of the two interface materials.

9. Process according to one of claims 6 to 8, characterized in that the two interface materials are different.

10. Process according to claim 9, characterized in that the two different interface materials are composed respectively of the material in an interface layer added onto the support and directly by the material of the thin layer.

11. Process according to claim 9, characterized in that the two different interface materials are composed of the material of an interface layer added onto the thin layer, and directly by the support material.

12. Process according to one of claims 10 and 11, characterized in that the material of the added interface layer is selected from the group comprising a semiconductor oxide and a semiconductor nitride, while the different material is a semiconductor carbide.

13. Process according to claim 12, characterized in that the semiconductor nitride is monocrystalline.

14. Process according to one of claims 6 to 8, characterized in that the two interface materials are semiconductor nitrides.

15. Process according to one of claims 6 to 8, characterized in that one of the two interface materials is a semiconductor nitride and the other is a semiconductor oxide.

16. Process according to one of claims 12 to 15, characterized in that the semiconductor is silicon.

17. Process according to one of claims 6 to 16, characterized in that at least one of the interface materials has an intrinsically rough surface.

18. Process according to claim 17, characterized in that the intrinsically rough interface material is made of the support material itself.

19. Process according to claim 17, characterized in that the intrinsically rough interface material is made of the material of the thin layer itself.

20. Process according to claim 17, characterized in that the intrinsically rough interface material is made of a deposit of interface material on a surface of lesser rugosity.

21. Process according to claim 6, characterized in that the assembly comprises:

- a silicon carbide substrate,
- a useful layer made of silicon carbide,
- an interface layer made of a material selected from the group comprising silicon oxide and silicon nitride, added onto the face of the substrate facing the thin layer or onto the face of the thin layer facing the substrate.

22. Process for preparation of a substrate for making optoelectronic components such as light emitting diodes (LEDs), and particularly blue LEDs, characterized in that it includes the implementation of the process according to one of claims 6 to 21 to obtain an assembly comprising a thin layer on a support, the formation of at least one

substrate layer by epitaxy on the free surface of the thin layer of the assembly, and the separation of the thin layer provided with the epitaxied layer(s) from the support at the interface of the assembly.

23. Process according to claim 22, characterized in that the epitaxied layer(s) is (are) made from semiconductor materials based on semiconducting metallic nitrides.

24. Process for making a semiconductor based structure, comprising a processed thin layer, for applications in electronics, optoelectronics and optics, characterized in that it comprises the following steps:

- preparing a semiconductor based assembly comprising a support and the thin layer, with the provision of an interface between the support and the thin layer by contacting and molecular bonding between two generally planar surfaces, at least one of the surfaces being the surface of a monocrystalline material, a main crystallographic plane of which has a slight inclination relative to the plane of the said surface,
- exposing the assembly to high temperatures in a given range during processes on the thin layer,
- separating the processed thin layer from the support by applying stresses, said slight inclination of said main crystallographic plane between the two interface materials allowing, in an intrinsic manner, a bonding which is sufficiently weak for allowing such separation.

25. Process according to claim 24, characterized in that said slight inclination is between 3 and 8°.