

This invention relates to a circuit arrangement to detect a voltage, including a voltage divider having applied to its divider node the input of a voltage detector which comprises a Schmitt-Trigger with reference voltage and an output driver, with the output of the voltage detector being connected to the positive potential of the voltage.

Voltage detectors comprising internally a Schmitt-Trigger with reference voltage and an output driver are commercially available devices. FIG. 4 illustrates the wiring of such a voltage detector VD when a specified voltage, for example, the voltage of two serially connected battery cells or accumulator cells (B), is to be detected which is greater than the internal reference voltage of the voltage detector VD. In this event, a voltage divider comprised of resistors R1 and R4 is connected in parallel with the battery B, and the junction of the two resistors R1 and R4 is connected to the IN input of the voltage detector VD. The OUT output of the voltage detector VD is applied to the positive potential of the battery B through a resistor R2. The voltage divider R1/R4 is so dimensioned that the internal reference voltage (2.1 volts, for example) will be present at the IN input of the voltage detector VD when the voltage to be detected (2.3 volts, for example) is present at the battery B. When the battery voltage drops below this value, the output of the voltage comparator VD will go from "high" to "low".

However, such commercially available voltage detectors have the disadvantage of having a hysteresis of, for example, 0.1 volts. This means that with the battery voltage falling, the output of the voltage detector VD will go from "high" to "low" when the voltage at the input reaches 2.1 volts (correspondingly 2.3 volts at the battery), however, with the battery voltage rising (for example, when the battery is being recharged), the output of the voltage detector VD will not reverse its state until the voltage at the input reaches 2.2 volts (2.1 volts + 0.1 volts). This is not satisfactory for some applications requiring an accurate voltage detection as, for example, when it is desired to detect a specified voltage accurately on a battery during both discharging and charging of the battery.

Further, from U.S. Pat. No. 4,906,055 a circuit arrangement is known in which the source voltage of a power source is tested for the attainment of different threshold values. In this arrangement, a voltage detector is provided in which an applied voltage is compared

...

with a single reference voltage. The attainment of several threshold values of the voltage of the power source is tested by applying the voltage to a voltage divider and comparing the divided voltage with the reference value in order to determine the attainment of a first threshold value, and by applying the full voltage of the power source to the same voltage detector and thus comparing it with the same reference value in order to determine the attainment of a second threshold value of the voltage of the power source. When the divided voltage is lower than the reference voltage, it is found that the voltage is below the first threshold value. When the full voltage of the power source is lower than the reference value, it is found that the voltage of the power source is below the second threshold value. In order to apply the proper voltage to the voltage detector, that is, either the divided voltage or the full voltage of the power source, the output signal of the voltage detector is fed to a CPU which in turn generates an output signal closing or opening a controllable switching means, with the closed position of this controllable switching means causing the full voltage of the power source to be applied to the voltage detector. The test procedure is as follows: First, the divided voltage is applied to the voltage detector. If the divided voltage is higher than the reference voltage, the voltage detector issues a "high" voltage signal, that is, the CPU continues to keep the controllable switching means open. If the divided voltage is found to be lower than the reference voltage, the voltage detector issues a "low" voltage signal. This then causes the CPU to close the controllable switching means. In this event, the voltage of the power source is below the first threshold value. The controllable switching means being closed, it is then tested in the next step whether the full voltage of the power source is lower than the reference value. If the answer is no, the voltage detector issues again a "high" voltage signal. This means that the CPU places the controllable switching means again in a non-conductive condition. In the next step the divided voltage is again fed to the voltage detector which again delivers a "low" voltage signal. The circuitry is thus caused to oscillate. If the full voltage is lower than the reference value of the voltage detector, the voltage detector constantly delivers a "low" voltage signal, meaning that the voltage of the power source is below the second threshold value. The subject-matter of this prior application is then required to continue generating CPU output signals, with a light-emitting diode as a warning device being driven when the voltage falls below the first threshold value. When it falls below the second threshold value, a load connected to the power source is deactivated, and a second diode is

driven to inform of this condition. This U.S. patent specification merely sets out with respect to the voltage detector that it includes a specified reference value. The specification does not describe that this specified reference value may have a hysteresis. By contrast, it is disclosed in this specification that the voltage detector is to include a specified value of the reference value, that is, that it is precisely the absence of a hysteresis in the reference voltage that is desired. When in the subject-matter of this prior application a voltage comparator whose reference voltage has a hysteresis is substituted for the voltage detector with a specified reference voltage, it will be seen that the first threshold value is tested by comparing the divided voltage with the lower value of the hysteresis of the reference voltage. Prior to each test of the divided voltage, the output of the voltage comparator is at a "high" level because of the full voltage which is above the reference value. When the second threshold value is tested, it will be seen that the full voltage is compared with the upper value of the hysteresis of the reference voltage. Because of the circuitry oscillating, the comparator is at a "low" level because the divided voltage is below the reference voltage. However, since in the subject-matter of the U.S. patent specification a specified reference voltage is to be employed, a voltage comparator whose reference voltage has a hysteresis cannot find application. As a result, in the use of a voltage comparator whose reference voltage includes a hysteresis, different reference voltages would be used when testing the attainment of the different threshold values.

It is therefore an object of the present invention to configure a circuit arrangement of the type initially referred to in such a manner as to permit a hysteresis-free detection of a specified voltage.

According to the present invention, this object is accomplished in that the output signal of the voltage detector is applied to the base of a first transistor, that the collector-emitter circuit, together with a series-connected capacitor, is connected in parallel with the voltage to be detected, that the junction of the capacitor and the first transistor is connected to the input of the voltage detector through a first resistor, and that the output of the voltage detector is further applied to the input of a component delivering different output signals in dependence upon whether its input receives a constant signal level or a varying signal level.

...

When it is desired to detect several specified voltages using the same voltage detector or to be able to vary the value of the voltage to be detected, the resistor of the first voltage divider connected to reference potential is comprised of a second voltage divider to which an integrating capacitor is connected in parallel and whose divider node receives a square-wave voltage whose pulse duty factor is variable.

Further advantageous embodiments of the present invention will become apparent from the other dependent claims and the subsequent description.

Embodiments of the present invention will now be described in more detail in the following with reference to the accompanying drawings, in which:

FIG. 1 is a schematic diagram showing a circuit arrangement for detecting a specified voltage value on a battery;

FIGS. 2 and 3 are schematic diagrams showing circuit arrangements for detecting several voltage values using a single voltage detector.

Referring now to FIG. 1 of the drawings, there is shown a circuit arrangement providing a suitable indication when the voltage U of the battery B has reached a specified value. A load resistor R_L may be connected to this battery (accumulator) through a switch S . This load resistor may be the motor of a small electrical appliance as, for example, an electric shaver. The battery is rechargeable by means of a charging circuitry not shown.

Connected in parallel with the battery B is a voltage divider comprised of resistors R_1 and R_4 , by means of which the voltage U of the battery B is divided down to the voltage U_e residing at the junction of the resistors R_1 and R_4 which is applied to the IN input of the voltage detector VD . The OUT output of the voltage detector VD is connected to the positive terminal of the battery B through a resistor R_2 , to the base of a transistor T_1 through a resistor R_3 , and to the microprocessor C driving a display device D through a resistor R_{10} .

The emitter of transistor T_1 is connected to the positive terminal of the battery B , its collector being connected to reference potential through a capacitor C_1 . In addition, the collector is connected to the junction of the resistors R_1 and R_4 of the voltage divider through resistors R_5 and R_6 . The resistor R_6 is of the variable type for adjustment.

...

The voltage divider $R1/R4$ is dimensioned such as to ensure that, when the battery B reaches a specified voltage U, the divided-down voltage U_e at the IN input of the voltage detector VD lies below the detection voltage of the voltage detector VD. This specified voltage U may be, for example, the "low charge" point at 2.3 volts (in which event the battery is discharged to 10% to 20% of its capacity). When the detection voltage of the voltage detector is, for example, 2.1 volts and the tolerance is ± 0.1 volts (which has no relation to the hysteresis of the voltage detector), these are 2.0 volts.

The mode of function of the circuit arrangement is as follows: When the battery voltage U has dropped to the voltage to be detected which is, for example, 2.3 volts, the voltage U_e at the IN input of the voltage detector VD will be 2.0 volts, and the OUT output of the voltage detector VD will change from "high" to "low". "Low" is the active state of the voltage detector VD. Transistor T1 will then conduct, causing the series arrangement comprised of the resistors R5, R6 to be connected in parallel with resistor R1. The input voltage U_e (divider voltage) is thereby increased to a value greater than the detection voltage of the voltage detector plus the hysteresis voltage, causing the voltage detector to assume the reverse state again (release voltage) and the OUT output to return to "high". The transistor T1 is again non-conducting, cancelling the parallel connection of resistors R5, R6 to resistor R1, whereby the divider voltage U_e is again below the detection voltage of the voltage detector VD, and the OUT output is again changed to "low".

The circuitry oscillates. The capacitor C1 provides time delays for the transition operations, thus reducing the oscillation frequency to about 1 kHz, for example. A square-wave voltage with an amplitude of the order of the battery voltage U is present at the OUT output.

Oscillation will cease to be possible when the release voltage of the voltage detector is no longer attained with the transistor T1 conducting. At this instant, the state of the voltage detector VD will be maintained, its output voltage being constantly at "low". This voltage point is adjusted by means of resistor R6.

Thus, it is possible to detect a specified value of the supply voltage solely by the presence of a constant signal level at the output of the voltage detector VD with respect to a varying (oscillating) signal level. The specified voltage value is detected without hysteresis, that is, it is irrelevant whether the specified

voltage value is reached starting from higher or from lower voltage values, since it is not the internal reference voltage of the voltage detector (2.1 volts) that is used for adjustment, but rather its release voltage.

The circuit arrangements of FIGS. 2 and 3 present an extension of FIG. 1 to cover the detection of several voltages using just a single voltage detector VD. In these Figures, the resistor R4 of FIG. 1 is subdivided into serially connected resistors R7, R8 and R9, whereof resistor R7 is connected to the input of the voltage detector VD, while resistor R9 is tied to reference potential. An integrating capacitor C2 is connected in parallel with the series arrangement comprised of resistors R8 and R9.

In FIG. 2, an output of the microprocessor C is connected to the junction of resistors R8 and R9. The microprocessor supplies to this junction a square-wave control signal whose pulse duty factor is variable.

Owing to this variable pulse duty factor, in combination with the resistors R7, R8, R9 and the integrating capacitor C2, the release voltage point of the voltage detector VD can be shifted over a wide range of the voltage U of the battery B. The greater the pulse duty factor of the square-wave voltage supplied, that is, the greater the ratio of pulse duration to pulse spacing, the higher the mean value of the voltage supplied. Correspondingly, the voltage at the junction of capacitor C2 and resistor R8, and consequently also the voltage Ue at the input of the voltage detector VD, are raised, whereby the release voltage of the voltage detector is reached at higher battery voltages U.

As described with reference to FIG. 1, it is thus possible to determine and detect any desired number of voltage points of the battery voltage U by varying the pulse duty factor of the square-wave voltage supplied. By sensing a voltage point and subsequently specifying a next voltage point by correspondingly varying the pulse duty factor of the square-wave voltage supplied, the voltage characteristic of a battery during charging and/or discharging can be retraced in dependence on time.

By allocating specified voltage points of a discharging or charging characteristic of the battery (for example, between 2.5 volts and 2.2 volts at 50 mV intervals) to a visual signal of the display device D, the current charging condition of the battery is displayed. Where a display device D comprising several segments is

...

employed, the segments are controlled by the microprocessor C such that in the fully charged condition (highest detected voltage), all segments are driven, whilst with the battery charge near depletion (lowest detected voltage), no segment is driven.

Where the display device D incorporating several segments provides a continuous indication of the charging condition on a time basis, that is, in dependence on the period of time during which the load resistor RL (load) was connected to the battery or the battery was charged, the voltage points detected in operation will be compared with the values of the battery charging and discharging characteristic stored in the microprocessor, and if a deviation is established, the display will be corrected correspondingly.

FIG. 3 shows a circuit arrangement suitable for the event that the voltage divider is not sufficiently high-resistance, that is, the output of the microprocessor C supplying the square-wave voltage is not in a position to provide the requisite power. In this case, the square-wave signal of the microprocessor C will be delivered through a resistor R11 to the base of a transistor T2 whose collector-emitter circuit is in parallel with the resistor R9. In accordance with the pulse duty factor of the square-wave signal supplied, the transistor T2 is rendered either conducting or non-conducting. In all other respects, the mode of function of the circuit arrangement is the same as that of FIG. 2.

All circuit arrangements described in the foregoing are self-oscillating, requiring no control voltages from an external source. In consequence of the low current requirements, the circuit arrangements may remain connected to the supply voltage U also with the appliance turned off (load resistor RL disconnected from the battery), without the battery discharging unacceptably.

Patent Claims

1. A circuit arrangement to detect a voltage (U), including a first voltage divider (R1, R4) having applied to its divider node the input of a voltage detector (VD) which comprises a Schmitt-Trigger with reference voltage and an output driver, with the output of the voltage detector (VD) being connected to the positive potential of the voltage (U), characterized in that the output signal of the voltage detector (VD) is applied to the base of a first transistor (T1), that the collector-emitter circuit of the first transistor (T1), together with a series-connected capacitor (C1), is connected in parallel with the voltage (U) to be detected, that the junction of the capacitor (C1) and the first transistor (T1) is connected to the input of the voltage detector (VD) through a first resistor (R5, R6), and that the output of the voltage detector (VD) is further applied to the input of a first component delivering different output signals in dependence upon whether its input receives a constant signal level or a varying signal level.

2. A circuit arrangement as claimed in claim 1, characterized in that the first component controls a display device (D) in dependence upon its input signal, such as to enable it to recognize whether the detected voltage (U) has reached a specified voltage value and/or lies above or below the specified voltage value.

3. A circuit arrangement as claimed in claim 1, characterized in that part of the first resistor (R5, R6) is adjustable (R6).

4. A circuit arrangement as claimed in claim 1, characterized in that the resistor (R4) of the first voltage divider (R1, R4) connected to reference potential is comprised of a second voltage divider (R8, R9) to which an integrating capacitor (C2) is connected in parallel, and that a second component delivers to the divider node of the second voltage divider (R8, R9) a square-wave voltage.

5. A circuit arrangement as claimed in claim 4, characterized in that a second resistor (R7) is inserted between the second voltage divider (R8, R9) and the input (IN) of the voltage detector (VD).

6. A circuit arrangement as claimed in claim 4, characterized in that the pulse duty factor of the square-wave voltage is variable.

...

7. A circuit arrangement as claimed in claim 1 or claim 4, characterized in that the first component and/or the second component are parts of a microprocessor (C).

8. A circuit arrangement as claimed in claim 6, characterized in that different specified values of the voltage (U) are determined by means of varying pulse duty factors of the square-wave voltage, and that a display device (D) provides a suitable indication when these specified voltage values are reached.

9. A circuit arrangement as claimed in claim 6, characterized in that the voltage (U) to be detected is the supply voltage of a battery (B), that different specified values of the battery voltage are determined by means of varying pulse duty factors of the square-wave voltage, that the supply voltage of the battery B is compared with the known charging/discharging characteristic of the battery, and that a time-controlled charge-status indication is corrected correspondingly when a deviation is established.

07 Feb 95/BH.