CLAIMS

What is claimed is:

1. A semiconductor device (10), comprising:

a substrate (100);

common electrode structures (200), the common electrode structures being stacked on the substrate in a first direction (D1), and the first direction intersecting the substrate;

stacked array structures (20), the stacked array structures comprising first electrode structures (300), and the first electrode structures being stacked on the substrate in the first direction and being electrically connected to the common electrode structures disposed at same layers with the first electrode structures;

first lead-out structures (400), the first lead-out structures being stacked in the first direction and being connected to the common electrode structures disposed at same layers with the first lead-out structures, the first lead-out structures comprising first lead-out wires (401) and first pseudowires (402) that are disposed opposite to each other, and the first lead-out wires and the first pseudowires in the different first lead-out structures being alternately disposed in the first direction; and

second lead-out structures (500), the second lead-out structures comprising second contact pads (501) and second contact plugs (502), the second contact pads being disposed at same layers with the corresponding first lead-out wires and being electrically connected to the corresponding common electrode structures through the corresponding first lead-out wires, the second contact plugs being disposed on the second contact pads, and the second contact plugs being staggered from each other in the first direction.

2. The semiconductor device according to claim 1, wherein

the first lead-out structures extend in a third direction (D3), the second lead-out structures are staggered in the third direction, and the third direction is parallel to the substrate.

3. The semiconductor device according to claim 1, wherein

the first lead-out structures extend in a third direction, the third direction is parallel to the substrate, the second lead-out structures are disposed in a second direction (D2), projections of the second lead-out structures on the substrate in the first direction partially overlap, and the second direction is parallel to the substrate and intersects the third direction.

4. The semiconductor device according to claim 3, wherein

the first lead-out wires connected to the second lead-out structures whose projections on the substrate in the first direction partially overlap are spaced apart by at least one layer.

5. The semiconductor device according to claim 1, wherein

the first electrode structures comprise bit line structures or word line structures.

6. The semiconductor device according to claim 1, wherein

both ends of the first lead-out structures are connected to the common electrode structures.

7. The semiconductor device according to claim 1, wherein

the second contact pads and the first lead-out wires are unibody.

8. The semiconductor device according to claim 1, wherein

the second contact pads and the second contact plugs are unibody.

9. The semiconductor device according to claim 1, wherein

each of the first pseudowires comprises laminated polysilicon and silicon nitride.

10. The semiconductor device according to claim 4, wherein

the first electrode structures comprise bit line structures or word line structures.

11. The semiconductor device according to claim 4, wherein

both ends of the first lead-out structures are connected to the common electrode structures.

12. The semiconductor device according to claim 4, wherein

each of the first pseudowires comprises laminated polysilicon and silicon nitride.

13. A manufacturing method for a semiconductor device, comprising:

providing a substrate on which a stacked structure is formed;

forming common electrode structures in the stacked structure;

forming stacked array structures in the stacked structure, the stacked array structures comprising first electrode structures;

forming first lead-out structures in the stacked structure, the first lead-out structures comprising first lead-out wires and first pseudowires that are disposed opposite to each other, the first lead-out wires and the first pseudowires in the different first lead-out structures being alternately disposed in the first direction, and the first direction intersecting the substrate; and

forming second lead-out structures in the stacked structure, the second lead-out structures comprising second contact pads and second contact plugs;

the common electrode structures being electrically connected to the first electrode structures formed at same layers with the common electrode structures, the second lead-out structures being electrically connected to the common electrode structures through the first lead-out wires, the second contact plugs being formed on the second contact pads, and the second contact plugs being staggered from each other in the first direction.

14. The manufacturing method for a semiconductor device according to claim 13,

wherein

the first lead-out wires, the second contact pads, and the second contact plugs are formed in a same step.

15. The manufacturing method for a semiconductor device according to claim 13, wherein

the step of forming the first lead-out structures comprises: first forming filling layers, the filling layers padding positions of the first lead-out structures;

forming trench structures corresponding to the second lead-out structures, and exposing the corresponding filling layers;

removing the exposed filling layers; and

forming the first lead-out wires, the second contact pads, and the second contact plugs, the remaining filling layers forming the first pseudowires.

16. The manufacturing method for a semiconductor device according to claim 15, wherein

the filling layers are formed by depositing polysilicon and silicon nitride in a lamination manner.

17. The manufacturing method for a semiconductor device according to claim 13, wherein

the forming the stacked structure comprises: alternately forming a silicon layer and a silicon-germanium layer.

18. The manufacturing method for a semiconductor device according to claim 13, wherein

the first electrode structures comprise bit line structures or word line structures.

19. The manufacturing method for a semiconductor device according to claim 13, wherein

both ends of the first lead-out structures are connected to the common electrode structures.

20. The manufacturing method for a semiconductor device according to claim 13, wherein

the first lead-out structures extend in a third direction, the third direction is parallel to the substrate, the second lead-out structures are formed in a second direction, projections of the second lead-out structures on the substrate in the first direction partially overlap, and the second direction is parallel to the substrate and intersects the third direction.