1,099,770

PATENT SPECIFICATION

DRAWINGS ATTACHED

1,099,770

Date of Application and filing Complete Specification: Dec. 28, 1966.

No. 57999/66.

Application made in United States of America (No. 533,635) on March 11, 1966.

Complete Specification Published: Jan. 17, 1968.

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Index at acceptance:—H1 K(1A1, 1C1, 1D3A, 1D4X, 4C11, 4C14, 5C5, 9D1, 9D2, 9K)

Int. Cl.:—H 01 l 15/00

COMPLETE SPECIFICATION

Improvements in or relating to Detector Array

We, FAIRCHILD CAMERA & INSTRUMENT CORPORATION, of 300 Robbins Lane, ~~Syosset~~, Long Island, New York, a Corporation of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

Detector arrays, such as photodetector arrays, have been constructed for the purpose of enabling image dissection by addressing each photodetector and determining the amplitude of the signal which it produces as an output. The problems that have been presented are not so much with the arrangement of the photodetectors in an array, but in the apparatus for sampling the photodetectors.

An object of this invention is the provision of a novel, simple, stable, and reliable apparatus for selectively sampling the photodetectors in an array of photodetectors which lends itself to integrated circuit techniques.

Effectively, the objects of the invention are accomplished by providing an image detection arrangement comprising a plurality of detecting devices on which the image is incident, each detecting device being operatively associated with a MOS transistor, the detecting devices and associated MOS transistors being arranged in rows and columns to form an array, means for selectively applying energising potentials to the MOS transistors in the rows and columns to render operative the MOS transistors at the intersections of the selected rows and columns whereby the associated detecting devices are selectively energised as determined by the image pattern and means for deriving outputs from said energised detecting devices.

The above system is preferably constructed by integrating with each detector in any array a MOS transistor having a gate electrode, a bulk electrode, and a pair of electrodes, one being a source and the other a drain. They are interconnected so that when a row and a column are energized, the detector at the intersection of the excited row and column has its signal sampled. The purpose of the MOS transistor is to perform an "And" function when row and column coincidence occur and thus to enable sampling.

MOS transistors are known devices characterized by a metal layer serving as the gate electrode and capacitively coupled to the semiconductor material through an insulating layer, often of an oxide of the semiconductive material such as silicon dioxide. The acronym MOS stands for Metal-Oxide-Semiconductor.

The invention will be better understood from the following description when read in connection with the accompanying drawings, comprising Figs. 1 and 2 in which:

Figure 1 is a schematic circuit diagram of a detector array in accordance with this invention; and

Figure 2 is a schematic illustration of an arrangement of a photodetector and sampling structure array, in accordance with this invention, as it would appear using integrated circuit techniques.

Referring now to Figure 1, there is shown a schematic circuit diagram of a two-dimensional array of detectors, for example, photodetectors, combined with the sampling circuitry in accordance with this invention. By way of illustration, and not to serve as a limitation upon the invention, there is also shown additional circuitry for selectively exciting the array at television frequencies, since an array, in accordance with this invention, may be considered as a solid state equivalent to a vidicon tube. Further, a 3 x 3 array is shown. This also should not be construed as a limitation upon the invention, but only as exemplary since an array of the type described herein can be made with densities in excess of 200 devices per inch in each dimension.

In the array shown in Figure 1, the MOS transistors in column 1 respectively are desig-

nated by reference numerals 11, 12, 13. In the second column, the MOS transistors are designated by reference numerals 21, 22, 23, respectively. The MOS transistors in the third column are designated by reference numerals 31, 32, 33, respectively. Associated with each one of the MOS transistors in the first column is a photodetector respectively 15,16, 17. Associated with each MOS transistor in the second column is a photodetector respectively 25, 26, 27. Associated with each MOS transistor in the third column is a photodetector respectively 35, 36, 37.

The photodetectors may be either a two layer structure (i.e., a photodiode) or a three layer structure (i.e. a phototransistor as illustrated herein). An added advantage of a three layer structure is that by proper choice in sample time and scan time, it is possible to operate the detectors in a storage mode, obtaining the advantages of this mode of operation, which is employed in television cameras.

A row bus 41 connects all the gate electrodes of all of the MOS transistors 11, 21, 31 together, so that upon the application to this row bus of a voltage which exceeds a predetermined threshold voltage for the MOS transistors, all of the MOS transistors 11, 21, 31 will be rendered operative. By operative it is meant that the device conducts current readily between source and drain. It should be noted at this point that the gate electrodes of the MOS transistors are designated by a G, the source electrodes are designated by an S, the drain electrodes are designated by a D, and the bulk electrodes are designated by a B.

A second row bus 42 connects together all of the gate electrodes of the MOS transistor 12, 22, 32. The application of a voltage to row bus 42 which exceeds a predetermined voltage will turn on all of the MOS transistors 12, 22, 32. A row bus 43 connects together all the gate electrodes of MOS transistors 13, 23 and 33. The application of a voltage to bus 43 which exceeds the threshold of the three MOS transistors will render them operative.

A first column bus 51 is provided to which are connected all of the drain electrodes, designated as D, of the respective MOS transistors 11, 12 and 13. A second column bus 52 is connected to all of the drain electrodes of the MOS transistors 21, 22 and 23. A third column bus 53 connects together all of the drain electrodes of the MOS transistors 31, 32 and 33. The emitter of each of the photodetectors, for example 15, is connected to the source electrode of its associated MOS transistor, for example 11. The bulk electrode of each of the MOS transistors is connected to the collector of each one of the associated photodetectors and these are all connected to a common load 60. Across the common load is connected the utilization apparatus 62. It should be appreciated, that instead of a common load, if desired, a separate load may be used for each row which is scanned, or for each combined MOS transistor and photodetector which is addressed. The reason a common load is shown is to illustrate how the device may be utilized to generate a train of video signals analogous to the output of a television camera. This, therefore, should not be construed as a limitation upon the use of the invention.

For the purpose of scanning the photodetector array shown, a source of clock signals 64 applies them to a horizontal frequency generator 66, and a vertical frequency generator 68. These respective horizontal and vertical frequency generators constitute dividers which divide down the clock signal to a desired horizontal and vertical scanning frequency. The output of the horizontal frequency generator comprises signals for scanning the rows which are applied to a cyclic counter 70. Each count output of the counter is applied to excite the respective row buses 41, 42 and 43. The output of the vertical frequency generator is applied to the cyclic counter 72 which serves to distribute the vertical frequency signals to the respective column buses 51, 52 and 53.

Assume now that the array of photodetectors is exposed to a scene for which it is desired to generate video signals. Upon the application of a scanning signal to both the cyclic counters energizing row bus 41 and column 51, current can flow from the source through the drain of MOS device 11 and through the photodetector 15 down through the load resistor 60. The amplitude of this current will vary with the excitation of the photodetector 15 which, of course, varies with the amplitude of the light to which it is exposed. While maintaining the row bus 41 energized, the cylic counter 72 energizes the second column bus 52 whereby the current that is caused to flow through the load 60 represents the light intensity upon photodetector 25 instead of the photodetector 15. It will be understood from the foregoing how each one of the columns is energized in turn while the energization is maintained for each row, whereby the scanning action of the photodetectors is effected. A sequence of voltages is generated across the load resistor 60 which represents the scene to which the photodetectors are exposed. The utilization apparatus 62 may be either a display device or any other suitable device for processing the video signal waveform which is generated by the circuitry shown in Figure 1. It should be noted that while sequential selection of rows and columns is described, selection does not necessarily have to be sequential. Selection may be done in any desired sequence. This invention therefore presents a simple arrangement for embodying the image which is being presented to the array.

Figure 2 illustrates, by way of example,

an integrated circuit arrangement for the embodiment of the invention. Each photodetector, such as photodetector 15, has the spade shaped appearance in which there is a p-type base 15p and an n-type emitter, 15e. The row buses, such as 41, are deposited (the process is explained in U.S. Patent No. 2,981,877). The MOS transistor 11 has a source 11S, a channel region 11C, and a drain 11D. The portion of bus 41 deposited over the channel region constitutes the gate. It is insulated from the source and the drain by an oxide layer, not shown. The emitter 15e of the photodetector is connected to the source of the MOS transistor by a deposited conductor 74. Contact is made to the emitter 15e and to the source 11S through holes in the oxide (not illustrated) as is well known in the art. The drain of each MOS transistor is connected in the same way to the column bus, for example 51, of the array. The arrangement shown in Figure 2 may be obtained using well-known integrated circuit techniques.

There has accordingly been described and shown herein a novel, useful and unique arrangement for enabling an array of photoconductors to be scanned. It will be appreciated that while the array is shown for scanning photodetectors, any other two terminal variable impedance device may be used in place of the photodetectors with the array of MOS transistors. Thus, for example, devices such as thermistors may be used whose resistance varies with their temperature. These may be substituted in place of the photodetectors and a video signal may be generated by scanning the array representative of the heat image of the area scanned. Thus, the use of photodetectors should not be construed as a limitation upon the scanning operation of the invention, but rather should be considered by way of illustration.

WHAT WE CLAIM IS:—

1. An image detection arrangement comprising a plurality of detecting devices on which the image is incident, each detecting device being operatively associated with a MOS transistor, the detecting devices and associated MOS transistors being arranged in rows and columns to form an array, means for selectively applying energising potentials to the MOS transistors in the rows and columns to render operative the MOS transistors at the intersections of the selected rows and columns whereby the associated detecting devices are selectively energised as determined by the image pattern and means for deriving outputs from said energised detecting devices.

2. An image detection arrangement as claimed in claim 1, wherein each of said MOS transistors is provided with a gate electrode, a bulk electrode and a pair of electrodes one of which is a drain electrode and the other of which is a source electrode and the associated detecting device is connected between the bulk electrode and one of said pair of electrodes.

3. An image detection arrangement as claimed in claim 2, wherein a separate bus for each row is connected in common to the gate electrodes of all the MOS transistors in the row and a separate bus for each column is connected in common to the other of said pair of electrodes of all the MOS transistors in the column.

4. An image detection arrangement as claimed in claim 2, wherein the bulk electrodes of a row of MOS transistors are connected together and to a common load for all rows, the common load being connected to utilisation apparatus.

5. An image detection arrangement as claimed in any of the preceding claims, and including means for applying the energising potentials successively to the MOS transistors in the rows and columns to render operative successively the MOS transistors at the intersections of the rows and columns.

6. An image detection arrangement as claimed in claim 1 or 2, wherein the detection devices comprise variable impedance devices.

7. An image detection arrangement as claimed in claim 1, 2 or 5, wherein the detecting devices comprise photosensors.

8. An image detection arrangement substantially as described with reference to the accompanying drawings.

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Leamington Spa: Printed for Her Majesty's Stationery Office, by the Courier Press.
—1968. Published by The Patent Office, 25 Southampton Buildings, London, W.C.2,
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