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PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Improvements relating to Semiconductor Circuits

We, TEXAS INSTRUMENTS INCORPORATED, of 6000 Lemmon Avenue, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates broadly to semiconductor circuits and more particularly to a diode AND gate semiconductor circuit.

Many methods and techniques for miniaturizing electronic circuits have been proposed in the past. At first, most of the effort was spent upon reducing the size of the components and packing them more closely together. Work directed toward reducing component size is still going on, but has nearly reached a limit. Other efforts have been made to reduce the size of electronic circuits, such as by eliminating the protective coverings from components, by using more or less conventional techniques to form components of a complete circuit on a single substrate, and by providing the components with a uniform size and shape to permit closer spacings in the circuit packaging therefor.

All of these methods and techniques require a very large number and variety of operations in fabricating a complete circuit. For example, of all circuit components, resistors are usually considered the most simple to form, but when adapted for miniaturization by conventional techniques, fabrication requires at least the following steps:

a. Formation of the substrate
b. Preparation of the substrate
c. Application of terminations
d. Preparation of resistor material
e. Application of the resistor material
f. Heat treatment of the resistor material
g. Protection or stabilization of the resistor

Capacitors, transistors, and diodes when adapted for miniaturization each require at least as many steps in the fabrication thereof. Unfortunately, many of the steps required are not compatible. A treatment that is desirable for the protection of a resistor may damage another element formed on the same substrate, such as a capacitor or transistor, and as the size of the complete circuit is reduced, such conflicting treatments, or interactions, become of increasing importance. Interactions may be minimized by forming the components separately and then assembling them into a complete package, but the very act of assembly may cause damage to the more sensitive components.

Because of the large number of operations required, control over miniaturized circuit fabrication becomes very difficult. To illustrate, many raw materials must be evaluated and controlled, even though they may not be well understood. Further, many testing operations are required and, even though a high yield may be obtained for each operation, so many operations are required that the over-all yield is often quite low. In service, the reliability of a circuit produced by methods of such complexity may also be quite low due to the tremendous number of controls required. Additionally, the separate formation of individual components requires individual terminations for each component. These terminations may eventually become as small as a dot of conductive paint. However, they still account for a large fraction of the usable area or volume of the circuit, and may become an additional cause of circuit failure or rejec-

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tion due to misalignment.

In contrast to the approaches to miniaturization that have been made in the past, the present invention has resulted from a new and totally different concept for miniaturization. This concept and circuit elements made in accordance with this concept are the subject matter of our pending application No. 3633/60 (Serial No. 945,734). It is proposed in said co-pending patent application that miniaturization can best be attained by use of as few materials and operations as possible, and in accordance with the invention disclosed therein, the ultimate in circuit miniaturization is attained using only one material for all circuit elements and a limited number of compatible process steps for the production thereof.

The above is accomplished by utilizing a body of semiconductor material exhibiting one type of conductivity, either N-type or P-type, and having formed therein a diffused region or regions of appropriate conductivity type to form a P-N junction between such region or regions and the remainder of the semiconductor body or, as the case may be, between diffused regions. It is, of course, understood that the P-N junction may be formed by other well known methods, even though diffused junctions are utilized in the preferred embodiment of this invention. According to this invention, all components of a semiconductor circuit are fabricated within the body so characterized by adapting the techniques described in said pending application, together with certain new techniques. It is to be noted that all components of the circuit are integrated into the body of semiconductor material and constitute portions thereof.

The present invention is a semiconductor circuit for providing an output from a plurality of input signals in accordance with a logical function, comprising a wafer of semiconductor material mainly of one type of conductivity, regions of opposite type conductivity material in said wafer forming two spaced apart P-N junction diodes in one portion of said wafer, another portion of said wafer displaying the electrical properties of a bias resistor, a terminal for receiving input signals connected to the opposite conductivity type regions of each of said diodes, and a terminal connected to the portion of said wafer displaying the properties of a bias resistor, away from said diodes, to receive a voltage to bias said diodes in one direction except when input signals of the proper magnitude and polarity received. The concept of shaping, described in detail in our said co-pending patent application, makes it possible in a circuit to obtain the necessary isolation between components and to define the components or, stated differently, to limit the area which is utilized for a given component. Shaping may be accomplished in a given circuit in one or more of several different ways. These various ways include actual removal of portions of the semiconductor material such as rectangular, "L"-shaped, "U"-shaped, etc., selective conversion of intrinsic semiconductor material by diffusion of impurities thereinto to provide low resistivity paths for current flow, and selective conversion of semiconductor material of one conductivity type to conductivity of the opposite type wherein the P-N junction thereby formed acts as a barrier to current flow. In any event, the effect of shaping is to direct and/or confine paths for current flow, thus permitting the fabrication of circuits which could not otherwise be obtained in a single wafer of semiconductor material. As a result, the final circuit is arranged in essentially planar form. It is possible to shape the wafer during processing and to produce by diffusion the various circuit elements in a desired and proper relationship.

An embodiment of the present invention will now be described, by way of example with reference to the accompanying drawing in which:—

Figure 1 is a plan view of a semiconductor circuit according to this invention;

Figure 2 is a schematic diagram of the circuit illustrated in Figure 1; and

Figure 3 is a sectional view taken along lines 3-3 of Figure 1.

Referring now to the drawings, a preferred embodiment of the present invention will be described in detail in order to provide a better understanding of the invention.

With reference to Figure 1, there is shown a ceramic substrate 10. A strip 12 of semiconductor material, preferably a silicon or germanium wafer of P-type conductivity is attached to the substrate 10. Regions 14, 16, 18, and 20 of N-type semiconductor material have been produced in the right-hand portion of strip 12 to form integral P-N junction diodes D_1, D_2, D_3, and D_4. These regions 14, 16, 18, and 20 may be produced, for example, by the method disclosed in the above-mentioned pending application. Ohmic contacts 15, 17, 19, and 21, which may be plated or alloyed contacts, are provided on each of the N-type regions. In Figure 3, there is illustrated a cross sectional view of the typical junction diode D_1 to show the various layers. In forming these junctions, the semiconductor strip may be first subjected to diffusion of a N-type significant impurity material over its entire surface. Then, the N-type semiconductor material may be etched away except in the regions in which the junctions are required. This process forms a raised mesa 24 on each area of the strip 12 in

which a junction is desired.

Returning now to Figure 1, three input leads 26, 28, and 30, an output lead 32 and a bias lead 34 are attached to substrate 10. Bias lead 34 passes beneath the left-hand end of semiconductor strip 12, and is placed in ohmic contact therewith, as by soldering. Wire leads 26a, 28a, 30a, and 32a are connected between their corresponding input and output leads 26, 28, 30, and 32 and junction diode ohmic contacts 15, 17, 19, and 21, respectively. The left-hand portion of strip 12 is shaped to define a resistor R_1 having a desired value, which in one embodiment of the circuit of the present invention may be 16 K, between the point of ohmic contact by bias lead 34 and the juncture with the anode of the junction diode D_1. The shaping of resistor R_1 is accomplished by etching or other means to provide a required length and cross sectional area of the left-hand portion of the strip 12 necessary for that strip to exhibit the required resistance, taking into consideration the resistivity of the material of the strip 12. A positive potential V+, which may be, for example, 12 volts, is applied to lead 34. A thin strip of conducting material 25 it attached to the substrate 10 beneath the semiconductor strip 12, which is in ohmic contact therewith. In this manner, all diode anodes are maintained at approximately the same potential inasmuch as the resistance in the strip 12 of semiconductor material beneath the diodes is effectively shorted out by the conductive strip 25. Alternatively, the same result may be accomplished by forming a suitable region of conducting material on the lower side of strip 12, using well known methods.

The miniature semiconductor circuit of Figure 1 is represented schematically by the circuit diagram shown in Figure 2. Corresponding elements in Figures 1 and 2 have been designated with the same reference numerals. The circuit operation is conventional, and may be easily understood by reference to Figure 2. The circuit functions to perform a logical "AND" operation. When simultaneous positive pulses of sufficient amplitude to back bias the diodes D_1, D_2, and D_3 are applied to the three input leads in opposition to the forward bias provided by the positive potential V+ applied through bias resistor R_1, current will no longer flow through R_1. The full V+ voltage is then applied to D_4 to forward bias it and provide a positive pulse to output lead 32, indicating coincidence of three inputs. If one or more of the diodes D_1, D_2 and D_3 remain forward biased, i.e., do not receive a positive pulse from their inputs, current continues to flow through R_1 to suppress the bias voltage applied to D_4. It is, of course, to be understood that a circuit with two inputs of four or more, rather than only three as shown in Figures 1 and 2, or a circuit which does not utilize the output diode D_4, could easily be fabricated by utilizing the principles of this invention and such variations are within the contemplated scope of this invention.

The described embodiment of this invention provides a miniaturized semiconductor circuit which functions as a diode "AND" gate, which is fabricated from a body of semiconductor material containing a plurality of P-N junctions wherein all components of the diode gate are completely fabricated within the body of semiconductor material, and which is substantially smaller, more compact, and simpler than circuit packages heretofore developed using known techniques.

It must be emphasized here that only one preferred embodiment of this invention has been described above and that other variations and modifications thereof may be made without departing from the scope of this invention which is defined in the appended claims.

WHAT WE CLAIM IS:—

1. A semiconductor circuit for providing an output from a plurality of input signals in accordance with a logical function, comprising a wafer of semiconductor material mainly of one type of conductivity, regions of opposite type conductivity material in said wafer forming two spaced apart P-N junction diodes in one portion of said wafer, another portion of said wafer displaying the electrical properties of a bias resistor, a terminal for receiving input signals connected to the opposite conductivity type regions of each of said diodes and a terminal connected to the portion of said wafer displaying the properties of a bias resistor, away from said diodes, to receive a voltage to bias said diodes in one direction except when input signals of the proper magnitude and polarity are received.

2. A semiconductor circuit according to claim 1 further including a third P-N junction diode in said wafer, spaced from said two diodes and a terminal at which an output signal from said circuit may be obtained connected to the opposite conductivity type regions of the third diode.

3. A semiconductor circuit according to claim 1 or 2 including means to maintain the regions of said one type conductivity of all of said diodes at essentially the same electrical potential.

4. A semiconductor circuit according to claim 2 or claim 3 when appendent to claim 2 in which an "AND" logical function is provided, whereby, when input signals of the proper magnitude and polarity are supplied simultaneously to both of said input terminals to bias said two diodes in the direction opposite to that in which they were

which a junction is desired.

Returning now to Figure 1, three input leads 26, 28, and 30, an output lead 32 and a bias lead 34 are attached to substrate 10. Bias lead 34 passes beneath the left-hand end of semiconductor strip 12, and is placed in ohmic contact therewith, as by soldering. Wire leads 26a, 28a, 30a, and 32a are connected between their corresponding input and output leads 26, 28, 30, and 32 and junction diode ohmic contacts 15, 17, 19, and 21, respectively. The left-hand portion of strip 12 is shaped to define a resistor R_1 having a desired value, which in one embodiment of the circuit of the present invention may be 16 K, between the point of ohmic contact by bias lead 34 and the juncture with the anode of the junction diode D_1. The shaping of resistor R_1 is accomplished by etching or other means to provide a required length and cross sectional area of the left-hand portion of the strip 12 necessary for that strip to exhibit the required resistance, taking into consideration the resistivity of the material of the strip 12. A positive potential V+, which may be, for example, 12 volts, is applied to lead 34. A thin strip of conducting material 25 it attached to the substrate 10 beneath the semiconductor strip 12, which is in ohmic contact therewith. In this manner, all diode anodes are maintained at approximately the same potential inasmuch as the resistance in the strip 12 of semiconductor material beneath the diodes is effectively shorted out by the conductive strip 25. Alternatively, the same result may be accomplished by forming a suitable region of conducting material on the lower side of strip 12, using well known methods.

The miniature semiconductor circuit of Figure 1 is represented schematically by the circuit diagram shown in Figure 2. Corresponding elements in Figures 1 and 2 have been designated with the same reference numerals. The circuit operation is conventional, and may be easily understood by reference to Figure 2. The circuit functions to perform a logical "AND" operation. When simultaneous positive pulses of sufficient amplitude to back bias the diodes D_1, D_2, and D_3 are applied to the three input leads in opposition to the forward bias provided by the positive potential V+ applied through bias resistor R_1, current will no longer flow through R_1. The full V+ voltage is then applied to D_4 to forward bias it and provide a positive pulse to output lead 32, indicating coincidence of three inputs. If one or more of the diodes D_1, D_2 and D_3 remain forward biased, i.e., do not receive a positive pulse from their inputs, current continues to flow through R_1 to suppress the bias voltage applied to D_4. It is, of course, to be understood that a circuit with two inputs of four or more, rather than only three as shown in Figures 1 and 2, or a circuit which does not utilize the output diode D_4, could easily be fabricated by utilizing the principles of this invention and such variations are within the contemplated scope of this invention.

The described embodiment of this invention provides a miniaturized semiconductor circuit which functions as a diode "AND" gate, which is fabricated from a body of semiconductor material containing a plurality of P-N junctions wherein all components of the diode gate are completely fabricated within the body of semiconductor material, and which is substantially smaller, more compact, and simpler than circuit packages heretofore developed using known techniques.

It must be emphasized here that only one preferred embodiment of this invention has been described above and that other variations and modifications thereof may be made without departing from the scope of this invention which is defined in the appended claims.

WHAT WE CLAIM IS:—

1. A semiconductor circuit for providing an output from a plurality of input signals in accordance with a logical function, comprising a wafer of semiconductor material mainly of one type of conductivity, regions of opposite type conductivity material in said wafer forming two spaced apart P-N junction diodes in one portion of said wafer, another portion of said wafer displaying the electrical properties of a bias resistor, a terminal for receiving input signals connected to the opposite conductivity type regions of each of said diodes and a terminal connected to the portion of said wafer displaying the properties of a bias resistor, away from said diodes, to receive a voltage to bias said diodes in one direction except when input signals of the proper magnitude and polarity are received.

2. A semiconductor circuit according to claim 1 further including a third P-N junction diode in said wafer, spaced from said two diodes and a terminal at which an output signal from said circuit may be obtained connected to the opposite conductivity type regions of the third diode.

3. A semiconductor circuit according to claim 1 or 2 including means to maintain the regions of said one type conductivity of all of said diodes at essentially the same electrical potential.

4. A semiconductor circuit according to claim 2 or claim 3 when appendent to claim 2 in which an "AND" logical function is provided, whereby, when input signals of the proper magnitude and polarity are supplied simultaneously to both of said input terminals to bias said two diodes in the direction opposite to that in which they were

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biased by said bias voltage, an output signal is provided at said output terminal.

5. A semiconductor circuit according to any of the preceding claims, in which said semiconductor wafer is mounted on an insulating substrate.

6. A semiconductor circuit according to claim 2 and any of claims 3 to 5 in which a relative low standing forward bias voltage is applied to all of said diodes through said bias resistor, and the input signals are of such magnitude and polarity that their simultaneous application to each of said input terminals will reverse bias said two diodes and apply a relatively high forward bias to said third diode to cause a relatively high voltage to appear at said output terminal.

7. A semiconductor circuit substantially as hereinbefore described with reference to Figs. 1 and 3 of the accompanying drawing.

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