

RISC-V INSTRUCTION SET SHIFT INSTRUCTION IMPLEMENTATION CIRCUIT

ABSTRACT

The invention relates to the technical field of integrated circuits, in particular to a RISC-V instruction set shift instruction realization circuit. The circuit is integrated with a shift module. The shift module is composed of a left shifter, a right shifter and a subtracter. When the instruction is emitted from the instruction cache, it enters the decoding module to complete the instruction decoding, and the decoding information and operands enter the shift module, and the left shifter is used to complete the left shift instruction. The right shifter completes the right shift instruction, and with the help of the subtracter is responsible for providing the left shifter and the right shifter with shift distance operands, and the output result is submitted after the operation is completed, and the execution of this instruction is completed. All the shift operation instructions contained in the *riscv* architecture instruction set are supported, and the timing is easy to converge, so a higher dominant frequency can be obtained. It is especially suitable for architecture design in pursuit of high-performance CPU.

(The most illustrative figure is FIG 1)