

ABSTRACT

A vertical memory device including: a substrate including a first and second regions; gate electrodes spaced apart from each other in a first direction, each of the gate electrodes extending in a second direction on the first and second regions, and the gate electrodes are stacked on the second region; a channel extending in the first direction on the first region, the channel extending through the gate electrodes; a first conductive structure on an end portion of a first gate electrode, the end portion on the second region, the first gate electrode being disposed at a lowermost level; and a second conductive structure spaced apart from the first conductive structure in the second direction on the second region, the second conductive structure not overlapping the first gate electrode in the first direction and being disposed at a height different from that of the first conductive structure.

FIG. 2