

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
23 June 2005 (23.06.2005)

PCT

(10) International Publication Number
WO 2005/057423 A3

(51) International Patent Classification:
G06F 17/14 (2006.01)

(21) International Application Number:
PCT/US2004/040498

(22) International Filing Date:
3 December 2004 (03.12.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/527,196 5 December 2003 (05.12.2003) US

(71) Applicant (for all designated States except US): **QUALCOMM Incorporated** [US/US]; 5775 Morehouse Drive, San Diego, California 92121 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **KRISHNAMOORTHY, Raghuraman** [IN/US]; 8730 Costa Verde Boulevard, #2302, San Diego, California 92122 (US). **GANAPATHY, Chinnappa K.** [IN/US]; 12055 Mil Pitrero Road, San Diego, California 92128 (US).

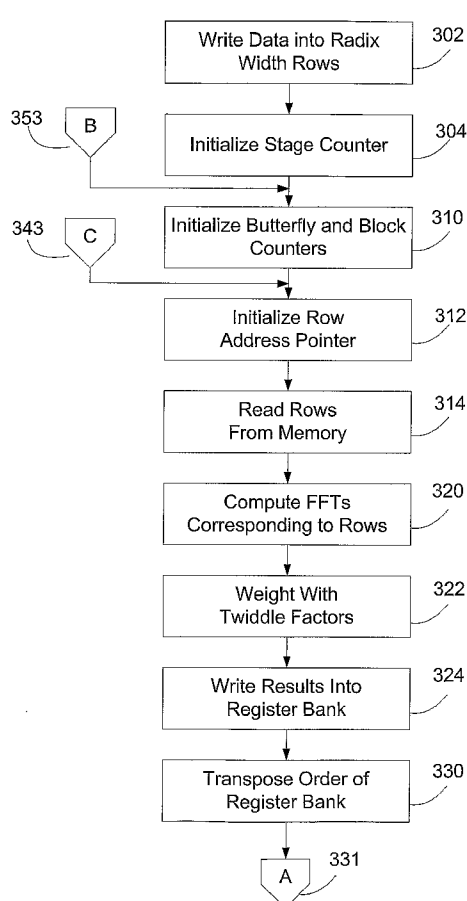
(74) Agents: **WADSWORTH, Philip R.** et al.; 5775 Morehouse Drive, San Diego, California 92121 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: FFT ARCHITECTURE AND METHOD



(57) Abstract: A Fast Fourier Transform (FFT) hardware implementation and method provides efficient FFT processing while minimizing the die area needed in an Integrated Circuit (IC). The FFT hardware can implement an N point FFT, where $N = rn$ is a function of a radix (r). The hardware implementation includes a sample memory having N/r rows, each storing r samples. A twiddle factor memory can store k twiddle factors per row, where $0 < k < r$ represents the number of complex twiddle multipliers available. An FFT module reads r rows from memory, performs an r-point complex FFT on the samples, followed by twiddle multiplication, and writes the results into an $r \times r$ register bank. The contents of the register bank are written in transposed order back to the sample memory. This operation is repeated N/r^2 times for each stage and then repeated for n- stages to produce the N point FFT.

**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:

1 June 2006

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.