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"Improvements in substrate structures"

The present invention relates to a substrate structure with a high thermal conductivity and high electrical insulation properties, a process of fabricating the substrate, and a semiconductor device using it.

A substrate onto which a semiconductor pellet is to be bonded must be made of a material with excellent thermal radiation properties. The substrate referred to hereinafter includes the base of a package to which a pellet is die-bonded, and the invention is directed to all substrates that have pellets bonded thereto. The alumina substrates used as substrates in the prior art have a low thermal conductivity. This makes it impossible to sufficiently dissipate the large quantity of heat generated within the pellets.

The main properties required of a substrate or its material are: (1) high electrical insulation properties; (2) a high thermal conductivity,

(3) a coefficient of thermal expansion close to that of the semiconductor pellet (which is usually of silicon); and (4) a high mechanical strength.

A sintered structure of silicon carbide containing a small quantity of beryllium has been noted as a substrate material which satisfies those requirements well. The sintered silicon carbide structure has a mechanical strength of 55 kg/mm^2, measured as three-point bending strength. This value is at least twice that of alumina. The sintered silicon carbide structure also has very good properties (1) to (3), (see above) as tabulated in Table 1, for example. The electrically insulating substrate structure made of silicon carbide containing a little beryllium is disclosed in detail in our Japanese Patent Publication Nos. 66063/1981 and 2591/1982.

Table 1 Characteristics

	Thermal Conductivity (Cal/cm·S·°C)	Coefficient of Thermal Exapnsion (x 10^{-7}/°C)	Electric Resistivity (Ω·cm)
S.C.	0.65	37	4×10^{15}
Alumina	0.05	67 to 75	$>10^{14}$
Aluminium	0.56	175	2.7×10^{-6}
Silicon	0.30	35 to 40	-

Note: "S.C." means "Silicon carbide with a little Beryllium.

The silicon carbide containing a little beryllium is a chemical compound of carbon (C) and silicon (Si) with excellent covalent bonding properties. In order to ensure sintering at a high density, therefore, a hot-pressing method at a very high temperature and under high pressure must be used. As a result, the prior art has been able to provide only a simple structure such as a simple plate at the best.

A substrate for moulding with a high degree of integration must sometimes be formed with through holes so as to increase the number of output terminals. A typical example of this type is a pin grid array package. The through holes are formed so as to extend normal to one main face of the substrate onto which the pellet is bonded, to the other main face parallel to the first face. In other words, the through holes extend through the substrate in the depthwise direction thereof. The forming of through holes in a substrate made of silicon carbide containing a little beryllium is very difficult.

It is an object of the present invention to provide a substrate structure which has excellent

thermal conductivity, and electrical insulation properties, which is suitable for a high degree of integration, and which has wiring formed therein in the depthwise direction thereof.

According to a first aspect of the present invention there is provided a substrate structure consisting of a hot-pressed sintered plate of silicon carbide based material with first and second main faces, wherein said sintered plate contains a plurality of wires which extend between said first and second main faces so that the two ends of each wire are exposed to the outside at the first and second main faces, respectively. The substrate thus fabricated can have a high mechanical strength, a high thermal conductivity, high electrical insulation properties, and a coefficient of thermal expansion similar to that of the semiconductor pellet to which it is to be bonded (and which pellet is normally of silicon).

Preferably the sintered structure is made of silicon carbide containing a little beryllium, and prepared by a hot-press method.

The following steps may be used to fabricate the substrate structure. Parallel wires extending in one direction are formed on the surface of a flat preform made of a powder of silicon carbide containing a little beryllium oxide. A block formed by hot-pressing together a stack of the preforms is sliced in a direction perpendicular to that in

which the wires extend, to form substrates.

The substrate structure has a wiring layer formed on either or both of main faces. The wiring layer is prepared by photolithography. The wiring layer thus prepared has a laminated wiring structure in which insulating layers and metal layers are laid alternately. Pellets are bonded onto one of the main faces, and leads are mounted onto the other main face. The silicon carbide containing a small quantity of beryllium, i.e., the hot-pressed block, contains 0.1 to 3.5% by weight beryllium. The raw material of the silicon carbide should contain no more than 0.1% by weight aluminium, and no more than 0.1% by weight boron. It is preferable that there is no aluminium or boron contained therein. The raw silicon carbide material should not contain more than 0.4% by weight excess (or free) carbon. The beryllium is added in the form of beryllium oxide to the powdered silicon carbide. The hot-pressed block will contain 0.1 to 3.5% by weight beryllium if 0.5 to 14% by weight beryllium oxide is added. The hot-pressing operation is conducted at a temperature of between 1,850 to 2,500°C. As a result, the sintered structure has a density of at least 90% of the theoretical value for silicon carbide.

According to a second aspect of the invention, there is provided a process of manufacturing a substrate including the steps of: (a) preparing a powder of a material for a sintered substrate; (b) moulding said powder into a plurality of preforms of identical flat shape, each having two surfaces; (c) printing the surfaces of selected said preforms with wiring in a stripe form; (d) piling up the printed preforms so that most of the wiring printed on one of said preforms is covered with another preform; (e) hot-pressing the piled-up preforms into a block; and (f) cutting the hot-pressed block along a plane crossing all of said wiring to form a plurality of substrate structures each having first and second main faces with formed therein a plurality of wires which extend between said first and second main faces such that the two ends of said wires are exposed to the outside at said first and second main faces, respectively.

The present invention will now be described in greater detail by way of examples with reference to the accompanying drawings in which identical reference numerals indicate identical parts and portions:-

Figures 1 to 6 are perspective views of consecutive steps in one preferred form of process of manufacturing a substrate structure;

Figure 7 is a perspective view of another example of the process of manufacture of the substrate structure;

Figure 8 is an enlarged section of an example of part of a substrate in which wiring layers are formed on the substrate structure;

Figure 9 is a section through one embodiment of the semiconductor device using the substrate structure according to the present invention;

Figure 10 is a section through another embodiment of the semiconductor device using the substrate structure according to the present invention; and

Figure 11 is a section through still another embodiment of the semiconductor device using the substrate structure according to the present invention.

Referring first to Figures 1 to 6, a small quantity of powdered beryllium oxide (BEO) is mixed as a sintering assistant with powered silicon-carbide (SiC). The composition of the powder mixture is disclosed in detail in Japanese Patent Publication No. 2591/1982, referred to above. This powder mixture is preformed by a press using a mould. This preforming step is conducted under a pressure of 100

to 500 kg/cm^2 at room temperature. A resultant preform 1 has the plate-shaped form shown in Fig. 1. In this state, the preform 1 has not yet acquired the various characteristics tabulated in Table 1.

In the next step, as shown in Fig. 2, the surface of the preform 1 is printed with the desired number of metallized wires (or wiring layers) 2 in stripes arranged in one direction. The well-known screen printing technique is used in this step. Each of the wires 2 has a width of 100 μm and a thickness of 10 μmm, for example. In this embodiment, zirconium boride (ZrB_2), which has excellent bonding properties with silicon carbide, is used as the material for the wires 2. The resistance of ZrB_2 is about 10^{-5} Ω·cm. ZrB_2 may be replaced by tantalum boride (TaB) whose resistance is about 10^{-4} Ω·cm. These materials do not deteriorate even if subjected to the hot-pressing operation that will be described below.

After that, a desired number of preforms 1 of identical shape and formed with wiring 2 are laid over each other, as shown in Fig. 3. For example, the number of the overlaid preforms can be selected so that the substrate structure according to the present invention can have a roughly square face

onto which pellets are bonded. The resultant laminated structure is hot-pressed by a vacuum hot-press, not shown. The hot-pressing conditions are a temperature of 2050°C under a pressure of 10^{-4} Torr, and a pressure of 290 kg/cm^2, for example. Argon, helium, or nitrogen is used as the gas of the atmosphere. As a result, as shown in Fig. 4, a hot-pressed block 3 is prepared in which the wiring 2 is embedded as internal wires extending in one direction. Of the preforms 1 laminated with their wiring 2 facing upward, the uppermost preform 1 used can preferably have no wiring 2. The hot-pressed block 3 has a construction in which wires 2 are exposed to the outside only at the two end faces thereof, as shown in Fig. 4. This structure is convenient for subsequent handling. This hot-pressed block 3 can have the excellent properties tabulated in Table 1.

The preforming and hot-pressing conditions used may be those disclosed in Japanese Patent Publication No. 2591/1982. (a temperature of 1,850 to 2,500°C, and a pressure of 100 to 300 kg/cm^2). However, the preforming conditions can be changed within ranges that will raise no problems in handling. The hot-pressing conditions are

preferably those disclosed in the present embodiment.

Next, as shown in Fig. 5, the hot-pressed block 3 is sliced (or cut) at right angles with respect to the wiring 2 by a diamond wheel or the like, to a predetermined thickness, e.g., 0.5 to 2 mm. The slicing means used may be a laser or an electron beam.

By repeatedly slicing the hot-pressed block 3, a plurality of substrate structures 4 are fabricated, one of which is shown in Fig. 6. The substrate structure 4 has two main faces which extend parallel to each other and at which the cut ends of the wires 2 are exposed to the outside. One of these main faces provides a surface for bonding pellets thereon, whereas the other provides a surface for the connection of leads (pins). The wires 2 extend through the substrate structure 4 in a direction connecting the two main faces, namely, in the depthwise direction of the substrate structure 4.

In order to fabricate the substrate structure 4, the process shown in Fig. 7 may be used instead of that shown in Fig. 3. The process of Fig. 7 is characterized in that the metalized wiring 2 is

formed both on one of the main faces of the preform 1, and on the other main face which extends parallel to the former. Each of the wires 2 has a width of 50 μm and a thickness of 10 μm, for example. When the preforms 1 are overlaid, the corresponding wires 2 formed on opposite side faces are juxtapositioned to each other. For this purpose, corresponding wires 2 are each formed in an identical shape on different preforms 1. The wires 2 thus overlaid are hot-pressed into an integrated structure, so that each of the laminated wires 2 has a thickness of 20 μm. This is effective for reducing the electrical resistances of the wires 2 extending through the substrate structure 4.

This substrate structure 4 is composed mainly of silicon carbide containing a small quantity of beryllium, so that it has excellent thermal radiation and electrical insulation properties, and has a coefficient of thermal expansion little different from that of silicon but has a higher mechanical strength.

Therefore, the above properties can be utilized effectively if the substrate structure 4 is used as an electrically insulating substrate for a semiconductor device such as a semiconductor

power module or a large scale integrated circuit. Moreover, the substrate structure 4 is excellent as a substrate for bonding, because the wiring 2 is integrated as internal wiring within a sintered structure of silicon carbide containing a small amount of beryllium by a hot-pressing operation. Thus it is possible to bond large pellets to a high density by adding the step of forming the cut faces with fine wiring by photolithography, and by bonding thereto pellets and leads.

Since the present embodiment uses a hot-pressing technique, the press-forming can be conducted at low cost by making use of a large pressing mould. Moreover, a number of substrate structures 4 can be fabricated by a single operation. Because of the hot-pressing operation, internal wiring is integrated within the substrate structure, and bubbles within the substrate structure are eliminated. As a result, the faces do not cut across bubbles in the substrate structure, so that very few holes are left by bubbles, and the surface roughness of the cut faces is very small. Either or both of the cut faces can be formed with the fine wiring by photolithography. Since the internal wiring and the substrate

structure are integrated, no gas can leak through their interfaces. As a result, the substrate structure 4 has an excellent hermetic seal.

The substrate structure 4 can be used as an electrically insulating substrate by printing both or one of its cut faces with wiring and sintering it.

Fig. 8 is an enlarged section of part of a substrate in which a multi-layered wiring layer is formed by photolithography on the substrate structure 4 according to the present invention. In a wiring layer 5 of this substrate, copper layers 6 are bonded over the end faces of the wires 2 which are formed to extend in the depthwise direction through the substrate structure 4. On top of the copper layers 6, two sets of copper layers 7 and 8 are bonded consecutively in that order. Two insulating layers 9 and 10 of SiO_2 are formed over the substrate structure 4. A pellet 12 is bonded to the uppermost copper layers 8 by bump electrodes 11 of Pb-Sn solder. The copper layers 6, 7 and 8 are deposited over all the surface by electron beam vacuum evaporation, for example, and a desired wiring configuration is attained by the use of photolithography. The SiO_2 layers 9 and 10 are

deposited over all the surface by chemical vapour deposition (CVD), and desired contact holes are then formed by photolithography. The wiring layer 5 is formed by repeating those two steps. The copper layers can be formed by other techniques such as screen printing or masked vapour evaporation. The SiO_2 layers can be formed by other techniques such as plasma CVD or sputtering.

Before the copper layers 6 are formed, the main face of the substrate structure 4 onto which the pellet is to be bonded can be polished to provide a mirror surface, or the main face could be coated thinly with glass. These can further facilitate the application of photolithography.

In the substrate shown in Fig. 8, the heat generated within the pellet 12 is transferred through the solder bump electrodes 11 to the substrate structure 4 mainly through the copper layers. Since copper has an excellent heat conductivity, the generated heat is transferred promptly to the substrate structure 4. As a result, the heat generated within the pellet 12 is radiated efficiently from the substrate structure 4.

Even if the silicon pellet 12 and the substrate

structure 4 expand due to heat, the peeling of the solder bump electrodes 11 can be prevented. This is due to the fact that they have substantially equal coefficients of thermal expansion, as tabulated in Table 1. As a result, it is possible to eliminate damage caused by thermal expansion, which is a major problem in the bonding method using solder bumps according to the prior art. In Fig. 8, the copper can be replaced by another metal such as aluminium, gold, a silver-palladium alloy, or nickel. The SiO_2 layers can be replaced by other insulating films having a small coefficient 3.0-3.5 $x10^{-6}$/°C of thermal expansion, such as films of phosphosilicate glass or borosilicate glass. The wiring layer 5 may be constructed of a laminated structure containing three or more conducting layers.

If the leads are bonded onto the opposite end faces of the wires 2 (i.e., the lower end faces in Fig. 8), which are on the face of the substrate structure 4 opposite to the wiring layer 5, then the substrate structure 4 can be used as a base of a package for a semiconductor device.

Fig. 9 is a section through one embodiment of the semiconductor device using the substrate structure 4 thus far described.

In the semiconductor device according to the present embodiment, the upper face of the substrate structure 4 has a single-layered wiring layer 16 composed of copper layers 13 and 14 electrically bonded onto the upper ends of the wires 2, and an insulating layer 15 of SiO_2. Two pellets 18 are bonded onto the copper layers 14 by solder bump electrodes 17. This example shows a highly integrated, multichip module. A cap 19, made of either silicon carbide containing a small amount of beryllium so that it has the identical composition to that of the substrate structure 4 or mullite, is bonded over the substrate structure 4 by sealant 20 of glass or epoxy resin. The pellets 18 are sealed hermetically by the cap 19.

Over the lower face of the substrate structure 4, a multi-layered wiring layer 26 is formed which is composed of copper layers 21, 22, and 23 connected electrically to the lower ends of the wires 2, and two insulating layers 24 and 25 of SiO_2. Leads 27 are bonded to the lower face of the outermost copper layers 23 of those copper layers 21, 22, and 23 by a bonding agent 28. If solder is used as the bonding agent 28, the leads 27 (pins) are made of a material belonging to the copper

group. If silver solder is used as the bonding agent 28, the leads 27 are made of Kovar(R.T.M.). The leads 27 connect the pellets 18 electrically with the outside by way of the wiring layer 16, the wires 2, and the wiring layer 26.

A cooling pipe 29 is arranged so as to surround the sides of the substrate structure 4. The cooling pipe 29 is made of a material with a small coefficient of thermal expansion, such as molybdenum or an iron-nickel alloy. The cooling pipe 29 is supplied with a cooling medium such as water, Freon, liquid nitrogen, or liquid helium which flows therein. Heat conducted from the pellets 18 through the wiring layer 16 and the substrate structure 4 is radiated more efficiently by the action of such a cooling pipe 29. In order to mount the cooling pipe 29, the substrate structure 4 is made as thin as about 5 mm.

In the embodiment being described, heat generated within the pellets 18 is transferred to the substrate structure 4 through copper layers which have an excellent conductivity. The wiring layer 16 is especially able to transfer heat because it is a single layer. In addition to this, the solder bump electrodes 17 are positioned over the copper

layers 13. In other words, the solder bump electrodes 17 are embedded in contact holes so that they are in contact with the substrate structure 4 only through the copper layers 13 and 14. As a result, heat is transferred much better. The heat transferred to the substrate structure 4 is then transferred to the side faces thereof and is forcibly radiated by the action of the cooling pipe 29. Since the substrate structure 4 has an excellent thermal conductivity, the heat transferred to the substrate structure 4 is dissipated sufficiently by the cooling operation at its side faces alone. Heat is also dissipated from the cap 19. The SiO_2 layer 15 forming the wiring layer 16 and the sealant 20 are made much thinner than the cap 19. Although they both have low thermal conductivities, heat is also transferred to the cap 19. This cap 19 also contributes to heat dissipation because it is made of a material with an excellent thermal conductivity.

According to the present embodiment, the dissipation of heat generated within the pellets 18 can be efficiently conducted. Incidentally, when there is no particular need for heat dissipation from the pellets 18, the wiring layer 16 on the

upper side of the substrate structure 4 can have a multi-layered construction.

As has been described hereinbefore, moreover, the solder bump electrodes can be prevented from being damaged. Since the substrate structure 4 has a high mechanical stregnth, the strength of the package can be improved. Since the adhesion between the substrate structure 4 and the wiring 2 is excellent, furthermore, the air-tightness of the seal can be improved.

Fig. 10 is a section through another embodiment of the semiconductor device using the substrate structure thus far described.

This embodiment shows, by way of example, a single chip structure equipped with only one pellet 18. A cap 19a is formed with radiator fins 30 thereon. The cooling pipe surrounding the substrate structure 4 can be provided, although it is not shown, as in the embodiment of Fig. 9. Sealing of the cap 19a is effected by a structure in which a metal layer 33 is sandwiched between metal layers 31 and 32. The metal layers 31 and 32 are made of Ti which has an excellent adhesion to the oxide film. The metal layer 33 is made of a gold-tin alloy for adhering to the Ti. The leads 27 are

bonded directly to the lower ends of the wires 2 by the bonding agent 28.

In the present embodiment, heat generated within the pellet 18 is radiated from the substrate structure 4 and the radiator fins 30. The transfer of the heat to the substrate structure 4 is identical to that of the embodiment of Fig. 9. The heat transfer to the cap 19a and the radiator fins 30 is improved over that of the embodiment of Fig. 9. Since metal layers 31, 32, and 33 are used as the seal instead of the glass and the epoxy resin of the previous embodiment, more heat is transferred to the cap 19a. The cap 19a and the radiator fins 30 contribute a great deal to the heat radiation because they are made of a material which has an excellent thermal conductivity, and an identical composition to that of the substrate structure 4.

In the present embodiment, as in the embodiment of Fig. 9, it is possible to prevent damage to the solder bump electrodes and improve the package strength and the air-tightness of the package.

The cap 19a and the radiator fins 30 are attached to each other by means of adhesive after they have been formed separately. Alternatively,

the bulk of a sintered structure can be worked by a laser.

Fig. 11 shows still another embodiment of the semiconductor device, in which the bonding pads (not shown) of the pellet and the leads to the wiring of the substrate structure are connected by wires.

At the central portion of the substrate structure 4, a copper layer 13a is located which is formed simultaneously with the copper layers 13. The pellet 18 is bonded over the copper layer 13a by a gold-silicon eutectic layer 34. Bonding wires 35 provide connections between the copper layers 14 and bonding pads on top of the pellet 18. The number of output terminals can be increased because the copper layers 14 can be formed by photolithography. The bonding wires 35 are made of aluminium and are bonded by an ultrasonic method. The cap 19a and the substrate structure 4 are connected to each other by metal layers 13b, 36, and 37. The metal layer 13b is a copper layer formed simultaneously with the copper layers 13. The metal layer 37 is of a gold-tin alloy, and the metal layer 36 is of copper. A cooling pipe can be provided as in the embodiment of Fig. 9.

In the present embodiment, the heat generated within the pellet 18 is dissipated mainly from the substrate structure 4. In the same way as in the embodiment of Fig. 10, heat is also dissipated from the radiator fins 30. Since the area of the pellet 18 in contact with the substrate structure 4 is large, the transfer of heat to the substrate structure 4 is excellent.

In the present embodiment, damage such as the peeling off of pellets can be prevented. As in the embodiment of Fig. 9, it is possible to improve the strength and the air-tightness of the package.

The present invention is not limited to the embodiments thus far described, but can be modified in a number of ways. For example, the shape (pattern) of the wiring 2 on the preform 1, or the direction of cutting the hot-pressed block 3 is not limited to those of the above embodiments. The wiring 2 may also be made of tungsten, molybdenum or tantalum.

Thus, according to the present invention, it is possible to easily fabricate a substrate structure which has excellent in thermal radiation and electrical insulation properties, and which is provided with internal wiring.

CLAIMS.

1. A substrate structure consisting of a hot-pressed sintered plate of silicon carbide based material with first and second main faces, wherein said sintered plate contains a plurality of wires which extend between said first and second main faces so that the two ends of each wire are exposed to the outside at the first and second main faces, respectively.

2. The substrate structure according to claim 1, wherein said sintered plate contains 0.1 to 3.5% by weight beryllium.

3. The substrate structure according to claim 2, wherein said wires are made of zirconium boride.

4. The substrate structure according to claim 3, wherein said zirconium boride is ZrB_2.

5. The substrate structure according to claim 2, wherein said wires are made of tantalum boride.

6. The substrate structure according to claim 5, wherein said tantalum boride is TaB.

7. The substrate structure according to any one of the preceding claims, wherein at least one of said first and second main faces has a mirror surface.

8. The substrate structure according to any one of the preceding claims 1 to 6, wherein said first and second main faces are oriented parallel to each other, and normal to said wires.

9. A process of manufacturing a substrate including the steps of:

(a) preparing a powder of a material for a sintered substrate;

(b) moulding said powder into a plurality of preforms of identical flat shape, each having two surfaces;

(c) printing the surfaces of selected said preforms with wiring in a stripe form;

(d) piling up the printed preforms so that most of the wiring printed on one of said preforms is covered with another preform;

(e) hot-pressing the piled-up preforms into a block; and

(f) cutting the hot-pressed block along a plane crossing all of said wiring to form a plurality of substrate structures each having first and second main faces with formed therein a plurality of wires which extend between said first and second main faces such that the two ends of said wires are exposed to the outside at said first and second main faces, respectively.

10. The process of manufacturing a substrate according to claim 9, wherein said powder is of silicon carbide containing 0.5 to 14% by weight beryllium oxide, so that said substrate structures are made of silicon carbide containing 0.1 to 3.5% by weight beryllium.

11. The process of manufacturing a substrate according to claim 9 or 10, wherein the cutting in step (f) is conducted along a plane normal to said wires so that said substrate structures have a predetermined thickness.

12. The process of manufacturing a substrate according to any one of the preceding claims 9 to 11, wherein said wiring is made of zirconium boride.

13. The process of manufacturing a substrate according to claim 12, wherein said zirconium boride is ZrB_2.

14. The process of manufacturing a substrate according to any one of the preceding claims 9 to 11, wherein said wiring is made of tantalum boride.

15. The process of manufacturing a substrate according to claim 14, wherein said tantalum boride is TaB.

16. The process of manufacturing a substrate according to any one of the preceding claims 9 to 15, wherein step (c) includes a sub-step (h) of forming wiring of identical shape on both a first surface of a first preform and a second surface of a second preform, selected from said preforms, and wherein step (d) includes a sub-step (i) of making said first and second surfaces face each other and integrating said wiring of identical shape.

17. The process of manufacturing a substrate according to any one of the preceding claims 9 to 16, further including a step (j) of polishing at least one of said first and second main faces of said substrate structure to form a mirror surface.

18. The process of manufacturing a substrate according to any one of the preceding claims 9 to 17, further including a step (k) of forming by photo-lithography on at least one of said first and second main faces a wiring layer which consists of: a plurality of conducting layers of which the lowermost one is connected to said wiring; and a plurality of insulating layers each formed between adjacent conducting layers and having a plurality of contactholes for providing connections between different conducting layers.

19. A semiconductor device including:

(a) a substrate structure constructed of a hot-pressed sintered plate of silicon carbide based material with first and second main faces;

(b) a plurality of wires each formed in said sintered plate so as to extend between said first and second main faces so that the two ends thereof are exposed to the outside at said first and second main faces, respectively;

(c) a wiring layer formed on at least said first main face and consisting of: a plurality of conducting layers of which the lowermost one is connected

to said wires at corresponding terminals thereof and the uppermost one is connected to a semiconductor pellet; with at least one insulating layer formed between adjacent ones conducting layers, said conducting layers being connected to each other through a plurality of contact holes formed in said insulating layer, said conducting layers and said insulating layer being laid alternately one over the other; and

(d) at least one semiconductor pellel bonded onto said first main face and connected electrically to said uppermost conducting layer overlying the first main face.

20. The semiconductor device according to claim 19, wherein said sintered place is made of silicon carbide containing 0.1 to 3.5% by weight beryllium.

21. The semiconductor device according to claim 19 or 20, wherein said wires are made of zirconium boride.

22. The semiconductor device according to claim 21, wherein said zirconium boride is ZrB_2.

23. The semiconductor device according to claim 19 or 20, wherein said wires are made of tantalum boride.

24. The semiconductor device according to claim 23, wherein said tantalum boride is TaB.

25. The semiconductor device according to any one of the preceding claims 19 to 24, wherein the first and second main faces are oriented parallel to each other, normal to said wires.

26. The semiconductor device according to any one of the preceding claims 19 to 24, wherein at least said first main face has a mirror surface.

27. The semiconductor device according to any one of the preceding claims 19 to 24, wherein said semiconductor pellet is connected electrically to said uppermost conducting layer overlying said first main face by bump electrodes made of solder.

28. The semiconductor device according to claim 27, wherein said bump electrodes are embedded in said contact holes.

29. The semiconductor device according to any one of the preceding claims 19 to 28, wherein said wiring layer includes said lowermost conducting layer, said uppermost conducting layer, and said insulating layer sandwiched therebetween, and wherein said contact holes are positioned over the terminals of said ends of said wires.

30. The semiconductor device according to claim 19 or 20, wherein electrical connections of said semiconductor pellet are effected by bonding wires.

31. The semiconductor device according to claim 30, wherein said wires are formed in said first main face except for the central portion thereof so that the ends thereof exposed at said first main face are arranged in the form of a matrix, said wiring layer is formed over said first main face except for said central portion, and said semicondcutor pellet is bonded onto said central portion of said first main face by a gold-silicon eutectic layer.

32. The semicondcutor device according to claim 31, wherein said semiconductor pellet is bonded to a conducting layer formed over said central portion of said first main face simultaneously with the formation of said lowermost conducting layer.

33. The semiconductor device according to claim 19 or 20, wherein a wiring layer is formed over each of said first and second main faces.

34. The semiconductor device according to claim 33, wherein said wiring layer on said first main face includes said lowermost conducting layer, said uppermost conducting layer, and said insulating layer sandwiched therebetween.

35. The semiconductor device according to claim 33 or 34, further comprising a plurality of leads mounted onto said second main face through said uppermost conducting layer of said wiring layer of said second main face by lead-connecting metal layers.

36. The semiconductor device according to claim 19 or 20, wherein said wiring layer is formed on said first main face.

37. The semiconductor device according to claim 36, wherein said wiring layer on said first main face includes said lowermost conducting layer, said uppermost conducting layer, and said insulating layer sandwiched therebetween.

38. The semiconductor device according to claim 36, further including a plurality of leads mounted onto said second main face of said substrate structure by lead-connecting metal layers.

39. The semiconductor device according to claim 38, wherein said leads are arranged on extensions of said wires.

40. The semiconductor device according to any one of the preceding claims 19 to 39, further including a cooling pipe mounted around the side faces of said substrate structure other than said first and second main faces, and provided with a cavity for allowing a liquid to flow therethrough.

41. The semiconductor device according to any one of the preceding claims 19 to 40, further including a cap mounted over said first main face by means of a seal which hermetically seals said semiconductor pellet.

42. The semiconductor device according to claim 41, wherein said seal consists of a first titanium layer, a gold-tin alloy layer, and a second titanium layer laid over each other consecutively, of which said first titanium layer is formed over said insulating layer.

43. The semiconductor device according to claim 41, wherein said seal consists of a first copper layer, a gold-tin alloy layer, and a second copper layer laid over each other consecutively, of which said first copper layer is formed over said substrate structure.

44. The semiconductor device according to any one of the preceding claims 41 to 43, wherein said cap is made of a material identical to that of said substrate structure.

45. The semiconductor device according to any one of the preceding claims 41 to 44, further including a plurality of radiator fins formed on said cap.

46. The semiconductor device according to claim 45, wherein said radiator fins are made of a material identical to that of said substrate structure and said cap, and are integrated with said cap.

47. A substrate structure constructed substantially as herein described with reference to and as illustrated in the accompanying drawings.

48. A process of manufacturing a substrate substantially as herein described with reference to Figures 1 to 6 or Figure 7 of the accompanying drawings.

49. A semiconductor device constructed substantially as herein described with reference to and as illustrated in any one of Figures 8 to 11 of the accompanying drawings.