SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERCONNECT STRUCTURE FOR ENCAPSULATED DIE HAVING PRE-APPLIED PROTECTIVE LAYER

Field of the Invention

The present invention relates in general to semiconductor devices and, more particularly, to a wafer level chip scale package (WLCSP) with interconnect structure, in which a semiconductor die is prepared from a semiconductor wafer having protective layer on the front or active side of the wafer.

Background of the Invention

Semiconductor devices are found in many products in the fields of entertainment, communications, networks, computers, and household markets. Semiconductor devices are also found in military, aviation, automotive, industrial controllers, and office equipment. The semiconductor devices perform a variety of electrical functions necessary for each of these applications.

The manufacture of semiconductor devices involves formation of a wafer having a plurality of die. Each semiconductor die contains hundreds or thousands of transistors and other active and passive devices performing a variety of electrical functions. For a given wafer, each die from the wafer typically performs the same electrical function. Front-end manufacturing generally refers to formation of the semiconductor devices on the wafer. The finished wafer has an active side containing the transistors and other active and passive components. Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then

packaging the die for structural support and environmental isolation.

One goal of semiconductor manufacturing is to produce a package suitable for faster, reliable, smaller, and higher-density integrated circuits (IC) at lower cost. Flip chip packages or wafer level packages (WLP) are ideally suited for ICs demanding high speed, high density, and greater pin count. Flip chip style packaging involves mounting the active side of the die facedown toward a chip carrier substrate or printed circuit board (PCB). The electrical and mechanical interconnect between the active devices on the die and conduction tracks on the carrier substrate is achieved through a solder bump structure comprising a large number of conductive solder bumps or balls. The solder bumps are formed by a reflow process applied to solder material deposited on contact pads which are disposed on the semiconductor substrate. The solder bumps are then soldered to the carrier substrate. The flip chip semiconductor package provides a short electrical conduction path from the active devices on the die to the carrier substrate in order to reduce signal propagation, lower capacitance, and achieve overall better circuit performance.

In a semiconductor package, a semiconductor die is encapsulated by a molding material using a process which leaves the active surface of the semiconductor die exposed after encapsulation. An interconnect build-up layer, including dielectric layers, metalized redistribution layers, and under bump metallurgy layer, is disposed over the active surface of the chip and the molding compound. Solder bumps or other electrical interconnections are then formed on the interconnect build-up layer, making the semiconductor die capable of electrically connecting to external devices.

The encapsulation of the semiconductor die includes using

a substrate on which the die is set facedown and allowing the molding compound to flow around and over the die without coating the active surface. In the resulting semiconductor package, the molding material is thinner over the semiconductor die than the surrounding area. Thus, delamination can occur between the semiconductor die and encapsulating material as a result of the difference between the coefficients of thermal expansion (CTE) of the molding material and the semiconductor die.

A mismatch of CTEs can also damage the area where the solder bumps connect to the interconnect build-up layer. Solder joints are fragile elements of a semiconductor package due to their small size and use at high temperatures relative to their melting points. Solder joint failure can occur for a variety of reasons. One category of failure arises from the application of cyclical stresses, primarily from temperature swings and the different CTEs of the solder joints and application board. As solder joint failures can result from standard daily events, such as powering on and off electrical equipment, solder joint reliability is important in the manufacture of WLCSPs.

A need exists to resolve solder joint failure and intermediate interconnect build-up layer delamination issues on WLCSPs due to CTE mismatch between the die and mounting board or interconnect build-up layer.

Summary of the Invention

In one embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a carrier made of electrically conducting material, forming contact pads on the carrier, forming a pre-applied protective layer over an active surface of a semiconductor wafer, removing a semiconductor die with the pre-applied protective layer from

the semiconductor wafer, mounting the semiconductor die with the pre-applied protective layer on the carrier, encapsulating the semiconductor die and contact pads on the carrier, removing the carrier, forming a first insulating layer over the pre-applied protective layer and contact pads, forming vias in the first insulating layer and pre-applied protective layer to expose interconnect sites on the semiconductor die, and forming an interconnect structure over the first insulating layer in electrical contact with the interconnect sites on the semiconductor die and contact pads.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a carrier, forming contact pads on the carrier, and mounting a semiconductor die on the carrier. The semiconductor die has a pre-applied protective layer over its active surface. The method further includes the steps of encapsulating the semiconductor die and contact pads on the carrier, removing the carrier, forming a first insulating layer over the pre-applied protective layer and contact pads, forming vias in the first insulating layer and pre-applied protective layer to expose interconnect sites on the semiconductor die, and forming an interconnect structure over the insulating layer in electrical contact with the interconnect sites on the semiconductor die and contact pads.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a carrier, forming contact pads on the carrier, and mounting a semiconductor die on the carrier. The semiconductor die has a protective layer on its active surface. The method further includes the steps of encapsulating the semiconductor die and contact pads on the carrier with a molding compound, removing the carrier, forming vias in the protective layer to

expose interconnect sites on the semiconductor die, and forming an interconnect structure over the protective layer in electrical contact with the interconnect sites on the semiconductor die and contact pads.

In another embodiment, the present invention is a semiconductor device comprising a semiconductor die having a protective layer formed over its active surface. An encapsulant is formed over the semiconductor die. A first insulating layer is formed over the protective layer. An interconnect structure is formed over the protective layer in electrical contact with interconnect sites on the semiconductor die.

Brief Description of the Drawings

FIG. 1 is a flip chip semiconductor device with solder bumps providing electrical interconnect between an active area of the die and a chip carrier substrate;

FIGs. 2a-2i illustrate the method of making a WLCSP with an interconnect build-up layer;

FIGs. 3a and 3b illustrate an alternative embodiment of the WLCSP made in FIGs. 2a-2i;

FIG. 4 illustrates an embodiment of a WLCSP where the redistribution layer is applied directly to the surface of the molding compound and protective layer of the semiconductor die;

FIG. 5 illustrates the embodiment of FIG. 4 where an additional metallized redistribution layer and insulating layer have been added; and

FIGs. 6a-6b illustrate a redistribution layer formed in the molding compound of the semiconductor package.

Detailed Description of the Drawings

The present invention is described in one or more embodiments in the following description with reference to the Figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

The manufacture of semiconductor devices involves formation of a wafer having a plurality of die. Each die contains hundreds or thousands of transistors and other active and passive devices performing one or more electrical functions. For a given wafer, each die from the wafer typically performs the same electrical function. Front-end manufacturing generally refers to formation of the semiconductor devices on the wafer. The finished wafer has an active side containing the transistors and other active and passive components. Back-end manufacturing refers to cutting or singulating the finished wafer into the individual die and then packaging the die for structural support and/or environmental isolation.

A semiconductor wafer generally includes an active surface having semiconductor devices disposed thereon, and a backside surface formed with bulk semiconductor material, e.g., silicon. The active side surface contains a plurality of semiconductor die. The active surface is formed by a variety of semiconductor processes, including layering, patterning, doping, and heat treatment. In the layering process, semiconductor materials are grown or deposited on the substrate by techniques involving

thermal oxidation, nitridation, chemical vapor deposition, evaporation, and sputtering. Photolithography involves the masking of areas of the surface and etching away undesired material to form specific structures. The doping process injects concentrations of dopant material by thermal diffusion or ion implantation.

Flip chip semiconductor packages and wafer level packages (WLP) are commonly used with integrated circuits (ICs) demanding high speed, high density, and greater pin count. Flip chip style semiconductor device 10 involves mounting an active area 12 of die 14 facedown toward a chip carrier substrate or printed circuit board (PCB) 16, as shown in FIG. 1. Active area 12 contains active and passive devices, conductive layers, and dielectric layers according to the electrical design of the die. The electrical and mechanical interconnect is achieved through a solder bump structure 20 comprising a large number of individual conductive solder bumps or balls 22. The solder bumps are formed on bump pads or interconnect sites 24, which are disposed on active area 12. The bump pads 24 connect to the active circuits by conduction tracks in active area 12. The solder bumps 22 are electrically and mechanically connected to contact pads or interconnect sites 26 on carrier substrate 16 by a solder reflow process. The flip chip semiconductor device provides a short electrical conduction path from the active devices on die 14 to conduction tracks on carrier substrate 16 in order to reduce signal propagation, lower capacitance, and achieve overall better circuit performance.

FIGs. 2a-2i illustrate the method of making a wafer level chip scale package (WLCSP) with an interconnect structure, in which the semiconductor die is prepared from a semiconductor wafer having a pre-applied protective layer on the active side of the wafer. In FIG. 2a, a metal carrier 40 is shown having a

photoresist layer 42 applied to a top surface of metal carrier 40. The metal carrier 40 is made of copper (Cu), aluminum (Al), or other electrically conducting metal. Carrier 40 acts as a support member to hold a semiconductor die and plated metal pads in place during the manufacturing process. During a subsequent electroplating process, metal carrier 40 also serves as a plating current path to form plated metal pads on the carrier.

In FIG. 2b, a plurality of openings or vias are made in the photoresist layer 42 using a photo patterning process such as ultraviolet (UV) exposure and development. The openings define areas for selective plating and can be strategically placed, allowing the areas, when plated, to act as fiducial marks, interconnection contact pads, and saw alignment marks. Metal contact pads 44 are deposited in the openings and onto metal carrier 40 using an electroplating process. Contact pads 44 can be made with electroless nickel/immersion gold (Ni/Au) or other metal or alloy having low resistivity. Once contact pads 44 have been deposited, photoresist layer 42 is stripped off metal carrier 40 through either UV or thermal curing, as shown in FIG. 2c.

In a separate part of the process, a protective layer is pre-applied to the active surface of a semiconductor wafer containing a plurality of semiconductor die. The protective layer is a lamination or coating adhesive applied by spin coating or screen printing. The protection layer is an insulator and can be made with polyimide (PI) film having a low coefficient of thermal expansion (CTE), such as 20ppm/°C or below, or a low modulus silicon base elastomer, under pressure of less than 200MPa.

Vias or openings can be formed in the active surface of the semiconductor wafer by laser drilling or deep reactive ion etching (DRIE). Photo vias can be formed if photosensitive

adhesive layer is applied. The wafer is placed protective layer down to dicing tape and cut with a dicing blade. A pick and place tool removes the individual die with its pre-applied protective layer and places the die on metal carrier 40.

FIG. 2d illustrates semiconductor die 48 with pre-applied protective layer 46 mounted face down on metal carrier 40. The protective layer 46 can be used as the die attach material. The interconnect sites 50 electrically connect to active and passive devices on semiconductor die 48 through conduction tracks or layers formed within the die. The conductive material can be Al, Cu, tin (Sn), nickel (Ni), gold (Au), or silver (Ag).

In one embodiment, metal carrier 40 has one or more passive components 52 with electrodes 54 electrically connected to metal pads 44 with conductive adhesive 56. Passive components 52 can include resistors, capacitors, inductors, transformers, voltage sources, current sources, or similar devices.

In FIG. 2e, the structure formed in FIG. 2d is encapsulated with a polymer molding compound 58 down to metal carrier 40. The molding compound 58 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. Molding compound 58 can be made with epoxy acrylate or other polymer material and applied by transfer molding, liquid encapsulant molding, or other molding process.

Carrier 40 is removed by an etching process, exposing protective layer 46 of semiconductor die 48 and metal pads 44. With metal carrier 40 removed, molding compound 58 provides rigid support for the semiconductor device.

In FIG. 2f, the semiconductor package is inverted such that interconnect sites 50 and active surface of semiconductor die 48 faces upwards. An insulating layer 63 is applied to contact pads 44, protective layer 46, and molding compound 58.

The insulating layer 63 is made with dielectric or photosensitive polymer material having low cure temperature, e.g. less than 200°C. A process carrier 62 is applied to a surface of molding compound 58, opposite protective layer 46, using an adhesive layer 60. Carrier 62 facilitates the process handling in the subsequent interconnect build-up process.

In FIG. 2g, a portion of insulating layer 63 and protective layer 46 is removed to form openings and expose contact pads 44 and interconnect sites 50. The openings can be formed using a photo patterning process if insulating layer 63 and protection layer 46 are photosensitive. Alternatively, if the protective layer 46 is not photosensitive, the openings are formed by laser drilling or DRIE process.

A metallized redistribution layer (RDL) 64 is formed by depositing thin layers of metals over the surface of insulating layer 63 and protection layer 46. Multiple metal layers are typically required to meet the different functional requirements of the metallized RDL such as adhesion, barrier, conductor, and protection. Accordingly, RDLs 64 can be made with layers of Al, titanium (Ti), and titanium tungsten (TiW). RDLs 64 provide electrical contact between metal pads 44 and interconnect sites 50 and subsequent layers.

In FIG. 2h, an insulating layer 66 is formed over insulating layer 63 and RDLs 64. The insulating layer 66 is made with dielectric or photosensitive polymer material having low cure temperature, e.g. less than 200°C. A portion of insulating layer 66 is removed using a photo patterning process such as UV exposure and development to expose RDLs 64. The insulating layers 63 and 66 and RDLs 64 constitute at least a portion of the interconnect build-up layer. Additional photosensitive insulating layers, metalized RDLs, and other conductive layers can be added as needed to expand the

interconnect build-up layers to meet the interconnect requirements for the functional design of semiconductor die 48.

Interconnection contact pads, known as an under bump metallurgy layer (UBM) 68, are deposited and patterned to electrically contact RDLs 64. UBMs 68 provide multiple benefits to the semiconductor package: (1) an interface between the interconnect sites 50 and subsequent electrical interconnections, (2) protection of interconnect sites 50 from the environment, (3) low resistive contact between interconnect sites 50 and the subsequent electrical interconnections, (4) a barrier to solder diffusion into the metal pad, and (5) a seed layer for solder wettability. UBMs 68 are made by forming successive layers of metals by sputtering, each layer having a different function. These layers may include an adhesion layer, diffusion layer, solder wettable layer, and protective layer.

In FIG. 2i, solder bumps 70 are formed on UBMs 68. The solder bumps 70 electrically connect interconnect sites 50 and metal pads 44 with other electrical devices. The solder bumps 70 may be deposited through an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process and are formed from any metal or electrically conductive material, e.g., Sn, lead (Pb), Ni, Au, Ag, Cu, bismuthinite (Bi), and alloys thereof. The solder bumps 70 represent one type of electrical interconnect structure. Finally, carrier 62 is removed either after attaching solder bumps 70 or after wafer singulation.

FIGs. 3a and 3b illustrate an alternative embodiment of the WLCSP made in FIGs. 2a-2i. As with the previously described semiconductor package, a metal carrier having a photoresist layer is used as a support member. Openings are made in the photoresist layer to define the areas where metal pads 44 are deposited and, once deposited, the photoresist layer is stripped

off.

In FIG. 3a, vias 72 are pre-formed in protective layer 46 to expose interconnect sites 50. The semiconductor die 48 is mounted to the metal carrier in a face down position and encapsulated, along with passive components 52, with molding compound 58. The metal carrier is stripped from the semiconductor device and insulating layer 63 is formed on contact pads 44 and protective layer 46. Vias 74, shown in FIG. 3b, are made in insulating layer 63 using a photo patterning process, such as UV exposure and development, directly coupling vias 74 with vias 72 in protective layer 46. The vias 74 in insulating layer 63 are typically the same size or larger than vias 72 in protective layer 46. Vias 74 are aligned with vias 72 to expose interconnect sites 50. As with the previous embodiment, metallized RDLs and additional insulating layers are formed as needed for the interconnect build-up process and, finally, the electrical interconnections are formed, see FIGs. 2g-2i.

FIG. 4 illustrates another embodiment of a semiconductor package. A metal carrier having a photoresist layer is used as a support member. Openings are made in the photoresist layer to define the areas where metal pads 44 are deposited and, once deposited, the photoresist layer is stripped off. A semiconductor die 48, having a pre-applied protective layer 46 on its face, is applied facedown to the metal carrier. The semiconductor die 48 may optionally have pre-formed vias similar to the embodiment illustrated in FIGs. 3a-3b. The semiconductor die 48 is encapsulated, along with passive components 52, with molding compound 58. Next, the metal carrier is stripped from the semiconductor device.

Vias are formed in protective layer 46 if semiconductor die 48 does not have pre-formed vias. Unlike previous

embodiments, FIG. 4 shows that RDL 76 is applied directly to the surface of protective layer 46, molding compound 58, and contact pads 46 using a chemical vapor disposition (CVD), physical vapor deposition (PVD), and/or plating process. The insulating layer 63 is not used in this embodiment. RDLs 76 can be made of Al, Ti, TiW, or other metal. An insulating layer 84 is applied to RDLs 76 and vias are formed, exposing RDLs 76. UBMs 78 can be plated to form the final metal pad areas. Solder bumps 80 are formed on UBMs 78.p

In FIG. 5, a second metalized RDL 86 is formed on insulating layer 84 and is electrically connected to RDL 76. An insulating layer 92 is formed over RDL 86 and insulating layer 84. The insulating layer 92 is made with dielectric or photosensitive polymer material having low cure temperature, e.g. less than 200°C. Vias are formed in insulating layer 92 to expose portions of RDLs 86. Optionally, UBMs 88 can be plated to form the final metal pad areas. Solder bumps 90 are formed on UBMs 88.

In FIGs. 6a and 6b, openings are made in photoresist layer that has been applied to the metal carrier. The openings define the areas where metal pads 44 are deposited and, once deposited, the photoresist layer is stripped off. A semiconductor die 48, with optional pre-formed vias in the protective layer 46, is applied to the metal carrier in a facedown position. The semiconductor die 48 is encapsulated, along with passive components 52, with molding compound 58. The metal carrier is stripped from the semiconductor device and insulating layer 63 is applied to contact pads 44 and protective layer 46. Vias are formed in insulating layer 63 and protective layer 46, if protective layer 46 did not have pre-formed vias.

As can be seen in FIG. 6a, a metalized RDL 104 is formed on insulating layer 63 and protective layer 46. A second

photosensitive insulating layer 100 is applied on top of insulating layer 63, covering RDLs 104. Vias are formed in insulating layer 100. Additional photosensitive insulating layers and metalized RDLs may be added as needed to form the interconnect build-up layers. Additionally, an optional UBMs 102 can be plated in insulating layer 100.

A temporary carrier 108 is applied to the bottom side of molding compound 58 using an adhesive layer 106. The temporary carrier 108 can be made of a stiff material or flexible tape and facilitates the interconnect build-up process formed on the top surface of molding compound 58. Vias or openings are formed through molding compound 58 to expose metal pads 44 using a laser drill or DRIE process. Another metallized RDL 110 is formed on the top surface of molding compound 58 and the vias made in molding compound 58. An insulating layer 112 is applied over RDLs 110. The insulating layer 112 is made with dielectric or photosensitive polymer material having low cure temperature, e.g. less than 200°C. Next, vias or openings are made in insulating layer 112, exposing portions of RDL 110. Finally, in FIG. 6b, process carrier 108 is released and solder bumps 114 are formed on UBMs 102. Optionally, UBMs can be plated to form the final metal pad areas in insulating layer 112.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a carrier made of electrically conducting material;

forming contact pads on the carrier;

forming a pre-applied protective layer over an active surface of a semiconductor wafer;

removing a semiconductor die with the pre-applied protective layer from the semiconductor wafer;

mounting the semiconductor die with the pre-applied protective layer on the carrier;

encapsulating the semiconductor die and contact pads on the carrier;

removing the carrier;

forming a first insulating layer over the pre-applied protective layer and contact pads;

forming vias in the first insulating layer and pre-applied protective layer to expose interconnect sites on the semiconductor die; and

forming an interconnect structure over the first insulating layer in electrical contact with the interconnect sites on the semiconductor die and contact pads.

2. The method of claim 1, further including:

forming a redistribution layer on the first insulating layer;

forming a second insulating layer on the redistribution layer; and

forming an under bump metallization layer over the second insulating layer in electrical contact with the redistribution layer.

3. The method of claim 1, further comprising:

forming a first via in the pre-applied protective layer; and

forming a second via in the first insulating layer aligned with the first via in the pre-applied protective layer to expose the interconnect sites.

4. The method of claim 1, further including mounting a passive component on the contact pads.

5. The method of claim 1, further including forming a solder bump on the under bump metallization.

6. A method of making a semiconductor device, comprising:

providing a carrier;

forming contact pads on the carrier;

mounting a semiconductor die on the carrier, the semiconductor die having a pre-applied protective layer over its active surface;

encapsulating the semiconductor die and contact pads on the carrier;

removing the carrier;

forming a first insulating layer over the pre-applied protective layer and contact pads;

forming vias in the first insulating layer and pre-applied protective layer to expose interconnect sites on the semiconductor die; and

forming an interconnect structure over the insulating layer in electrical contact with the interconnect sites on the semiconductor die and contact pads.

7. The method of claim 6, further including:

forming the protective layer over an active surface of a semiconductor wafer; and

removing the semiconductor die with the pre-applied protective layer from the semiconductor wafer.

8. The method of claim 6, further including:

forming a redistribution layer on the first insulating layer;

forming a second insulating layer on the redistribution layer; and

forming an under bump metallization layer over the second insulating layer in electrical contact with the redistribution layer.

9. The method of claim 6, further comprising:

forming a first via in the pre-applied protective layer; and

forming a second via in the first insulating layer aligned with the first via in the pre-applied protective layer to expose the interconnect sites.

10. The method of claim 6, further including mounting a passive component on the contact pads.

11. The method of claim 6, further including forming a solder bump on the under bump metallization.

12. A method of making a semiconductor device, comprising:

providing a carrier;

forming contact pads on the carrier;

mounting a semiconductor die on the carrier, the semiconductor die having a protective layer on its active surface;

encapsulating the semiconductor die and contact pads on the carrier with a molding compound;

removing the carrier;

forming vias in the protective layer to expose interconnect sites on the semiconductor die; and

forming an interconnect structure over the protective layer in electrical contact with the interconnect sites on the semiconductor die and contact pads.

13. The method of claim 12, further including forming a first insulating layer over the protective layer and contact pads.

14. The method of claim 12, further including:

forming the protective layer over an active surface of a semiconductor wafer; and

removing the semiconductor die with the protective layer from the semiconductor wafer.

15. The method of claim 12, further including:

forming a redistribution layer on the first insulating layer;

forming a second insulating layer on the redistribution layer; and

forming an under bump metallization layer over the second insulating in electrical contact with the redistribution layer.

16. The method of claim 12, further comprising:

forming a first via in the protective layer; and

forming a second via in the first insulating layer aligned with the first via in the protective layer to expose the interconnect sites.

17. The method of claim 12, further including mounting a passive component on the contact pads.

18. The method of claim 12, further including forming a solder bump on the under bump metallization.

19. The method of claim 12, further including:

forming vias through the molding compound to expose the contact pads; and

forming a redistribution layer over the molding compound in electrical contact with the contact pads.

20. A semiconductor device, comprising:

a semiconductor die having a protective layer formed over its active surface;

an encapsulant formed over the semiconductor die;

a first insulating layer formed over the protective layer; and

an interconnect structure formed over the protective layer in electrical contact with interconnect sites on the semiconductor die.

21. The semiconductor device of claim 20, wherein the interconnect structure includes:

a redistribution layer formed on the first insulating layer;

a second insulating layer formed on the redistribution layer; and

an under bump metallization layer formed over the second insulating layer in electrical contact with the redistribution layer.

22. The semiconductor device of claim 20, further including:

a first via formed in the protective layer; and

a second via in the first insulating layer aligned with the via in the protective layer to expose the interconnect sites.

23. The semiconductor device of claim 20, further including a solder bump formed on the under bump metallization.