

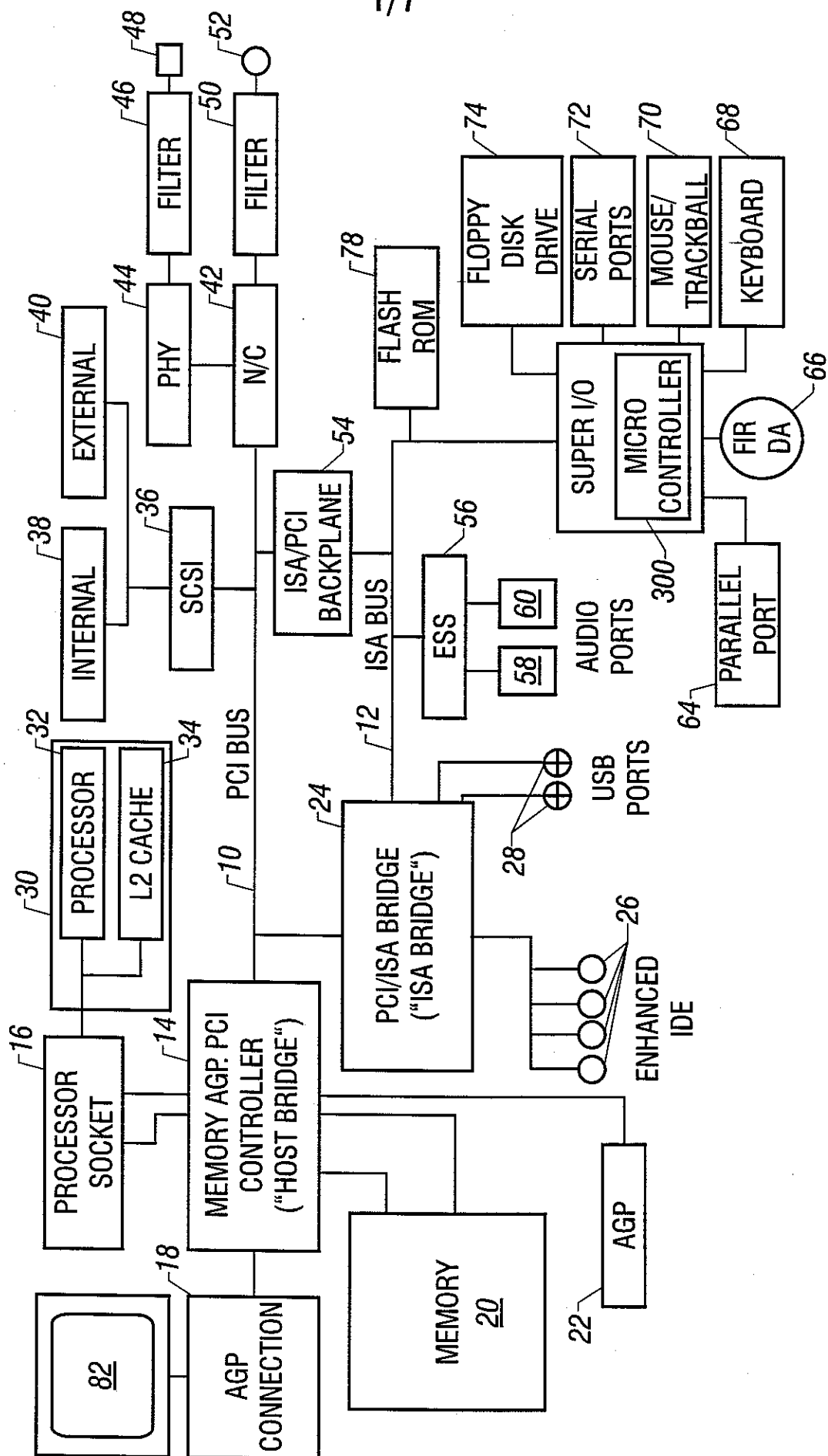


FIG. 1

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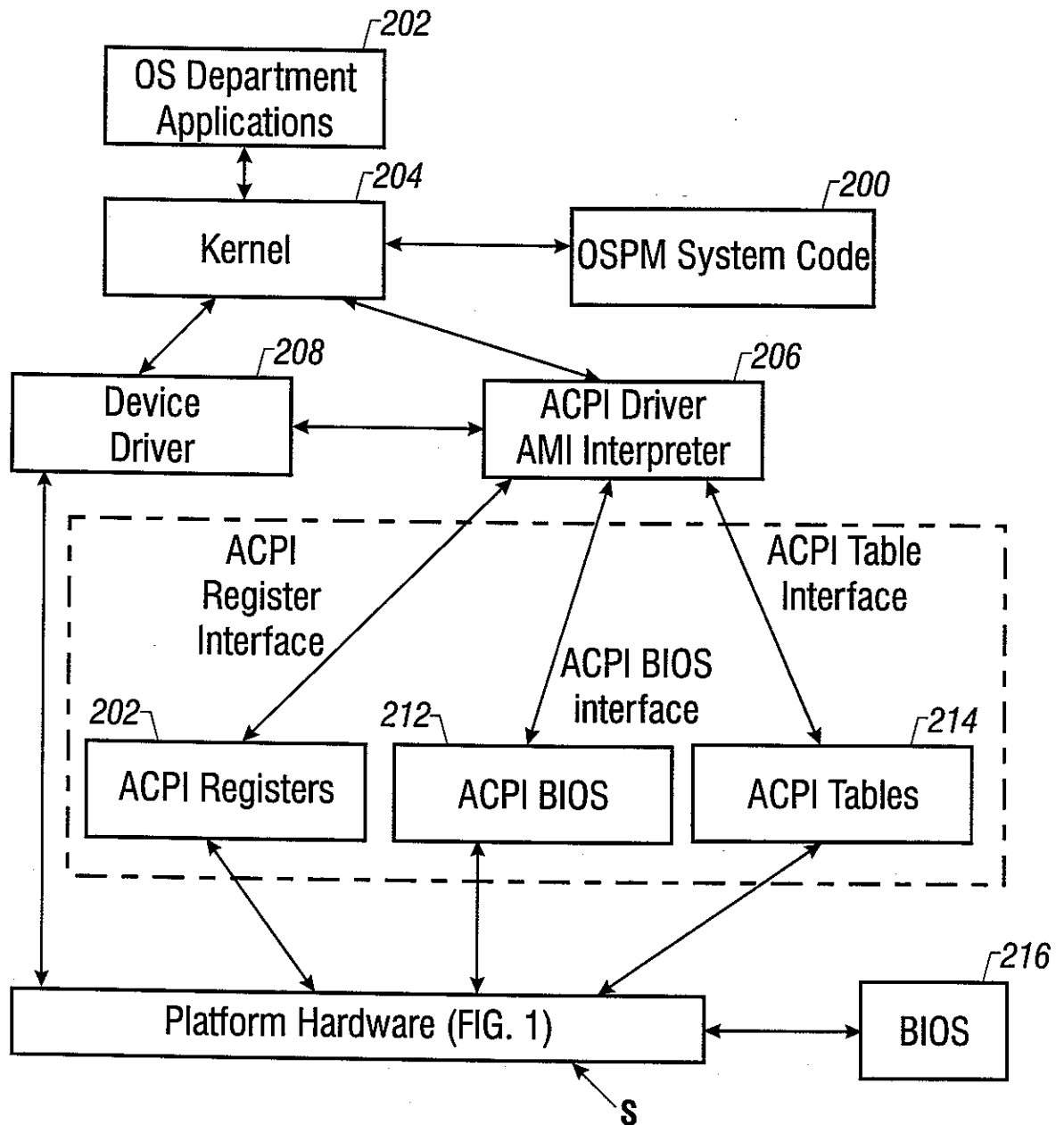
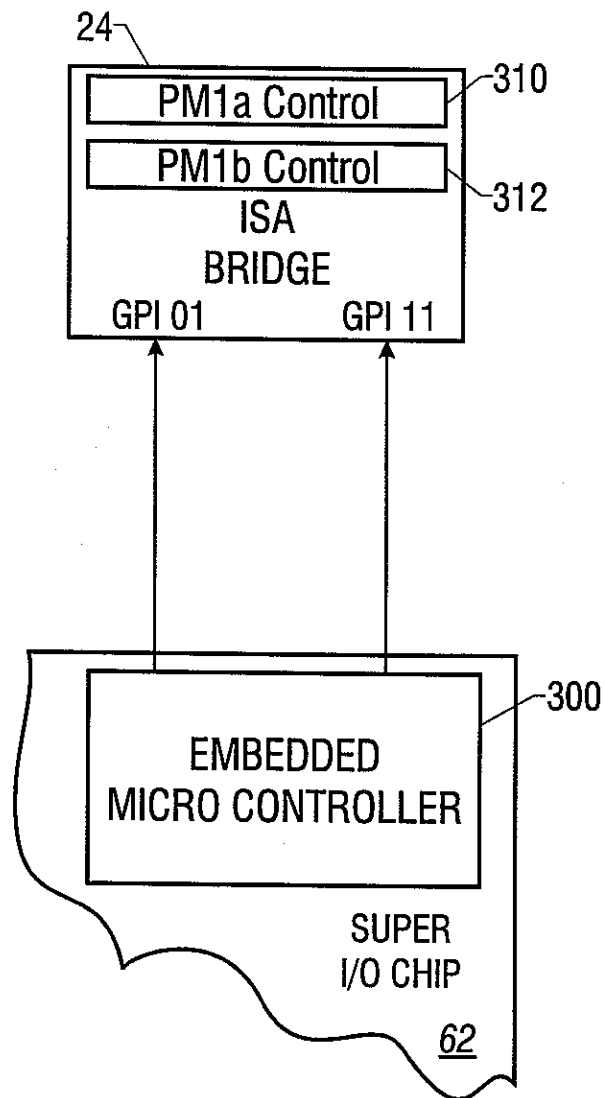


FIG. 2

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**FIG. 3**

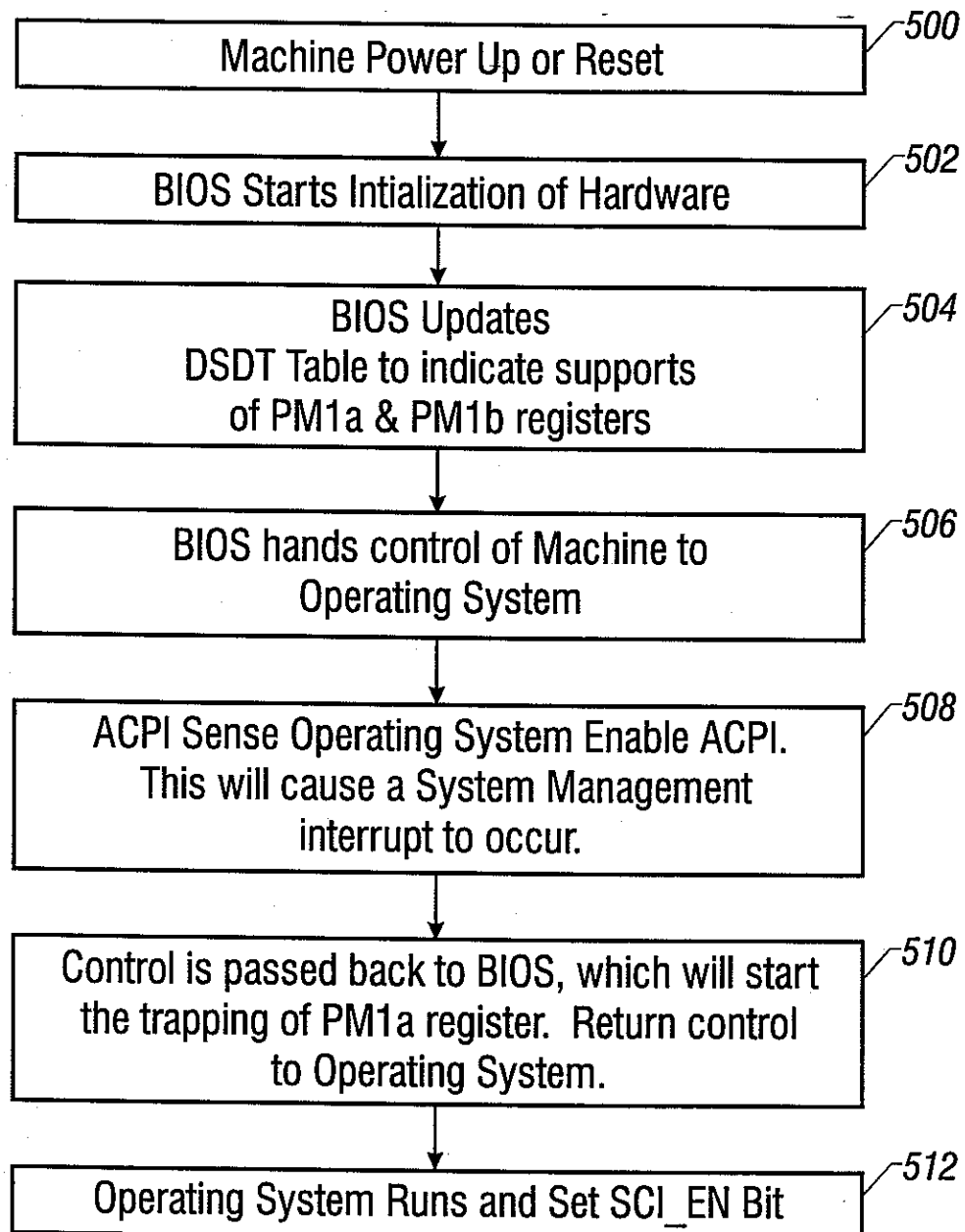
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PM1a, PM1b CONTROL REGISTER

BIT 15:14	BIT 13	BIT 12-10	BIT 9-3	BIT 2	BIT 1	BIT 0
Reserved	Suspend Enable Bit SUS_EN	Suspend Type Field SUS_TYP	Reserved	Global Release Bit	Bus Mater Reload Enable Bit	SCI Enable Bit SCI_EN

FIG. 4

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Intialization Process**FIG. 5**

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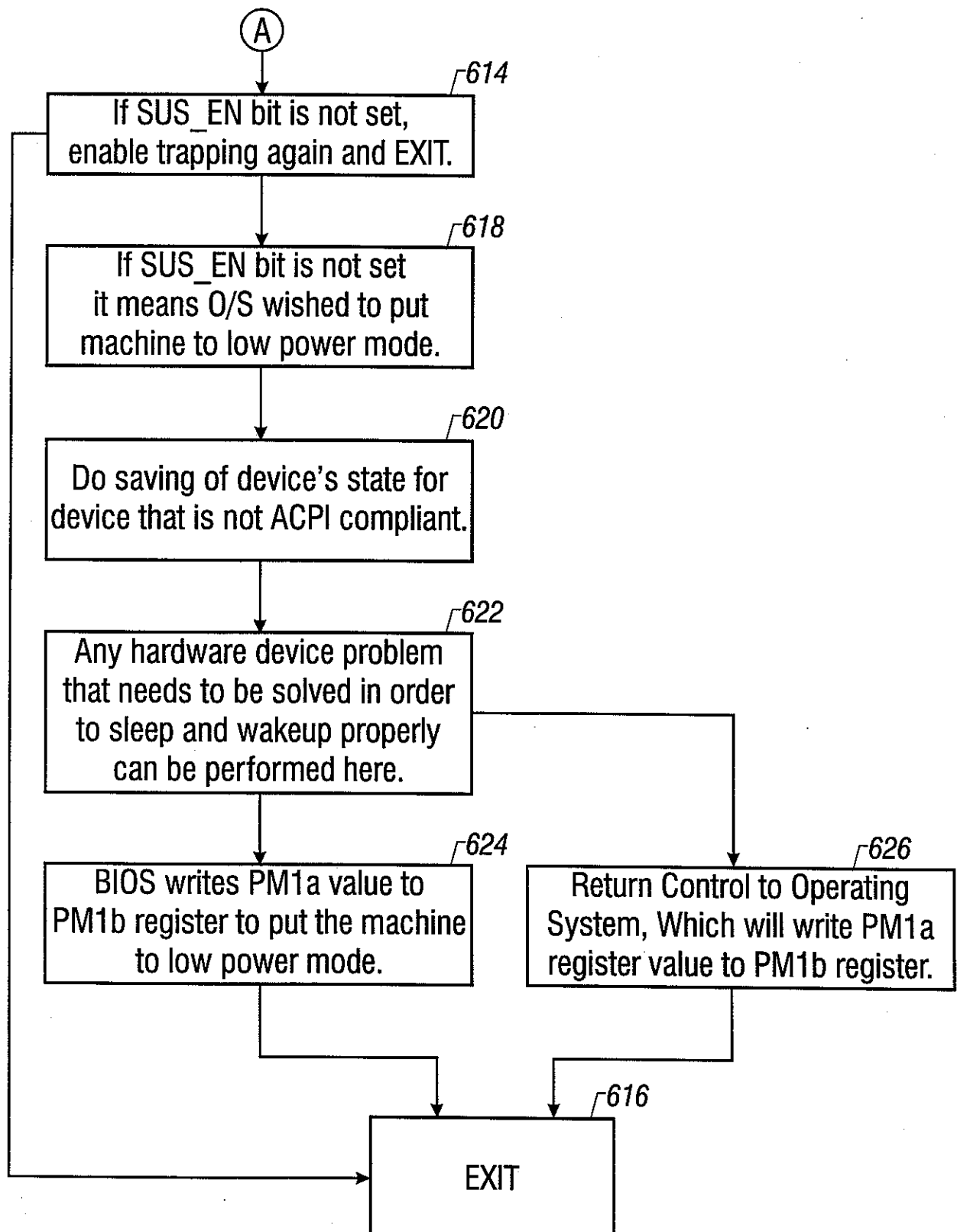


FIG. 6B