

Description

Background of the invention

The present invention relates generally to data transmission systems, and more particularly to an improved method and apparatus for the self-clocking transmission of digital data signals.

Among the self-clocking data transmission techniques in the prior art, one technique commonly referred to as "polar return to zero" utilizes three different voltage levels within a bit interval to encode a data signal. As described in U.S. Patent No: 3,863,025 with reference to Fig. 1 therein a positive voltage level with respect to a reference voltage level indicates a binary one state, while a negative voltage level with respect to the reference voltage level indicates a binary zero state.

A data transmission method in accordance with the prior art portion of claim 1 is disclosed in U.S. patent no. 3,808,366. A data transmission system is described with respect to Figure 1 therein that transmits binary data in the form of a return to zero pulse train with differential polarity reversal used to distinguish the binary states of the data. Synchronizing pulses occurring at the mid-point of each data bit are applied to either line 111 or 112 depending on whether the bit on data line 105 has a binary one state or binary zero state, respectively. The line 111 or 112 being pulsed has a negative potential with respect to the other line, and both lines 111 and 112 otherwise have a positive potential.

Another technique commonly referred to as Manchester coding provides a transition during each bit interval where the direction of the transition determines the binary state of the bit. For example, a positive transition during a bit interval may represent a binary one bit, while a negative transition may represent a binary zero bit.

However, in order to properly receive data signals transmitted according to these prior art techniques, it is essential that timing relationships between successive bits of the data signal be accurately maintained at the data transmitter and properly recognized at the data receiver. Furthermore, proper reception at the data receiver is also dependent on recovery of the clock signal and precise definition of the bit interval. Thus, transmission systems utilizing these prior art techniques are very sensitive to speed and timing variations in the transmission of the data signals, and require that receiving apparatus include expensive and complex circuitry to compensate for such variations.

Summary of the invention

Accordingly, it is an object of the present invention to provide an improved method and apparatus for self-clocking data transmission systems that accommodates expansive variation in the speed and timing of the transmission.

In practicing the present invention, data signals having a plurality of binary bits are transmitted on

two signal lines between a data transmitter and one or more data receivers of a self-clocking data transmission system. According to the data transmission scheme of the present invention, a first two bit binary state of the signal lines is provided both before and after the data signal, and for each bit of the data signal a second two-bit binary state of the signal lines followed by a third two-bit binary state of the signal lines is generated for a bit having a binary one state and a fourth two-bit binary state of the signal lines followed by a third two-bit binary state of the signal lines is generated for a bit having a binary zero state. As a result, the transmitted data signal is not only self-clocking, but also independent of the transmission frequency, thereby accommodating expansive variations in the time duration of successive bit intervals.

In the data transmission system of the present invention, a data transmitter is coupled to one or more data receivers by two signal lines on which data signals are transmitted according to the foregoing data transmission scheme. The data transmitter includes circuitry for generating the two-bit binary states of the signal lines for each bit of a data signal to be transmitted. The receiving units include circuitry responsive to the third two-bit binary state of the signal lines for providing a clock signal. The receiving unit also includes first storing circuitry responsive to the second and fourth two-bit binary states of the signal lines for storing an output signal having a binary one or zero state, respectively. Thus, the output signal of the first storing circuitry reflects the binary state of the successive bits of the transmitted data signal. The output signal of the first storing circuitry is then stored into second storing circuitry in response to the clock signal. At the end of the transmission, the second storing circuitry holds the received data signal. The received data signal in the second storing circuitry may then be utilized for accomplishing any suitable function in the data receiver.

Brief description of the drawings

Fig. 1 is a block diagram of a self-clocking data transmission system embodying the present invention.

Fig. 2 is a block diagram of a data transmitter for the data transmission system in Fig. 1.

Fig. 3 is a block diagram of a data receiver for the data transmission system in Fig. 1.

Fig. 4 is a state diagram illustrating the binary states that may be utilized to encode the data signals transmitted between the data transmitter and data receivers in the data transmission system in Fig. 1.

Fig. 5 is a timing diagram illustrating the wave forms of various blocks of the data receiver in Fig. 3.

Fig. 6 is a block diagram of a different data receiver for the data transmission system in Fig. 1.

Fig. 7 is a timing diagram of the waveforms for various blocks of the data receiver in Fig. 6.

Detailed description of the preferred embodiment

In Fig. 1, there is illustrated a block diagram of a self-clocking data transmission system embodying the present invention. Data transmitter 101 is coupled to data receivers 102—104 by two signal lines, labelled "true data" and "complement data". The data receivers 102—104 may also transmit return data signals to the data transmitter by means of a shared signal line, labelled "return data", as shown for data receivers 103 and 104 or by means of a separate signal line as for data receiver 102. The return data signals transmitted by the data receivers 102—104 on the return data signal line are transmitted in synchronism with the data signals received from the data transmitter 101 on the true data and complement data signal lines. The data transmitter 101 and data receivers 102—104 may be in close proximity with one another or may be separated by great distances because the data transmission is self-clocking and is independent of the transmitting frequency.

According to the present invention, data is transmitted by the data transmitter 101 to the data receivers 102—104 by making use of the four two-bit binary states that can be assumed by the true data and complement data signal lines taken together. For example, referring to state diagram of Fig. 4, a first two-bit binary state may be referred to as a "word state" 401, where the true data signal line has a binary one state and the complement data signal line has a binary one state. When no data is being transmitted, the word state 401 is provided on the true data and complement data signal lines. When a data signal is to be transmitted, a transition is made from the word state 401 to the zero state 402, represented as binary state 01, or to the one state 404, represented as the binary state 10, where the complement data signal line has a binary one state for binary zero bits of the data signal and the true data signal line has a binary one state for binary one bits of the data signal. For all succeeding bits of the data signal to be transmitted, a transition is first made to the bit state 403, represented by the binary state 00, before a transition to the one state 404 or zero state 402. The two-bit binary states of the true data and complement data signal lines are set forth hereinbelow in Table I.

TABLE I

True data	Complement data	Two-bit state
1	1	Word state
0	1	Zero state
1	0	One state
0	0	Bit state

Furthermore, transitions between the states 401—404 in Fig. 4 are selected so that only one signal line is changing binary state at a time. Transitions between the word state 401 and bit state 403 and between the one state 404 and zero state 402 are not allowed since they would require that the state of both the true data and complement data signal lines change simultaneously. By limiting transitions between the binary states 401—404 to those where only one of the signal lines is changing binary state at a time, the effects of skewing and timing variations are minimized. Moreover, by transmitting data signals as illustrated by the state diagram in Fig. 4, the transmission on the true data and complement data signal lines is both self-clocking and independent of the transmitting frequency. The time duration between each of the state transitions illustrated in Fig. 4 need not be the same and may vary dynamically. Thus, according to the data transmission system of the present invention, the frequency of the data transmission may be entirely asynchronous with randomly varying time intervals between successive state transitions.

To summarize the transmission sequence, the true data and complement data signal lines have the word state 401 when no data is being transmitted (see waveforms in Fig. 5). For transmission of a data signal, two state transitions occur for each bit. For the first bit of the data signal, a transition is made from the word state 401 to the one state 404 or zero state 402, depending on the binary state of the bit to be transmitted. Next, a state transition is made to the bit state 403. Then, for each succeeding bit of the data signal, a transition is made to the one state 404 or the zero state 402 and then back to the bit state 403. Since a transition is made to the bit state 403 for each bit of the data signal to be transmitted, the bit state 403 can be utilized at the data receivers to generate a clock signal. For the last bit of the data signal, the last state transition is made from the one state 404 or zero state 402 back to the word state 401. Returning to the word state 401, after the last bit of the data signal has been transmitted indicates to the data receivers 102—104 that a complete data signal has been transmitted.

In order to provide for the bidirectional transmission of data signals between the data transmitter 101 and the data receivers 102—104 in Fig. 1, another signal line, referred to as the return data signal line, may be provided for carrying non-return-to-zero (NRZ) coded data signals from the data receivers 102—104. The data receivers 102—104 can transmit a return data signal on the return data signal line by utilizing the clock signal developed by detecting the bit state of the true data and complement data signal lines. In order to accommodate the transmission of return data signals, separate return data signal lines can be provided to each data receiver, as for data

Detailed description of the preferred embodiment

In Fig. 1, there is illustrated a block diagram of a self-clocking data transmission system embodying the present invention. Data transmitter 101 is coupled to data receivers 102—104 by two signal lines, labelled "true data" and "complement data". The data receivers 102—104 may also transmit return data signals to the data transmitter by means of a shared signal line, labelled "return data", as shown for data receivers 103 and 104 or by means of a separate signal line as for data receiver 102. The return data signals transmitted by the data receivers 102—104 on the return data signal line are transmitted in synchronism with the data signals received from the data transmitter 101 on the true data and complement data signal lines. The data transmitter 101 and data receivers 102—104 may be in close proximity with one another or may be separated by great distances because the data transmission is self-clocking and is independent of the transmitting frequency.

According to the present invention, data is transmitted by the data transmitter 101 to the data receivers 102—104 by making use of the four two-bit binary states that can be assumed by the true data and complement data signal lines taken together. For example, referring to state diagram of Fig. 4, a first two-bit binary state may be referred to as a "word state" 401, where the true data signal line has a binary one state and the complement data signal line has a binary one state. When no data is being transmitted, the word state 401 is provided on the true data and complement data signal lines. When a data signal is to be transmitted, a transition is made from the word state 401 to the zero state 402, represented as binary state 01, or to the one state 404, represented as the binary state 10, where the complement data signal line has a binary one state for binary zero bits of the data signal and the true data signal line has a binary one state for binary one bits of the data signal. For all succeeding bits of the data signal to be transmitted, a transition is first made to the bit state 403, represented by the binary state 00, before a transition to the one state 404 or zero state 402. The two-bit binary states of the true data and complement data signal lines are set forth hereinbelow in Table I.

TABLE I

True data	Complement data	Two-bit state
1	1	Word state
0	1	Zero state
1	0	One state
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Furthermore, transitions between the states 401—404 in Fig. 4 are selected so that only one signal line is changing binary state at a time. Transitions between the word state 401 and bit state 403 and between the one state 404 and zero state 402 are not allowed since they would require that the state of both the true data and complement data signal lines change simultaneously. By limiting transitions between the binary states 401—404 to those where only one of the signal lines is changing binary state at a time, the effects of skewing and timing variations are minimized. Moreover, by transmitting data signals as illustrated by the state diagram in Fig. 4, the transmission on the true data and complement data signal lines is both self-clocking and independent of the transmitting frequency. The time duration between each of the state transitions illustrated in Fig. 4 need not be the same and may vary dynamically. Thus, according to the data transmission system of the present invention, the frequency of the data transmission may be entirely asynchronous with randomly varying time intervals between successive state transitions.

To summarize the transmission sequence, the true data and complement data signal lines have the word state 401 when no data is being transmitted (see waveforms in Fig. 5). For transmission of a data signal, two state transitions occur for each bit. For the first bit of the data signal, a transition is made from the word state 401 to the one state 404 or zero state 402, depending on the binary state of the bit to be transmitted. Next, a state transition is made to the bit state 403. Then, for each succeeding bit of the data signal, a transition is made to the one state 404 or the zero state 402 and then back to the bit state 403. Since a transition is made to the bit state 403 for each bit of the data signal to be transmitted, the bit state 403 can be utilized at the data receivers to generate a clock signal. For the last bit of the data signal, the last state transition is made from the one state 404 or zero state 402 back to the word state 401. Returning to the word state 401, after the last bit of the data signal has been transmitted indicates to the data receivers 102—104 that a complete data signal has been transmitted.

In order to provide for the bidirectional transmission of data signals between the data transmitter 101 and the data receivers 102—104 in Fig. 1, another signal line, referred to as the return data signal line, may be provided for carrying non-return-to-zero (NRZ) coded data signals from the data receivers 102—104. The data receivers 102—104 can transmit a return data signal on the return data signal line by utilizing the clock signal developed by detecting the bit state of the true data and complement data signal lines. In order to accommodate the transmission of return data signals, separate return data signal lines can be provided to each data receiver, as for data

Receiver 102, or a number of data receivers, such as data receivers 103—104, can be connected to one return data signal line. If a number of data receivers are connected to the same return data signal line, it will be necessary to selectively address the particular data receiver that is to transmit a return data signal. Many different addressing schemes can be utilized, such as, for example, utilizing a portion of the data signal transmitted by the data transmitter to provide an address, or transmitting separate address signals and data signals.

Referring to Fig. 2, there is illustrated a block diagram of data transmitter 101 in Fig. 1. When it is desired to transmit data, a data strobe pulse (a momentary binary one state) is applied to the strobe input of latch 201 for loading a new set of input data, which here is represented as an eight-bit binary signal. Latch 201 is transparent during data strobe pulse, and is otherwise latched. The data strobe signal via inverting gate 202 also clocks the Q output of flip-flop 208 to a binary one state, which corresponds to a +V voltage level with respect to ground. The binary one state of the Q output of flip-flop 208 is coupled via OR gate 204 to produce a binary one state of the busy signal, indicating that the data transmitter is presently busy transmitting a data signal.

The shift clock signal coupled to the clock inputs of flip-flop 209 and registers 203 and 211 determines the rate at which data is transmitted on the true data and complement data signal lines to the data receivers. The shift clock signal may be provided by a clock oscillator or by a remote device, such as a microcomputer. According to the present invention, the shift clock signal need not be periodic and may vary dynamically in frequency over time and from transition to transition.

Once flip-flop 208 has been clocked by the data strobe signal, the Q output of flip-flop 209 is clocked to a binary one state at the next positive transition of the shift clock signal. The Q output from flip-flop 209 is coupled to the parallel/shift input of register 203 and to the D input of register 211. Thus, at the next positive transition of the shift clock signal, register 203 is parallel loaded with the data signal from latch 201 and the first stage of shift register 211 is loaded with a binary one. The binary one state of the Q output of flip-flop 209 is also used to reset flip-flop 208, maintain the busy signal at a binary one state via OR gates 205 and 204, and apply the shift clock signal to register 203 via OR gate 205, inverting gate 206 and OR gate 207.

For the next eight cycle intervals of the shift clock signal, the data signal in register 203 is shifted right applying each bit in succession to inverting gate 216 and AND gate 219, while at the same time a binary one bit is shifted from stage to stage in shift register 211. The outputs of shift register 211 are combined via OR gate 212 for enabling AND gate 214 and for maintaining a

binary one state of the busy signal via OR gates 205 and 204.

Prior to transmission of the data signal loaded into latch 201, the true data and complement data signal lines were maintained at a binary one state by OR gate 212 via OR gate 218 and inverting gate 215. When OR gate 218 changes state from a binary zero state to a binary one state, the state of the true data and complement data signal lines will be determined by each bit of the data signal in register 203. During the binary one interval of the first shift clock signal, the true data and complement data signal lines are maintained at a binary one state by AND gate 213. Next, during each succeeding binary zero interval of the shift clock signal, AND gates 217 and 219 are enabled to apply successive bits of the data signal from register 203 to OR gates 220 and 221 for the complement data and true data signal lines, respectively. The true data signal lines will have a binary one state for those bits of the data signal that likewise have a binary one state, while the complement data signal line will have a binary one state for those bits of the data signal which have a binary zero state. Typical waveforms for the true data and complement data signal lines are illustrated by the waveforms in Fig. 5.

At the same time that a data signal is being transmitted on the complement data and true data signal lines, a return data signal may be received on the return data signal line, which is coupled to the D input of register 203. Register 203, which is initially parallel loaded with the input data signal from latch 201, serially receives the return data signal as it is shifted to transmit the input data signal. Once the last bit of the input data signal has been transmitted, OR gate 212 changes state from a binary one state to a binary zero state and disables via OR gate 205 and inverting gate 206 the shift clock signal to register 203. Also, when the transmission is complete, register 203 provides the return data signal received from a data receiver at its outputs.

Referring to Fig. 3, there is illustrated a detailed circuit diagram for data receiver 102—104 in Fig. 1. Waveforms corresponding to labelled blocks in Fig. 3 for a typical data signal transmission are illustrated in Fig. 4, where the transmitted data signal is 11010001 and the return data signal is 01110101. The data receiver in Fig. 3 includes a data latch formed by NAND gates 305 and 306, which is set by NAND gate 303, which detects the one state (see Fig. 4) of the true data and complement data signal lines, and is reset by NAND gate 304, which detects the zero state of the true data and complement data signal lines. Complements of the true data and complement data signal lines necessary for decoding the two-bit binary states thereon are provided by inverting gates 301 and 302. The output from data latch 305 and 306 is the recovered NRZ data signal and is coupled to the D input and high order parallel input of register 312.

The data receiver also includes a last bit latch formed by NAND gates 309 and 310. The last bit

latch 309—310 is set by the bit state of the true data and complement data signal lines, as detected by NAND gate 307, and is reset by the word state of the true data and complement data signal lines, as detected by NAND gate 308. The last bit latch output signal is applied to NAND gate 314 and to the parallel/shift input of register 312.

A recovered bit clock signal is provided by NAND gate 311 in response to the bit state of the true data and complement data signal lines, as detected by NAND gate 307. The bit clock signal is also forced to a binary one state by the word state of the true data and complement data signal lines, as detected by NAND gate 308.

When a data signal is transmitted to the data receiver in Fig. 3, register 312 is initially parallel loaded in response to the last bit latch output signal and thereafter serially clocked in response to each positive transition of the bit clock signal for shifting in the recovered NRZ data signal. Since the data signals in the preferred embodiment have eight bits, register 312 and latch 31 have eight stages. When eight bits of the recovered NRZ data signal have been shifted into register 312, the frame clock signal provided by NAND gate 308 changes state from a binary zero state to a binary one state causing latch 313 to be transparent, coupling the received NRZ data signal from register 312 to its output. While register 312 was shifting, latch 313 was held in the latched state by the binary zero state of the frame clock signal. Also, the return data signal loaded into register 312 is serially applied by NAND gates 314—316 to the return data signal line while the transmitted data signal is being received.

The data receiver of Fig. 3 requires a separate return data signal line for each additional data receiver included in the data transmission system. In order to couple a number of data receivers to the same return data signal line, it is necessary to provide capability for selectively addressing each data receiver. One way to provide for selectively addressing a number of data receivers is to transmit an address signal before the data signal. Many different transmission formats providing for an address signal prior to the data signal can be realized utilizing the data transmission system of the present invention. For example, the address signal and data signal may be separated by the word state of the true data and complement data signal lines if the data transmission system in Fig. 4 is used. According to another system, the address signal and data signal may be differentiated by providing the word state of the true data and complement data signal lines between each bit of the address signal and the bit state between each bit of the data signal. By utilizing this system, variable length addresses may be defined while maintaining fixed length data words. The end of the address signal is identified by the bit state of the true data and complement data signal lines occurring after the first bit of the following data signal. A data receiver which receives an eight-bit

address signal followed by an eight-bit data signal transmitted according to this scheme is illustrated in Fig. 6.

Referring to Fig. 6, the data receiver illustrated there is essentially identical to the data receiver of Fig. 3, with the exception of the additional address register 320, address decoder 321 and gates 322—325. Waveforms corresponding to labelled blocks in Fig. 6 for a typical address and data signal transmission are illustrated in Fig. 7, where the transmitted address signal is 01010101, the transmitted data signal is 11010001, and the return data signal is 01110101. In Fig. 6, address register 320 serially receives the NRZ data signal from data latch 305—306 in response to the word state of the true data and complement data signal lines, as detected by NAND gate 308 and inverting gate 322. Since the word state is provided between each bit of the address signal, NAND gate 308 and inverting gate 322 provide clock pulses in response to the detected word state. The eight-bit address signal received by address register 320 is decoded by address decoder 21 and enables NAND gate 323 if the correct address for this receiver has been received and decoded. The data signal following the address signal is then serially shifted into register 312 as described with reference to Fig. 3. A return data signal previously parallel loaded into register 312 is serially applied by way of inverting gate 324 to NAND gate 315 which also is enabled by address decoder 321 if the correct address has been received and decoded. The return data signal is coupled from NAND gate 315 by way of NAND gate 316 to open collector inverting gate 325 for application to the shared return data signal line. The open-collector inverting gate 325 is disabled until the address signal is detected by the decoder 321 which then enables NAND gate 315. Since a number of different data receivers are coupled to the return data signal line, an open collector inverting gate 325 is utilized to interface each data receiver to the return data signal line. Any other suitable tri-state busing devices could also be utilized for interfacing the data receivers to the return data signal line.

When all eight bits of the transmitted data signal have been serially shifted into register 312, NAND gate 323, having been enabled by address decoder 321, clocks the received data signal from register 312 into register 326 in response to the output from last bit latch 309, 310.

According to another feature of the present invention, the data receiver in Fig. 6 may alert the data transmitter that a return data signal is available by putting a momentary interrupt signal on the return data signal line. In Fig. 6, NAND gate 314 is enabled to couple the interrupt signal to the return data signal line by an output of the last bit latch 309, 310. The output of the last bit latch 309, 310 disables NAND gate 314 only during transmission of the return data signal. Thus, an interrupt signal can be coupled to the return data signal line by any receiver at any time except during the time interval during which a selected

data receiver is transmitting a return data signal. Since the data transmitter has no way of telling which data receiver generated the interrupt signal, the data transmitter will have to poll all data receivers after receiving the interrupt signal.

The data transmitter in Fig. 2 and the data receivers in Figs. 3 and 6 can be constructed of conventional integrated circuit devices, such as the CMOS devices described in the CMOS Integrated Circuits Book, published by Motorola Semiconductor Products, Inc., Austin, Texas, 1978. Furthermore, the electrical circuit devices comprising the data transmitter in Fig. 2 and the data receiver in Figs. 3 and 6 can be readily integrated into a semiconductive substrate such that a data transmitter and data receiver can be separately, or both, provided in a single integrated circuit device.

The data transmission system of the present invention can be advantageously utilized in many different data transmission applications. For example, the inventive data transmission system can be used to communicate data between a microprocessor and peripheral devices such as auxiliary memories, keyboards, displays and radio units. Likewise, the inventive data transmission system can be used to control a plurality of radio transmitters located in geographically separated remote stations from a central control station. Delays and skewing due to long distances are not critical to proper transmission since the data transmission system is self-clocking and independent of speed and timing variations.

In summary, the data transmission system and apparatus of the present invention provide for reliable, self-clocking, bidirectional data transmission that is highly immune to speed and timing variations. By utilizing two bit binary states of the true data and complement data signal lines taken together, the inventive data transmission system is capable of uniquely defining the beginning and end of a data signal and the binary states of the bits of a data signal, while also differentiating between address and data signals. The exact two-bit binary states selected can be varied as long as only one signal line changes binary state for each state transition, as illustrated in Fig. 4.

Claims

1. A method of serially transmitting a data signal from a signal source by means of first and second binary signal sequences transmitted over respective first and second signal lines, the data signal including a plurality of bits each having a binary zero state or a binary one state, said method comprising the steps of:

a) generating a first binary state of the first and second signal sequences before and after the data signal; and

b) generating for each bit of the data signal a second binary state of the first signal sequence and the first binary state second signal sequence for a bit having a binary zero state, and generating

the first binary state of the first signal sequence and the second binary state of the second signal sequence for a bit having a binary one state; and characterized by the step of:

c) generating the second binary state of the first and second signal sequences between successive bits of the data signal.

2. The method according to claim 1, further characterized by the step of repeating steps b) and c) for transmitting subsequent data signals.

3. The method according to claim 1, further characterized by the step of generating a clock signal having a dynamically varying frequency, said step b) generating the respective binary states of the first and second signal sequences for each bit of the data signal in response to the clock signal.

4. The method according to claim 1, further characterized by the step of generating a clock signal having a frequency varying over a predetermined range of frequencies, said step b) generating the respective binary states of the first and second signal sequences for each bit of the data signal in response to the clock signal.

5. The method according to claim 1, further characterized by the step of generating a clock signal having a predetermined frequency, said step b) generating the respective binary states of the first and second signal sequences for each bit of the data signal in response to the clock signal.

6. A method of serially transmitting an address signal and a data signal from a signal source by means of first and second binary signal sequences transmitted over respective first and second signal lines, the address signal and data signal each including a plurality of bits having a binary zero state or a binary one state, said method characterized by the steps of:

a) generating a first binary state of the first and second signal sequences before the first bit of the address signal and after the last bit of the data signal;

b) generating for each bit of the address signal a second binary state of the first signal sequence and the first binary state of the second signal sequence followed by the first binary state of the first and second signal sequences for a bit having a binary zero state, and generating the first binary state of the first signal sequence and the second binary state of the second signal sequence followed by the first binary state of the first and second signal sequences for a bit having a binary one state;

c) generating for each bit of the data signal the second binary state of the first signal sequence and the first binary state of the second signal sequence for a bit having a binary zero state, and generating the first binary state of the first signal sequence and the second binary state of the second signal sequence for a bit having a binary one state; and

d) generating the second binary state of the first and second signal sequences between successive bits of the data signal.

7. The method according to claim 6, further

data receiver is transmitting a return data signal. Since the data transmitter has no way of telling which data receiver generated the interrupt signal, the data transmitter will have to poll all data receivers after receiving the interrupt signal.

The data transmitter in Fig. 2 and the data receivers in Figs. 3 and 6 can be constructed of conventional integrated circuit devices, such as the CMOS devices described in the CMOS Integrated Circuits Book, published by Motorola Semiconductor Products, Inc., Austin, Texas, 1978. Furthermore, the electrical circuit devices comprising the data transmitter in Fig. 2 and the data receiver in Figs. 3 and 6 can be readily integrated into a semiconductive substrate such that a data transmitter and data receiver can be separately, or both, provided in a single integrated circuit device.

The data transmission system of the present invention can be advantageously utilized in many different data transmission applications. For example, the inventive data transmission system can be used to communicate data between a microprocessor and peripheral devices such as auxiliary memories, keyboards, displays and radio units. Likewise, the inventive data transmission system can be used to control a plurality of radio transmitters located in geographically separated remote stations from a central control station. Delays and skewing due to long distances are not critical to proper transmission since the data transmission system is self-clocking and independent of speed and timing variations.

In summary, the data transmission system and apparatus of the present invention provide for reliable, self-clocking, bidirectional data transmission that is highly immune to speed and timing variations. By utilizing two bit binary states of the true data and complement data signal lines taken together, the inventive data transmission system is capable of uniquely defining the beginning and end of a data signal and the binary states of the bits of a data signal, while also differentiating between address and data signals. The exact two-bit binary states selected can be varied as long as only one signal line changes binary state for each state transition, as illustrated in Fig. 4.

Claims

1. A method of serially transmitting a data signal from a signal source by means of first and second binary signal sequences transmitted over respective first and second signal lines, the data signal including a plurality of bits each having a binary zero state or a binary one state, said method comprising the steps of:

a) generating a first binary state of the first and second signal sequences before and after the data signal; and

b) generating for each bit of the data signal a second binary state of the first signal sequence and the first binary state second signal sequence for a bit having a binary zero state, and generating

the first binary state of the first signal sequence and the second binary state of the second signal sequence for a bit having a binary one state; and characterized by the step of:

c) generating the second binary state of the first and second signal sequences between successive bits of the data signal.

2. The method according to claim 1, further characterized by the step of repeating steps b) and c) for transmitting subsequent data signals.

3. The method according to claim 1, further characterized by the step of generating a clock signal having a dynamically varying frequency, said step b) generating the respective binary states of the first and second signal sequences for each bit of the data signal in response to the clock signal.

4. The method according to claim 1, further characterized by the step of generating a clock signal having a frequency varying over a predetermined range of frequencies, said step b) generating the respective binary states of the first and second signal sequences for each bit of the data signal in response to the clock signal.

5. The method according to claim 1, further characterized by the step of generating a clock signal having a predetermined frequency, said step b) generating the respective binary states of the first and second signal sequences for each bit of the data signal in response to the clock signal.

6. A method of serially transmitting an address signal and a data signal from a signal source by means of first and second binary signal sequences transmitted over respective first and second signal lines, the address signal and data signal each including a plurality of bits having a binary zero state or a binary one state, said method characterized by the steps of:

a) generating a first binary state of the first and second signal sequences before the first bit of the address signal and after the last bit of the data signal;

b) generating for each bit of the address signal a second binary state of the first signal sequence and the first binary state of the second signal sequence followed by the first binary state of the first and second signal sequences for a bit having a binary zero state, and generating the first binary state of the first signal sequence and the second binary state of the second signal sequence followed by the first binary state of the first and second signal sequences for a bit having a binary one state;

c) generating for each bit of the data signal the second binary state of the first signal sequence and the first binary state of the second signal sequence for a bit having a binary zero state, and generating the first binary state of the first signal sequence and the second binary state of the second signal sequence for a bit having a binary one state; and

d) generating the second binary state of the first and second signal sequences between successive bits of the data signal.

7. The method according to claim 6, further



characterized by the step of repeating steps c) and d) for transmitting subsequent data signals.

8. The method according to claim 6, further characterized by the step of generating a clock signal having a dynamically varying frequency, said steps b) and c) generating the respective binary states of the first and second signal sequences for each bit in response to the clock signal.

9. The method according to claim 6, further characterized by step of generating a clock signal having a frequency varying over a predetermined range of frequencies, said steps b) and c) generating the respective binary state of the first and second signal sequences for each bit in response to the clock signal.

10. The method according to claim 6, further characterized by the step of generating a clock signal having a predetermined frequency, said steps b) and c) generating the respective binary states of the first and second signal sequences for each bit in response to the clock signal.

11. Apparatus for serially transmitting a data signal from a signal source by means of first and second binary signal sequences transmitted over respective first and second signal lines, the data signal including a plurality of bits each having a binary zero state or a binary one state, said apparatus comprising first means (212, 214, 215, 218) for generating a first binary state of the first and second signal sequences before and after the data signal; second means (216, 217, 219) for generating for each bit of the data signal a second binary state of the first signal sequence and the first binary state of the second signal sequence for a bit having a binary zero state, and generating a first binary state of the first signal sequence and the second binary state of the second signal sequence for a bit having a binary one state; and said apparatus being characterized by:

said second means generating the second binary state of the first and second signal sequences between successive bits of the data signal.

12. The data transmitting apparatus according to claim 11, further characterized by means for generating a clock signal, said second generating means (216, 217, 219) generating the respective binary states of the first and second signal sequences for each bit of the data signal in response to the clock signal.

13. The data transmitting apparatus according to claim 12, further characterized by means for providing a strobe signal and means (201) responsive to the strobe signal for storing a data signal, said second generating means (216, 217, 219) responsive to the data signal stored in the storing means for generating the respective states of the first and second signal sequences.

14. Apparatus for receiving a data signal from first and second binary signal sequences serially transmitted over respective first and second signal lines by a signal source, the data signal including a plurality of bits each having a binary zero state or a binary one state, the first and

second signal sequences having a first binary state before and after the data signal, the first signal sequence having a second binary state and the second signal sequence having a first binary state for data signal bits having a binary zero state and the first signal sequence having a first binary state and the second signal sequence having a second binary state for data signal bits having a binary one state, and characterized in that the first and second signal sequences have a second binary state between successive data signal bits, said receiving apparatus comprising:

first means (307, 308, 311) responsive to the second binary state of the first and second signal sequences for generating a clock signal;

second means (303, 304, 305, 306) coupled to the first and second signals for storing an output signal having a binary zero state in response to a second binary state of the first signal sequence and a first binary state of the second signal sequence, and storing an output signal having a binary one state in response to a first binary state of the first signal sequence and a second binary state of the second signal sequence; and

third means (312) coupled to the first means and second means for storing the second means output signal in response to the clock signal.

15. The data receiving apparatus according to claim 14, further characterized by a signal source for transmitting a return data signal having a plurality of binary bits by means of return signal sequence on a return signal line, and means (314, 315, 316) responsive to the clock signal for generating for successive bits of the return data signal a corresponding binary state of the return signal sequence.

16. The data receiving apparatus according to claim 15, further characterized by means (314, 316) for generating a pulse signal of a predetermined binary state on the return signal line to indicate that a return data signal is available for transmission.

17. A system for serially communicating data signals, each including a plurality of bits each having a binary zero state or a binary one state, between a transmitting unit (101) and at least one receiving unit (102, 103, 104) intercoupled by first and second signal lines carrying respective first and second binary signal sequences, the transmitting unit including a signal source for providing a data signal, first means (212, 214, 215, 218) for generating a first binary state of the first and second signal sequences before and after the data signal and second means (216, 217, 219) for generating for each bit of the data signal a second binary state of the first signal sequence and a first binary state of the second signal sequence for a bit having a binary zero state, and the first binary state of the first signal sequence and a second binary state of the second signal sequence for a bit having a binary one state; and said transmitting unit characterized by:

said second means (216, 217, 219) generating the second binary state of the first and second



signal sequences between successive bits of the data signal; and

the receiving unit including:

third means (307, 308, 311) responsive to the second state of the first and second signal sequences for generating a clock signal;

fourth means (303, 304, 305, 306) responsive to the first and second signal sequences for storing an output signal having a binary zero state in response to a second binary state of the first signal sequence and a first binary state of the second signal sequence, and a binary one state in response to a first binary state of the first signal sequence and second binary state of the second signal sequence; and

fifth means (312) coupled to the third means (307, 308, 311) and fourth means (303, 304, 305, 306) for storing successive binary states of the fourth means output signal in response to the third means clock signal.

18. The data communication system according to claim 17, characterized in that said transmitting unit further includes sixth means for generating a clock signal, said second means (216, 217, 219) generating the respective binary states of the first and second signal sequences for each bit in response to the clock signal.

19. The data communication system according to claim 18 further characterized by a return signal line for carrying a return signal sequence transmitted between the receiving unit and transmitting unit, said receiving unit including a signal source for providing a return data signal having a plurality of binary bits, and seventh means (314, 315, 316) responsive to the third means clock signal for generating for successive bits of the return data signal a corresponding binary state of the return signal sequence, and the transmitting unit further including eighth means (203) coupled to the return signal line for storing in response to the sixth means clock signal successive binary states of the return signal sequence.

20. The data communication system according to claim 19, characterized in that said receiving unit further includes ninth means (314, 316) for generating a pulsed binary state of the return signal line to indicate that a return data signal is available for transmission, said transmitting unit including tenth means coupled to the return signal line for detecting said pulsed binary state and enabling the transmitting unit to transmit a data signal.

21. The data communication system according to claim 19 or 20, further characterized in that a plurality of said receiving units are coupled to the first and second signal lines and the return signal line.

Patentansprüche

1. Verfahren zum seriellen Übertragen eines Datensignals von einer Datenquelle mittels erster und zweiter Binärsignalfolgen, die über entsprechende erste und zweite Signalleitungen übertragen werden, wobei das Datensignal eine

Vielzahl von Bits aufweist, von denen jedes einen binären Null-Zustand oder einen binären Eins-Zustand aufweist, mittels folgender Schritte:

a) Erzeugen eines ersten Binärzustandes der ersten und zweiten Signalfolgen vor und nach dem Datensignal; und

b) Erzeugen für jedes Bit des Datensignals einen zweiten Binärzustand der ersten Signalfolge und den ersten Binärzustand der zweiten Signalfolge für ein Bit, das den Binärzustand Null hat, und Erzeugen des ersten Binärzustandes der ersten Signalfolge und des zweiten Binärzustandes der zweiten Signalfolge für ein Bit, das einen Binärzustand Eins hat, gekennzeichnet durch den Schritt

c) Erzeugen des zweiten Binärzustandes der ersten und zweiten Signalfolgen zwischen aufeinanderfolgenden Bits des Datensignals.

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß die Schritte b) und c) für die Übertragung nachfolgender Datensignale wiederholt werden.

3. Verfahren nach Anspruch 1, gekennzeichnet durch den Schritt des Erzeugens eines Taktsignals mit einer sich dynamisch ändernden Frequenz, wobei der Schritt b) die entsprechenden Binärzustände der ersten und zweiten Signalfolgen für jedes Bit des Datensignals als Folge des Taktsignals erzeugt.

4. Verfahren nach Anspruch 1, gekennzeichnet durch den Schritt des Erzeugens eines Taktsignals mit einer sich über einen vorbestimmten Frequenzbereich ändernden Frequenz, wobei der Schritt b) die entsprechenden Binärzustände der ersten und zweiten Signalfolgen für jedes Bit des Datensignals in Übereinstimmung mit dem Taktsignal erzeugt.

5. Verfahren nach Anspruch 1, gekennzeichnet durch den Schritt des Erzeugens eines Taktsignals mit einer vorbestimmten Frequenz, wobei der Schritt b) die entsprechenden Binärzustände der ersten und zweiten Signalfolgen für jedes Bit des Datensignals als Folge des Taktsignals erzeugt.

6. Verfahren zum seriellen Übertragen eines Adresssignals und eines Datensignals von einer Signalquelle mit Hilfe von erster und zweiter Binärsignalfolgen, die über entsprechende erste und zweite Signalleitungen übertragen werden, wobei das Adresssignal und das Datensignal jeweils eine Mehrzahl von Bits aufweisen mit einem binären Null-Zustand und einem binären Eins-Zustand, gekennzeichnet durch folgende Schritte

a) Erzeugen eines ersten Binärzustandes der ersten und zweiten Signalfolgen vor dem ersten Bit des Adresssignals und nach dem letzten Bit des Datensignals;

b) Erzeugen für jedes Bit des Adresssignals einen zweiten Binärzustand der ersten Signalfolge und den ersten Binärzustand der zweiten Signalfolge gefolgt von dem ersten Binärzustand der ersten und zweiten Signalfolgen für ein Bit eines binären Null-Zustandes und Erzeugen des ersten Binärzustandes der ersten Signalfolge und des zweiten Binärzustandes der zweiten Signal-



folge gefolgt von dem ersten Binärzustand der ersten und zweiten Signalfolgen für ein Bit, das einen binären Eins-Zustand hat;

c) Erzeugen für jedes Bit des Datensignals den zweiten Binärzustand der ersten Signalfolge und den ersten Binärzustand der zweiten Signalfolge für ein Bit, das einen binären Null-Zustand hat, und Erzeugen des ersten Binärzustandes der ersten Signalfolge und des zweiten Binärzustandes der zweiten Signalfolge für ein Bit, das einen binären Eins-Zustand hat; und

d) Erzeugen des zweiten Binärzustandes der ersten und zweiten Signalfolgen zwischen aufeinanderfolgenden Bits des Datensignals.

7. Verfahren nach Anspruch 6, gekennzeichnet durch den Schritt der Wiederholung der Schritte c) und d) für die Übertragung aufeinanderfolgender Datensignale.

8. Verfahren nach Anspruch 6, gekennzeichnet durch den Schritt des Erzeugens eines Taktsignals mit einer sich dynamisch ändernden Frequenz, wobei die Schritte b) und c) die entsprechenden Binärzustände der ersten und zweiten Signalfolgen für jedes Bit infolge des Taktsignals erzeugen.

9. Verfahren nach Anspruch 6, gekennzeichnet durch den Schritt des Erzeugens eines Taktsignals mit einer sich über einen vorgegebenen Frequenzbereich ändernden Frequenz, wobei die Schritte b) und c) die entsprechenden Binärzustände der ersten und zweiten Signalfolgen für jedes Bit infolge des Taktsignals erzeugen.

10. Verfahren nach Anspruch 6, gekennzeichnet, durch den Schritt des Erzeugens eines Taktsignals mit einer vorbestimmten Frequenz, wobei die Schritte b) und c) die entsprechenden Binärzustände der ersten und zweiten Signalfolgen für jedes Bit infolge des Taktsignals erzeugen.

11. Vorrichtung zum seriellen Übertragen eines Datensignals von einer Signalquelle mittels erster und zweiter Binärsignalfolgen, die über entsprechende erste und zweite Signalleitungen übertragen werden, wobei das Datensignal eine Mehrzahl von Bits aufweist, von denen jedes einen binären Null-Zustand oder einen binären Eins-Zustand hat, mit einer ersten Einrichtung (212, 214, 215) zum Erzeugen eines ersten Binärzustandes der ersten und zweiten Signalfolgen vor und nach dem Datensignal, zweiten Einrichtung (216, 217, 219) zum Erzeugen für jedes Bit des Datensignals einen zweiten Binärzustand der ersten Signalfolge und des ersten Binärzustandes der zweiten Signalfolge für ein Bit eines binären Null-Zustandes und Erzeugen eines ersten Binärzustandes der ersten Signalfolge und des zweiten Binärzustandes der zweiten Signalfolge für ein Bit eines binären Eins-Zustandes, dadurch gekennzeichnet, daß die zweite Einrichtung den zweiten Binärzustand der ersten und zweiten Signalfolgen zwischen aufeinanderfolgenden Bits des Datensignals erzeugt.

12. Vorrichtung nach Anspruch 11, gekennzeichnet durch Einrichtungen zum Erzeugen eines Taktsignals, wobei die zweite erzeugende Ein-

richtung (216, 217, 219) die entsprechenden Binärzustände der ersten und zweiten Signalfolgen für jedes Bit des Datensignals als Folge des Taktsignals erzeugen.

13. Vorrichtung nach Anspruch 12, gekennzeichnet durch eine Einrichtung zum Bereitstellen eines Tastsignals und eines auf das Tastsignal ansprechende Einrichtung (201) zum Speichern eines Datensignals, wobei die zweiten erzeugenden Einrichtungen (216, 217, 219) auf das in der Speichereinrichtung gespeicherte Datensignal ansprechen, um die entsprechenden Zustände der ersten und zweiten Signalfolgen zu erzeugen.

14. Vorrichtung zum Empfangen eines Datensignals aus ersten und zweiten Binärsignalfolgen, die seriell über entsprechende erste und zweite Signalleitungen von einer Signalquelle übertragen werden, wobei das Datensignal eine Mehrzahl von Bits enthält, von denen jedes einen binären Null- oder einen binären Eins-Zustand hat, die ersten und zweiten Signalfolgen einen ersten binären Zustand von und nach dem Datensignal haben, die erste Signalfolge einen zweiten Binärzustand und die zweite Signalfolge einen ersten Binärzustand für Datensignalbits eines binären Null-Zustandes und die erste Signalfolge einen ersten Binärzustand und die zweite Signalfolge einen zweiten Binärzustand für Datensignalbits eines binären Eins-Zustandes haben, dadurch gekennzeichnet, daß die ersten und zweiten Signalfolgen einen zweiten binären Zustand zwischen aufeinanderfolgenden Datensignalbits haben und die Empfangseinrichtung aufweist:

erste Einrichtungen (307, 308, 311), die auf den zweiten Binärzustand der ersten und zweiten Signalfolgen ansprechen und ein Taktsignal erzeugen;

zweite Einrichtungen (303, 304, 305, 306) die die ersten und zweiten Signale empfangen und ein Ausgangssignal speichern, das einen binären Null-Zustand infolge eines zweiten Binärzustandes der ersten Signalfolge und eines ersten Binärzustandes der zweiten Signalfolge hat, und zum Speichern eines Ausgangssignals, das einen binären Eins-Zustand als Folge eines ersten Binärzustandes der ersten Signalfolge und eines zweiten Binärzustandes der zweiten Signalfolge hat; und

dritte Einrichtungen (312), die mit den ersten und zweiten Einrichtungen verbunden sind zum Speichern des Ausgangssignals der zweiten Einrichtung infolge des Taktsignals.

15. Empfangseinrichtung nach Anspruch 14, gekennzeichnet durch eine Signalquelle zum Übertragen eines Datenrücksignals mit einer Vielzahl von Binärbits mittels einer Rücksignalfolge auf einer Rücksignalleitung und Einrichtungen (314, 315, 316), die auf das Taktsignal ansprechen und aufeinanderfolgende Bits des Rücksignals eines korrespondierenden Binärzustandes zur Rücksignalfolge erzeugen.

16. Empfangseinrichtung nach Anspruch 15, gekennzeichnet durch Einrichtungen (314, 316) zum Erzeugen eines Impulssignales eines vor-



bestimmten Binärzustandes auf der Rücksignalleitung, um anzuzeigen, daß ein Datenrücksignal zur Übertragung bereit steht.

17. System zur seriellen Übermittlung von Datensignalen, von denen jedes eine Mehrzahl von Bits umfaßt, von denen jedes einen binären Null-Zustand oder einen binären Eins-Zustand aufweist, zwischen einer Sendeeinheit (101) und wenigstens einer Empfangseinheit (102, 103, 104), die miteinander durch erste und zweite Signalleitungen miteinander verbunden sind, die entsprechende erste und zweite Binärsignalfolgen führen, wobei die Sendeeinheit eine Signalquelle zum Bereitstellen eines Datensignals, erste Einrichtungen (212, 214, 215, 218) zum Erzeugen eines ersten Binärzustandes der ersten und zweiten Signalfolgen vor und nach dem Datensignal und zweite Einrichtungen (216, 217, 219) zum Erzeugen für jedes Bit des Datensignals einen zweiten binären Zustand der ersten Signalfolge und einen ersten binären Zustand der zweiten Signalfolge für ein Bit eines binären Null-Zustandes und den ersten Binärzustand der ersten Signalfolge und einen zweiten Binärzustand der zweiten Signalfolge für ein Bit eines binären Eins-Zustandes erzeugt, dadurch gekennzeichnet, daß

die zweite Einrichtung (216, 217, 219) den zweiten Binärzustand der ersten und zweiten Signalfolgen zwischen aufeinanderfolgenden Bits des Datensignals erzeugt, und

die Empfangseinheit dritte Einrichtungen (307, 308, 311) enthält, die auf den zweiten Zustand der ersten und zweiten Signalfolgen ansprechen, um ein Taktsignal zu erzeugen, und

daß vierte Einrichtungen (303, 304, 305, 306) vorgesehen sind, die auf die ersten und zweiten Signalfolgen ansprechen, um ein Ausgangssignal zu speichern, das einen binären Null-Zustand als Folge eines zweiten binären Zustandes der ersten Signalfolge und einen ersten binären Zustand der zweiten Signalfolge und einen binären Eins-Zustand infolge eines ersten Binärzustandes der ersten Signalfolge und eines zweiten Binärzustandes der zweiten Signalfolge aufweist, und

fünfte Einrichtungen (312) vorgesehen sind, die mit den dritten Einrichtungen (307, 308, 311) und den vierten Einrichtungen (303, 304, 305, 306) verbunden sind, um aufeinanderfolgende Binärzustände des Ausgangssignals der vierten Einrichtungen als Folge der Taktsignale der dritten Einrichtungen zu speichern.

18. Datenübertragungssystem nach Anspruch

17, dadurch gekennzeichnet, daß die Sendeeinheit weiterhin sechste Einrichtungen zum Erzeugen eines Taktsignales aufweist, wobei die zweiten Einrichtungen (216, 217, 219) die entsprechenden Binärzustände der ersten und zweiten Signalfolgen für jedes Bit infolge des Taktsignales erzeugen.

19. Datenübertragungssystem nach Anspruch 18, gekennzeichnet durch eine Rücksignalleitung zum Führen einer Rücksignalfolge, die zwischen der Empfangseinheit und der Sendeeinheit übertragen wird, wobei die Empfangseinheit eine

Signalquelle zum Erzeugen eines Datenrücksignals aus einer Vielzahl von Bits aufweist sowie siebente Einrichtungen (314, 315, 316) enthält, die auf das Taktsignal der dritten Einrichtungen ansprechen, um für die aufeinanderfolgenden Bits des Datenrücksignals einen der Rücksignalfolge korrespondierenden Binärzustand zu erzeugen, und daß die Sendeeinheit weiterhin achte Einrichtungen (203) enthält, die an die Rücksignalleitung angeschlossen sind, um in Abhängigkeit vom Taktsignal der sechsten Einrichtungen aufeinanderfolgende Binärzustände der Rücksignalfolge zu speichern.

20. Datenübertragungssystem nach Anspruch 19, dadurch gekennzeichnet, daß die Empfangseinheit weiterhin neunte Einrichtungen (314, 316) enthält, die einen gepulsten Binärzustand der Rücksignalleitung erzeugt, um anzuzeigen, daß ein Datenrücksignal zur Übertragung bereitsteht, daß die Sendeeinheit zehnte Einrichtungen aufweist, die mit der Rücksignalleitung verbunden sind, um den gepulsten Binärzustand zu detektieren und die Übertragungseinheit zum Senden eines Datensignals freizuschalten.

21. Datenübertragungssystem nach Anspruch 19 oder 20, dadurch gekennzeichnet, daß eine Vielzahl von Empfangseinheiten mit den ersten und zweiten Signalleitungen und der Rücksignalleitung verbunden sind.

Revendications

1. Procédé de transmission en série d'un signal de donnée provenant d'une source de signal au moyen de première et seconde séries de signaux binaires transmis par des première et seconde lignes de signaux respectives, le signal de donnée incluant un ensemble de bits ayant chacun un état binaire "zéro" ou un état binaire "un", ledit procédé consistant à: a) engendrer un premier état binaire des première et seconde séries de signaux avant et après le signal de donnée; et b) engendrer pour chaque bit du signal de donnée un second état binaire de la première série de signaux et le premier état binaire de la seconde série de signaux pour un bit ayant un état binaire "zéro", en engendrer le premier état binaire de la première série de signaux et le second état binaire de la seconde série de signaux pour un bit ayant un état binaire "un"; caractérisé en ce qu'il consiste en outre à c) engendrer le second état binaire des première et seconde séries de signaux entre les bits successifs du signal de donnée.

2. Procédé selon la revendication 1, caractérisé en ce qu'il consiste en outre à répéter les opérations b) et c) pour transmettre des signaux de données suivants.

3. Procédé selon la revendication 1, caractérisé en ce qu'il consiste en outre à engendrer un signal d'horloge ayant une fréquence variant dynamiquement, ladite opération b) consistant à engendrer les états binaires respectifs des première et seconde séries de signaux pour chaque bit du signal de donnée étant exécutée en réponse au signal d'horloge.



4. Procédé selon la revendication 1, caractérisé en ce qu'il consiste en outre à engendrer un signal d'horloge ayant une fréquence qui varie dans une gamme de fréquences prédéterminée, ladite opération b) consistant à engendrer les états binaires respectifs des première et seconde séries de signaux pour chaque bit du signal de donnée étant exécutée en réponse au signal d'horloge.

5. Procédé selon la revendication 1, caractérisé en ce qu'il consiste en outre à engendrer un signal d'horloge ayant une fréquence prédéterminée, ladite opération b) consistant à engendrer les états binaires respectifs des première et seconde séries de signaux pour chaque bit du signal de donnée étant exécutée en réponse au signal d'horloge.

6. Procédé de transmission en série d'un signal d'adresse et d'un signal de donnée provenant d'une source de signaux au moyen de première et seconde séries de signaux binaires transmis par des première et seconde lignes de signaux respectives, le signal d'adresse et le signal de donnée incluant chacun un ensemble de bits ayant un état binaire "zéro" ou un état binaire "un", ledit procédé étant caractérisé en ce qu'il consiste à:

a) engendrer un premier état binaire des première et seconde séries de signaux ayant le premier bit du signal d'adresse et après le dernier bit du signal de donnée;

b) engendrer pour chaque bit du signal d'adresse un second état binaire de la première série de signaux et le premier état binaire de la seconde série de signaux suivi par le premier état binaire des première et seconde séries de signaux pour un bit ayant un état binaire "zéro", et engendrer le premier état binaire de la première série de signaux et le second état binaire de la seconde série de signaux suivi par le premier état binaire des première et seconde séries de signaux pour un bit ayant un état binaire "un";

c) engendrer pour chaque bit du signal de donnée le second état binaire de la première série de signaux et le premier état binaire de la seconde série de signaux pour un bit ayant un état binaire "zéro", et engendrer le premier état binaire de la première série de signaux et le second état binaire de la seconde série de signaux pour un bit ayant un état binaire "un"; et

d) engendrer le second état binaire des première et seconde séries de signaux entre les bits successifs du signal de donnée.

7. Procédé selon la revendication 6, caractérisé en ce qu'il consiste en outre à répéter les opérations c) et d) pour transmettre les signaux de données suivants.

8. Procédé selon la revendication 6, caractérisé en ce qu'il consiste en outre à engendrer un signal d'horloge ayant une fréquence variant dynamiquement, lesdites opérations b) et c) consistant à engendrer les états binaires respectifs des première et seconde séries de signaux pour chaque bit étant exécutées en réponse au signal d'horloge.

9. Procédé selon la revendication 6, caractérisé

en ce qu'il consiste en outre à engendrer un signal d'horloge ayant une fréquence variant dans une gamme de fréquences prédéterminée, lesdites opérations b) et c) consistant à engendrer les états binaires respectifs des première et seconde séries de signaux pour chaque bit étant exécutées en réponse au signal d'horloge.

10. Procédé selon la revendication 6, caractérisé en ce qu'il consiste en outre à engendrer un signal d'horloge ayant une fréquence prédéterminée, lesdites opérations b) et c) consistant à engendrer les états binaires respectifs des première et seconde séries de signaux pour chaque bit étant exécutées en réponse au signal d'horloge.

11. Dispositif pour transmettre en série un signal de donnée provenant d'une source de signal au moyen de première et seconde séries de signaux binaires transmis par des première et seconde séries de signaux binaires transmis par des première et seconde lignes de signaux respectives, le signal de donnée incluant un ensemble de bits ayant chacun un état binaire "zéro" ou un état binaire "un", ledit dispositif comprenant des premiers moyens (212, 214, 215, 218) pour engendrer un premier état binaire des première et seconde séries de signaux avant et après le signal de donnée; des seconds moyens (216, 217, 219) pour engendrer pour chaque bit du signal de donnée un second état binaire de la première série de signaux et le premier état binaire de la seconde série de signaux pour un bit ayant un état binaire "zéro", et pour engendrer un premier état binaire de la première série de signaux et le second état binaire de la seconde série de signaux pour un bit ayant un état binaire "un"; ledit dispositif étant caractérisé en ce que les seconds moyens engendrent le second état binaire des première et seconde séries de signaux entre les bits successifs du signal de donnée.

12. Dispositif de transmission de données selon la revendication 11, caractérisé en ce qu'il comprend en outre des moyens pour engendrer un signal d'horloge, lesdits seconds moyens de génération (216, 217, 219) engendrant les états binaires respectifs des première et seconde séries de signaux pour chaque bit du signal de donnée en réponse au signal d'horloge.

13. Dispositif de transmission de données selon la revendication 12, caractérisé en ce qu'il comprend en outre des moyens pour fournir un signal d'échantillonnage et un moyen (201) sensible au signal d'échantillonnage pour mémoriser un signal de donnée, lesdits seconds moyens de génération (216, 217, 219) étant sensibles au signal de donnée mémorisé dans le moyen de mémorisation pour engendrer les états respectifs des première et seconde séries de signaux.

14. Dispositif pour recevoir un signal de donnée à partir de première et seconde séries de signaux binaires transmis en série par des première et seconde lignes de signaux par une source de signal, le signal de donnée incluant un ensemble de bits ayant chacun un état binaire "zéro" ou un état binaire "un", les première et seconde séries



de signaux ayant un premier état binaire avant et après le signal de donnée, la première série de signaux ayant un second état binaire et la seconde série de signaux ayant un premier état binaire pour les bits de signal de donnée ayant un état binaire "zéro" et la première série de signaux ayant un premier état binaire et la seconde série de signaux ayant un second état binaire pour les bits de signal de donnée ayant un état binaire "un", caractérisé en ce que les première et seconde séries de signaux ont un second état binaire entre les bits successifs de signal de donnée et en ce que le dispositif récepteur comprend;

des premiers moyens (307, 308, 311) sensibles au second état binaire des première et seconde séries de signaux pour engendrer un signal d'horloge;

des seconds moyens (303, 304, 305, 306) reliés aux première et seconde lignes de signaux pour mémoriser un signal de sortie ayant un état binaire "zéro" en réponse à un second état binaire de la première série de signaux et un premier état binaire de la seconde série de signaux, et pour mémoriser un signal de sortie ayant un état binaire "un" en réponse à un premier état binaire de la première série de signaux et un second état binaire de la seconde série de signaux; et

un troisième moyen (312) relié aux premiers et seconds moyens pour mémoriser le signal de sortie des seconds moyens en réponse au signal d'horloge.

15. Dispositif récepteur de données selon la revendication 14, caractérisé en ce qu'il comprend en outre une source de signal pour émettre un signal de donnée de retour ayant un ensemble de bits au moyen d'une série de signaux de retour sur une ligne de signaux de retour, et des moyens (314, 315, 316) sensibles au signal d'horloge pour engendrer pour les bits successifs du signal de donnée de retour un état binaire correspondant de la série de signaux de retour.

16. Dispositif récepteur de données selon la revendication 15, caractérisé en ce qu'il comprend en outre des moyens (314, 316) pour engendrer un signal pulsé d'un état binaire prédéterminé sur la ligne de signaux de retour afin d'indiquer qu'un signal de donnée de retour est disponible pour une transmission.

17. Système pour une transmission en série de signaux de données, incluant chacun un ensemble de bits ayant chacun un état binaire "zéro" ou un état binaire "un", entre une unité émettrice (101) et au moins une unité réceptrice (102, 103, 104) interconnectées par des première et seconde lignes de signaux par lesquelles passent des première et seconde séries de signaux binaires, l'unité émettrice incluant une source de signal pour fournir un signal de donnée, des premiers moyens (212, 214, 215, 218) pour engendrer un premier état binaire des première et seconde séries de signaux avant et après le signal de donnée et des seconds moyens

(216, 217, 219) pour engendrer pour chaque bit du signal de donnée un second état binaire de la première série de signaux et un premier état binaire de la seconde série de signaux pour un bit ayant un état binaire "zéro", et le premier état binaire de la première série de signaux et un second état binaire de la seconde série de signaux pour un bit ayant un état binaire "un"; caractérisé en ce que dans l'unité émettrice:

les seconds moyens (216, 217, 219) engendrent le second état binaire des première et seconde séries de signaux entre les bits successifs du signal de donnée;

et en ce que l'unité réceptrice comprend:

des troisièmes moyens (307, 308, 311) sensibles au second état des première et seconde séries de signaux pour engendrer un signal d'horloge;

des quatrièmes moyens (303, 304, 305, 306) sensibles aux première et seconde séries de signaux pour mémoriser un signal de sortie ayant un état binaire "zéro" en réponse à un second état binaire de la première série de signaux et un premier état binaire de la seconde série de signaux, et ayant un état binaire "un" en réponse à un premier état binaire de la première série de signaux et un second état binaire de la seconde série de signaux; et

un cinquième moyen (312) relié aux troisièmes moyens (307, 308, 311) et aux quatrièmes moyens (303, 304, 305, 306) pour mémoriser des états binaires successifs du signal de sortie des quatrièmes moyens en réponse au signal d'horloge des troisièmes moyens.

18. Système de transmission de données selon la revendication 17, caractérisé en ce que l'unité émettrice comprend en outre des sixièmes moyens pour engendrer un signal d'horloge, les seconds moyens (216, 217, 219) engendrant les états binaires respectifs des première et seconde séries de signaux pour chaque bit en réponse au signal d'horloge.

19. Système de transmission de données selon la revendication 18, caractérisé en ce qu'il comprend en outre une ligne de signaux de retour pour faire passer une série de signaux de retour transmis entre l'unité réceptrice et une unité émettrice, l'unité réceptrice incluant une source de signal pour fournir un signal de donnée de retour comportant un ensemble de bits, et des septièmes moyens (314, 315, 316) sensibles au signal d'horloge des troisièmes moyens pour engendrer pour les bits successifs du signal de donnée de retour un état binaire correspondant de la série de signaux de retour, et en ce que l'unité émettrice comprend en outre un huitième moyen (203) relié à la ligne de signaux de retour pour mémoriser en réponse au signal d'horloge des sixièmes moyens les états binaires successifs de la série de signaux de retour.

20. Système de transmission de données selon la revendication 19, caractérisé en ce que l'unité réceptrice comprend en outre des neuvièmes moyens (314, 316) pour engendrer un état binaire pulsé de la ligne de signaux de retour pour indiquer qu'un signal de donnée de retour est



disponible pour une transmission, et en ce que l'unité émettrice comprend des dixièmes moyens reliés à la ligne de signaux de retour pour détecter l'état binaire pulsé et pour permettre à l'unité émettrice d'émettre un signal de donnée.

21. Système de transmission de données selon

l'une quelconque des revendication 19 et 20, caractérisé en ce qu'il comprend un ensemble d'unités réceptrices reliées aux première et seconde lignes de signaux et à la ligne de signaux de retour.

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