APPLICATION FOR UNITED STATES PATENT

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Formation of a Frontside Contact on Silicon-on-insulator Substrate

RELATED APPLICATION

This application claims priority to and incorporates by reference U.S. Provisional Application Serial No. 60/275,764 filed March 14, 2001.

FIELD

The present invention relates generally to device processing of Silicon-On-Insulator (SOI) wafers, and more particularly, relates to a method of forming a frontside contact to the silicon substrate of a SOI wafer.

BACKGROUND

SOI is a device processing technique that places an insulating layer (e.g. a buried oxide layer) over the silicon substrate. Transistors are then fabricated in a layer of silicon located on top of the insulating layer. This technique may provide higher speeds and use less power by reducing capacitance, making device operation on SOI superior to the conventional Complementary Metal-Oxide Semiconductor (CMOS) techniques.

In many applications it is desirable to ground or bias the silicon substrate of an SOI circuit. However, in most of the more advanced packaging technologies, such as flip chip and die stacking, making a connection to the substrate is cost prohibitive. Therefore, connecting the substrate to a frontside contact is necessary. The standard

semiconductor manufacturing process must typically be modified to make this frontside contact.

Submicron lithography requires a high degree of planarity in the contact dielectric to define the contact and metal interconnect layers. In order to make simultaneous contact to the gate polysilicon, the source/drain regions, and the underlying substrate, the selectivity requirements must be increased significantly to be able to etch the planarized contact dielectric down to the silicon substrate. These requirements increase the cost of manufacturing.

A frontside contact formation process was described by Brady, et al. in U.S. Patent No. 5,314,841, "Method of Forming a Frontside Contact to the Silicon Substrate of a SOI Wafer." This process forms a frontside contact without planarization of the structure as seen in Fig. 1. This requires significant adjustment of the contact etch to be compatible with today's planarized contact dielectric processes.

U.S. Patent Application No. 09/163,687, titled "Method for Forming a Frontside Contact to the Silicon Substrate of a SOI Wafer in the Presence of Planarized Contact Dielectrics," which is assigned to the same assignee as the present invention, describes another technique for forming such a contact. This technique includes a positive profile and a local interconnect as seen in Fig. 2. The positive profile impacts density, while the local interconnect is not required for all SOI processes.

The techniques and structures disclosed herein are believed to improve upon these prior attempts.

SUMMARY

Exemplary embodiments are described for connecting a silicon substrate layer of an SOI wafer to a frontside contact. A hole is etched through a field oxide layer and a buried oxide layer, exposing the silicon substrate layer in the area in which the frontside contact is to be formed. An implant is performed in the silicon substrate layer in the area of the hole. Connection polysilicon is then deposited in the hole and etched to form the frontside contact. A contact dielectric layer is then deposited. A contact hole is etched into the contact dielectric layer and filled with a refractory metal forming a contact plug. A metal pad is then located above the contact plug to provide surface wiring to other components on the wafer. Placing doped spacers in the hole prior to depositing the connection polysilicon can provide additional doping.

BRIEF DESCRIPTION OF THE DRAWINGS

Presently preferred embodiments are described below in conjunction with the appended drawing figures, wherein like reference numerals refer to like elements in the various figures, and wherein:

Fig. 1 is a cross sectional view of the prior art demonstrating a method of forming a frontside contact without planarization of the structure.

Fig. 2 is a cross sectional view of the prior art demonstrating a method of forming a frontside contact using positive profile control and a local interconnect.

Fig. 3 is a cross sectional view of a frontside contact according to a first exemplary embodiment.

Fig. 4 is a cross sectional view of the frontside contact area after removal of top

silicon and deposition of field oxide according to an exemplary embodiment.

Fig. 5 is a cross sectional view of the frontside contact area after etch and implant according to an exemplary embodiment.

Fig. 6 is a cross sectional view of the frontside contact area after connection polysilicon is deposited according to a first exemplary embodiment.

Fig. 7 is a cross sectional view of the frontside contact area after a contact dielectric layer is deposited according to a first exemplary embodiment.

Fig. 8 is a cross sectional view of a frontside contact according to a second exemplary embodiment.

Fig. 9 is a cross sectional view of the frontside contact area after forming spacers according to a second exemplary embodiment.

Fig. 10 is a cross sectional view of the frontside contact area after connection polysilicon is deposited according to a second exemplary embodiment.

Fig. 11 is a flow diagram illustrating a method for forming a frontside contact according to a first exemplary embodiment.

Fig. 12 is a flow diagram illustrating a method for forming a frontside contact according to a second exemplary embodiment.

DETAILED DESCRIPTION

First Exemplary Embodiment

Fig. 3 illustrates a first exemplary embodiment of a frontside contact 100. The frontside contact 100 may contain a silicon substrate layer 102, a buried oxide layer 104, a field oxide layer 106, an implant 112, connection polysilicon 114, a contact dielectric layer 116, a contact plug 118, and a metal pad 120. As shown, the connection

polysilicon 114 connects the silicon substrate layer 102 to the contact plug 118 providing a means to ground or bias the silicon substrate of a Silicon-On-Insulator (SOI) circuit. A method of fabricating the frontside contact 100 is described as follows.

Fig. 4 shows the frontside contact area during initial stages of processing according to an exemplary embodiment. The formation of the frontside contact 100 may begin by removing the top layer of silicon from an SOI wafer in the area in which the frontside contact 100 is to be formed, exposing the buried oxide layer 104. The top layer of silicon is not shown in Fig. 4. For example, the top layer of silicon may be removed using reactive ion etching (RIE). Other etching methods that are selective to the buried oxide layer 104 may also be used. The field oxide layer 106 may then be deposited on the buried oxide layer 104. Deposition may be performed using chemical vapor deposition or any other suitable method. The field oxide layer 106 may act as a protective layer and serve as a doping barrier.

Fig. 5 shows the frontside contact area during additional stages of processing according to an exemplary embodiment. After the field oxide layer 106 is deposited, as shown in Fig. 4, a photoresist 108 with the pattern to be etched may be placed on the field oxide layer 106. A hole 110 may then be etched through the field oxide layer 106 and the buried oxide layer 104, down to the silicon substrate layer 102. A positive profile on the hole 110 may be beneficial, as outlined in a commonly assigned patent application "Method for Forming a Frontside Contact to the Silicon Substrate of a SOI Wafer in the Presence of Planarized Contact Dielectrics" (Serial No. 09/163,687), which is incorporated by reference herein. The choice of an etching technique may be based on factors such as cost effectiveness. According to an exemplary embodiment, an industry standard straight walled RIE plasma etch is used.

After etching has created hole 110, the implant 112 may be performed through the hole 110 to increase the doping in the silicon substrate layer 102. The implant 112 may be either a P+ implant or an N+ implant. The implant 112 may be of sufficient conductivity to provide an electrical connection between the silicon substrate layer 102 and the connection polysilicon 114. According to an exemplary embodiment, a P+ implant 112 of substantially $1.25x10^{15}$ atoms/cm^2 at 70keV is performed in the silicon substrate layer 102 when the connection polysilicon 114 is doped N+, but other implants may be employed. In other embodiments, it may be beneficial to perform an N+ implant or no implant at all. After the implant 112 is performed, the photoresist 108 may be removed and the wafer cleaned.

Fig. 6 shows the frontside contact area during additional stages of processing according to an exemplary embodiment. The connection polysilicon 114 may be deposited on the wafer. The connection polysilicon 114 may be doped N+ or P+. Doping may be performed either before or after deposition. The choice of dopant and the timing of the doping may be determined based on other fabrication requirements on the wafer. For example, if other N+ doped polysilicon is needed for gate fabrication on the wafer, the same material may be used to form frontside contact 100 (See Fig. 3).

The connection polysilicon 114 may then be etched. A photoresist is typically used to define the edges of the connection polysilicon 114 prior to the etching process. The photoresist is not shown in Fig. 6. Any etching process that is compatible with the connection polysilicon 114 may be employed. According to an exemplary embodiment, this photoresist and etch process would occur concurrently with gate processing on the wafer. While Fig. 6 shows an exemplary embodiment of the connection polysilicon 114 after etching, the connection polysilicon is not limited to this shape. Any shape that

provides a means to connect the silicon substrate layer 102 to the contact plug 118 may be employed.

Fig. 7 shows the frontside contact area during additional stages of processing according to an exemplary embodiment. The contact dielectric layer 116 may be deposited on the wafer. Planarization may then be performed to provide a flat surface on the wafer. Chemical mechanical polishing is performed in an exemplary embodiment, but other planarization techniques may also be employed. Since the frontside contact 100 may be at the same elevation as a normal gate contact, no additional selectivity requirements are necessary relative to a process flow that does not include the frontside contact 100.

Referring back to Fig. 3, a contact hole may then be etched through the contact dielectric layer 116. A refractory metal may be deposited in the contact hole to form the contact plug 118. In an exemplary embodiment, tungsten is employed; however, other metals, such as copper or aluminum, may also be suitable for this purpose. Other methods of connecting the connection polysilicon 114 to the top layer of the wafer may also be used. The metal pad 120 is located above the contact plug 118 to provide surface wiring to other components on the wafer. The metal pad 120 may be aluminum, but other conducting materials may be used for this purpose.

A silicide may be located between the contact plug 118 and the connection polysilicon 114. The silicide is not shown in Fig. 3. The silicide may be formed during the heat treatment step of alloying or may be deposited on the connection polysilicon 114 prior to depositing contact plug 118. Other barrier layers may also be employed. In another alternative embodiment, the silicide may not be used in forming the frontside contact 100.

Fig. 11 provides a flow diagram illustrating a method of forming the frontside contact 100 according to an exemplary embodiment. Method 1100 summarizes the process described above with reference to Fig. 3 through Fig. 7.

Second Exemplary Embodiment

Fig. 8 illustrates a frontside contact 800 in accordance with another exemplary embodiment. The frontside contact 800 contains a silicon substrate layer 102, a buried oxide layer 104, a field oxide layer 106, an implant 112, connection polysilicon 114, a contact dielectric layer 116, a contact plug 118, a metal pad 120 and spacers 122. As shown, the connection polysilicon 114 connects the silicon substrate 102 to the contact plug 118 providing a means to ground or bias the silicon substrate of a SOI circuit.

Frontside contact 800 contains spacers 122 to provide additional doping. Spacers 122 may be needed when a circuit design requires a thick buried oxide layer 104. For example, if the frontside contact 800 thickness is in the range of 10,000 to 20,000 Angstroms, spacers 122 may be needed to provide sufficient doping. A method of fabricating the frontside contact 800 is described as follows.

Fig. 4 shows the frontside contact area during initial stages of processing according to an exemplary embodiment. The formation of the frontside contact 800 may begin by removing the top layer of silicon from an SOI wafer in the area in which the frontside contact 800 is to be formed, exposing the buried oxide layer 104. The top layer of silicon is not shown in Fig. 4. For example, the top layer of silicon may be removed using RIE. Other etching methods that are selective to the buried oxide layer 104 may also be used. The field oxide layer 106 may then be deposited on the buried oxide layer 104. Deposition may be performed using chemical vapor deposition or any other suitable method. The field oxide layer 106 may act as a protective layer and serve

as a doping barrier.

Fig. 5 shows the frontside contact area during additional stages of processing according to an exemplary embodiment. After the field oxide layer 106 is deposited, as shown in Fig. 4, a photoresist 108 with the pattern to be etched may be placed on the field oxide layer 106. A hole 110 may then be etched through the field oxide layer 106 and the buried oxide layer 104, down to the silicon substrate layer 102. A positive profile on the hole 110 may be beneficial, as outlined in a commonly assigned patent application "Method for Forming a Frontside Contact to the Silicon Substrate of a SOI Wafer in the Presence of Planarized Contact Dielectrics" (Serial No. 09/163,687), which is incorporated by reference herein. The choice of an etching technique may be based on factors such as cost effectiveness. According to an exemplary embodiment, an industry standard straight walled RIE plasma etch is used.

After etching has created hole 110, the implant 112 may be performed through the hole 110 to increase the doping in the silicon substrate layer 102. The implant 112 may be either a P+ implant or an N+ implant. The selection of implant dopant may be determined based on the dopant type of spacers 122 and the connection polysilicon 114. For example, if the spacers 122 and connection polysilicon 114 are P+, then a P+ implant may be preferred. The implant 112 may be of sufficient conductivity to provide an electrical connection between the silicon substrate layer 102 and the connection polysilicon 114. According to an exemplary embodiment, a P+ implant 112 of substantially 1.25×10^{15} atoms/cm^2 at 70keV is performed in the silicon substrate layer 102, but other implants may be employed. In other embodiments, it may be beneficial to perform an N+ implant or no implant at all. After the implant 112 is performed, the photoresist 108 may be removed and the wafer cleaned.

Fig. 9 shows the frontside contact area during additional stages of processing according to an exemplary embodiment. In an exemplary embodiment, borosilicate glass may be deposited in the hole 110 and etched back to form spacers 122 along the frontside contact sidewalls 124. Borosilicate glass spacers may provide additional P+ doping. Any deposition and etching technique that is selective to borosilicate glass may be employed. Borosilicate glass is chosen as a doping source in an exemplary embodiment; however, other dopant materials may be used, including those that provide N+ doping.

Fig. 10 shows the frontside contact area during additional stages of processing according to an exemplary embodiment. The connection polysilicon 114 may be deposited on the wafer. In an exemplary embodiment, the connection polysilicon 114 may be deposited as undoped polysilicon. The connection polysilicon 114 may be doped N+ or P+ after deposition. In an alternative embodiment, the connection polysilicon 114 may be doped prior to or insitu during deposition. The selection of dopant type may be based upon the dopant type of the implant 112 and the spacers 122. For example, if the implant 112 and the spacers 122 are P+, then the connection polysilicon 114 may be doped P+. Other embodiments may employ different combinations of dopant types. For example, the implant 112, the spacers 122, and the connection polysilicon 114 may all be doped N+.

The connection polysilicon 114 may then be etched. A photoresist is typically used to define the edges of the connection polysilicon 114 prior to the etching process. The photoresist is not shown in Fig. 10. Any etching process that is compatible with connection polysilicon 114 may be employed. According to an exemplary embodiment, this photoresist and etch process would occur concurrently with gate processing on the

wafer. While Fig. 10 shows an exemplary embodiment of the connection polysilicon 114 after etching, the connection polysilicon is not limited to this shape. Any shape that provides a means to connect the silicon substrate layer 102 to the contact plug 118 may be employed.

The source/drain/gate implants and anneals associated with typical Metal Oxide Semiconductor (MOS) transistor fabrication methods may be sufficient to dope a top region of the connection polysilicon 114. However, in a case of a deep and narrow frontside contact 800 opening, a dopant may not substantially diffuse to the interface of the silicon substrate layer 102. Out diffusion from the doped spacers 122 may provide for doping of the connection polysilicon 114 substantially to the interface of the silicon substrate layer 102.

Referring back to Fig. 8, the contact dielectric layer 116 may be deposited on the wafer. Planarization may then be performed to provide a flat surface on the wafer. Chemical mechanical polishing is performed in an exemplary embodiment, but other planarization techniques may also be employed.

A contact hole may then be etched through the contact dielectric layer 116. A refractory metal may be deposited in the contact hole to form the contact plug 118. In an exemplary embodiment, tungsten is employed; however, other metals, such as copper or aluminum, may also be suitable for this purpose. Other methods of connecting the connection polysilicon 114 to the top layer of the wafer may also be used. The metal pad 120 is located above the contact plug 118 to provide surface wiring to other components on the wafer. The metal pad 120 may be aluminum, but other conducting materials may be used for this purpose.

A silicide may be located between the contact plug 118 and the connection polysilicon 114. The silicide is not shown in Fig. 8. The silicide may be formed during the heat treatment step of alloying or may be deposited on connection polysilicon 114 prior to depositing contact plug 118. Other barrier layers may also be employed. In another alternative embodiment, the silicide may not be used in forming the frontside contact 800.

Fig. 12 provides a flow diagram illustrating a method of forming the frontside contact 800 according to an exemplary embodiment. Method 1200 summarizes the process described above with reference to Figures 4, 5, 8, 9, and 10.

Although two exemplary embodiments have been disclosed herein, other variations may be made without departing from the intended scope of the invention. For example, a variety of semiconductor fabrication techniques, including various methods of etching and deposition, may be employed without departing from the scope of the invention itself. The claims should not be read as limited to the described order or elements unless stated to that effect. Therefore, all embodiments that come within the scope and spirit of the following claims and equivalents thereto are claimed as the invention.

WE CLAIM:

The embodiments of the invention in which an exclusive property or right is claimed are defined as follows:

1. A frontside contact on a silicon-on-insulator substrate, comprising in combination:

a contact plug;

a plurality of layers including at least a field oxide layer and a buried oxide layer, wherein a hole is etched through the field oxide layer and the buried oxide layer exposing a substrate layer; and

a connection polysilicon providing a connection between the substrate layer and the contact plug, wherein the connection provides a means to bias the substrate layer.

2. The contact of Claim 1, wherein the contact plug is a metal.

3. The contact of Claim 2, wherein the metal is tungsten.

4. The contact of Claim 1, wherein the substrate layer has a doped region below the hole.

5. The contact of Claim 4, wherein the doped region is doped with a P+ implant.

6. The contact of Claim 5, wherein the P+ implant is substantially an implant of $1.25x10^{15}$ atoms/cm^2 at 70keV.

7. The contact of Claim 4, wherein the doped region is doped with an N+ implant.

8. The contact of Claim 4, wherein the doped region provides an electrical connection between the silicon substrate layer and the connection polysilicon.

9. The contact of Claim 4, wherein the connection polysilicon substantially contacts the doped region in the substrate layer.

10. The contact of Claim 1, wherein a metal pad is substantially located above the contact plug.

11. The contact of Claim 1, wherein a silicide is substantially located between the connection polysilicon and the contact plug.

12. The contact of Claim 1 wherein a contact dielectric layer is substantially located above the field oxide layer.

13. The contact of Claim 1, further comprising at least one spacer disposed in the hole, wherein the at least one spacer is composed of borosilicate glass to provide additional doping.

14. A frontside contact on a silicon-on-insulator substrate, comprising in combination:

a contact plug;

a plurality of semiconductor layers including at least a field oxide layer and a buried oxide layer, wherein a hole is etched through the field oxide layer and the buried oxide layer exposing a substrate layer;

at least one spacer disposed in the hole to provide additional doping; and

a connection polysilicon providing a connection between the substrate layer and the contact plug, wherein the connection provides a means to bias the substrate layer.

15. The contact of Claim 14, wherein the at least one spacer is composed of borosilicate glass.

16. The contact of Claim 14, wherein the contact plug is a metal.

17. The contact of Claim 16, wherein the metal is tungsten.

18. The contact of Claim 14, wherein the substrate layer has a doped region below the hole.

19. The contact of Claim 18, wherein the doped region is doped with a P+ implant.

20. The contact of Claim 19, wherein the P+ implant is substantially an implant of $1.25x10^{15}$ atoms/cm^2 at 70keV.

21. The contact of Claim 18, wherein the doped region provides an electrical connection between the silicon substrate layer and the connection polysilicon.

22. The contact of Claim 18, wherein the connection polysilicon substantially contacts the doped region in the substrate layer.

23. The contact of Claim 14, wherein a metal pad is substantially located above the contact plug.

24. The contact of Claim 14, wherein a silicide is substantially located between the connection polysilicon and the contact plug.

25. The contact of Claim 14, wherein a contact dielectric layer is substantially located above the field oxide layer.

26. A frontside contact on a silicon-on-insulator substrate, comprising in combination:

a tungsten contact plug, wherein a metal pad is located substantially above the tungsten contact plug;

a plurality of semiconductor layers including at least a field oxide layer and a buried oxide layer, wherein a hole is etched through the field oxide layer and the buried oxide layer exposing a substrate layer, wherein the substrate layer has a P+

implant region below the hole that is substantially doped with an implant of $1.25x10^{15}$ atoms/cm^2 at 70keV, and wherein a contact dielectric layer is substantially located above the field oxide layer; and

a connection polysilicon providing a connection between the doped region of the substrate layer and the tungsten contact plug, wherein a silicide is substantially located between the connection polysilicon and the tungsten contact plug, and wherein the connection provides a means to bias the substrate layer.

27. The contact of Claim 26, further comprising at least one spacer disposed in the hole, wherein the at least one spacer is composed of borosilicate glass to provide additional doping.

28. A method of forming a frontside contact on a silicon-on-insulator substrate, comprising in combination:

removing a top layer of silicon in an area where the frontside contact is to be formed, thereby substantially exposing a buried oxide layer;

depositing a field oxide layer on the buried oxide layer;

etching a hole through the field oxide layer and the buried oxide layer to a substrate layer;

performing an implant in the substrate layer through the hole;

depositing a connection polysilicon;

etching the connection polysilicon;

depositing a contact dielectric layer; and

forming a contact plug.

29. The method of Claim 28, further comprising forming a metal pad substantially above the contact plug.

30. The method of Claim 28, further comprising depositing and etching at least one spacer to provide additional doping after the step of performing an implant.

31. The method of Claim 30, wherein the at least one spacer is composed of borosilicate glass.

32. The method of Claim 28, wherein the step of removing a top layer of silicon includes employing reactive ion etching.

33. The method of Claim 28, wherein the step of etching a hole includes applying photoresist to substantially define the location to be etched.

34. The method of Claim 28, wherein the step of etching a hole includes performing a straight wall etch.

35. The method of Claim 28, wherein the step of performing an implant includes performing a P+ implant of substantially 1.25×10^{15} atoms/cm^2 at 70keV.

36. The method of Claim 28, wherein the step of etching the connection polysilicon includes applying photoresist to substantially define a location to be etched.

37. The method of Claim 28, wherein the step of forming a contact plug includes etching a contact hole in the contact dielectric layer.

38. The method of Claim 28, wherein the step of forming a contact plug includes depositing a metal in the contact hole.

39. The method of Claim 38, wherein the metal is tungsten.

40. The method of Claim 38, whercin a silicide is substantially located between the metal and the connection polysilicon.