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WIDEBAND DUAL AMPLIFIER CIRCUITS

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BACKGROUND OF THE INVENTION**Field Of The Invention**

The present invention generally relates to amplifier circuits providing wideband amplification with minimal noise, and in particular, to amplifier circuits utilizing pairs of functionally complementing devices.

Description Of The Related Art

A gain-bandwidth product as well as a noise factor of a field effect transistor (hereinafter "FET") limits the FET's ability to amplify low-level voltage input signals over a wide range of frequencies. Additionally, a gain-bandwidth product as well as a noise factor of a magnetic tunnel junction device (hereinafter "MTJ") limits the MTJ's ability to amplify low-level current input signals over a wide range of frequencies.

In radio frequency and microwave circuits, the gain of amplifiers utilizing a FET or MTJ as an active filter can be increased by narrowing the pass band of the FET or MTJ. However, that gain responses are not flat and often have phase discontinuities. Furthermore, the noise performance is poorer when stages are cascaded.

The high frequency electronic industry is therefore continually striving to improve the gain-bandwidth product of amplifying circuits.

SUMMARY OF THE INVENTION

The present invention relates to an amplifier circuit which utilizes duality of devices to provide high gain-bandwidth product.

A FET and MTJ are connected in functional cascade to best utilize the amplification, impedance, noise, and operating mode characteristics of each device. This composite utilizes a synergistic improvement in the gain bandwidth of such cascaded pair. In one form the MTJ input is the load of the FET. In another form, the FET input (gate electrode) is the load of the MTJ. The FET/MTJ composite matches respective desirable impedance characteristics while eliminating the noise introduced by resistors in conventional cascade configurations.

The foregoing forms and other forms, features and advantages of the invention will become further apparent from the following detailed description of the presently preferred embodiments, read in conjunction with the accompanying drawings. The detailed description and drawings are merely illustrative of the invention rather than limiting, the scope of the invention being defined by the appended claims and equivalents thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 depicts small signal models of a FET and a MTJ;

FIG. 2 depicts cascaded FET and MTJ amplifiers;

FIG. 3a depicts a dual voltage amplifier employing the duality concept of the present invention;

FIG. 3b depicts a dual current amplifier employing the duality concept of the present invention;

FIG. 3c depicts a cascaded dual voltage amplifier employing the duality concept of the present invention;

FIG. 3d depicts a small signal model for the amplifier in **FIG. 3a**;

FIG. 4 is a schematic of a MTJ in accordance with the present invention;

FIG. 5 is a magnetoresistive response curve of the **FIG. 4** MTJ; and

FIG. 6 is a portion of the **FIG. 5** magnetoresistive response curve that is applicable to an operation of the **FIG. 3a** amplifying circuit.

DETAILED DESCRIPTION OF THE

PRESENTLY PREFERRED EMBODIMENTS

Two electrical circuits are said to be dual of one another if they obey identical circuit equations, but with the roles of current and voltages interchanged. In general, a dual circuit can be constructed by the parameter/configuration interchanges set forth in TABLE 1.

TABLE 1

FIRST ELECTRICAL CIRCUIT	SECOND ELECTRICAL CIRCUIT
current I	voltage V
electric field E	magnetic field M
resistance R	conductance G
inductance L	capacitance C
charge Q	magnetic flux Φ
open circuit	close circuit
series connection	parallel connection
node	Mesh

The semiconductor field-effect transistors and the magnetic tunnel junction behave like active dual elements. The FETs are voltage-controlled, i.e. the voltage at the gates control the channel (output) currents, the gate poses a capacitive impedance, and the differential channel impedance is high – ideally a current source. The MTJs are current-controlled, i.e. current through the control lines controls the output voltages, the control lines poses an inductive impedance, and the differential channel impedance is low – ideally a voltage source.

The important small-signal parameters for the FET and MTJ are listed in TABLE 2.

TABLE 2

FET	MTJ
Transconductance g_m	Transresistance r_m
Input capacitance C_i	Input inductance L_i
GB produce $\omega_v = g_m / C_i$	GB produce $\omega_v = r_m / L_i$
Voltage gain $A_v = g_m r_m$	Current gain $A_c = r_m g_c$
Output resistance $r_v = \partial V_{ds} / \partial I_{ds}$	Output conductance $g_c = \partial I_J / \partial V_J$

If one were to cascade individual FET amplifier stages or the MTJ stages as depicted in FIG. 2, one would always have amplifiers with maximum GB product ω_v or ω_c , and noise characteristics worse than that of individual stage.

Given a semiconductor FET 20 with GB product ω_v and a MTJ 30 dual with GB product ω_c , the dual amplifier 10 in FIG. 3a can attain signal gain and power gain for a bandwidth ω_h , which is greater than either ω_v or ω_c . A unique characteristic of this amplifier 10 is that it has no "load" elements; the dual devices FET 20 and MJT 30 simply transduce voltages to currents and vice versa.

The voltage gain of dual voltage amplifier 10 in FIG. 3a and the current gain of dual current amplifier 40 in FIG. 3b are represented by the following equation (1):

$$A_h = g_m r_m \quad (1)$$

where g_m is the transconductance of FET 20 and r_m is the transresistance of MTJ 30 at the operating point. The FET 20 stage with high output impedance drives the low (inductive) input impedance of the MTJ 30 and the low output impedance of the MTJ 50 drive the high (capacitive) input impedance of the FET 60. This results in the ultra-wide bandwidth response with good gain flatness. If r_v is the small-signal output impedance of the FET (20 or 60), and g_c is the small-signal output

conductance of the MTJ (30 or 50), the GB product of the hybrid amplifier (10 or 40) is given by the following equation (2):

$$\omega_h = (g_m r_m) / ((L_i / r_v) + (C_i / g_c)) \quad (2)$$

where L_i and C_i are the input inductance of the magnetically coupled MTJ (30 or 50) and the input capacitance of the FET (10 or 40), respectively. Interestingly, ω_h is independent of the width of the FET (10 or 40) and the length or number of the series-connected MTJs (30 or 50). This is because g_m , C_i , and r_v^{-1} are proportional to the width of the FET (10 or 40), and r_m , L_i , and g_c^{-1} are proportional to the length of the MTJ (30 or 50). The dual amplifier (10 or 40) each comprising a FET and a MTJ acts like a single stage with the GB product representing the correct performance measure. By algebraic manipulations, ω_h can be expressed in terms of the (maximum possible) voltage gain of the FET ($A_v = g_m r_v$) and the (maximum possible) current gain of the magnetically coupled MTJ ($A_c = r_m g_c$), the GB product of the FET (ω_v), and the BF product of the MTJ (ω_c) as represented by the following equation (3):

$$1/\omega_h = (1/A_v \omega_c) + (1/A_c \omega_v) \quad (3)$$

If both A_v and A_c are much larger than unity, it follows that ω_h is much larger than ω_v and ω_c . This is a remarkable result since GB product is the more important parameter of a wideband amplifier.

There are three specific reasons why the noise of the dual amplifiers (10 or 40) is low: First, an absence of load resistors, and the Johnson noise associated with the resistors. Second, the individual stages are coupled magnetically. Hence the ground bounce or voltage disturbances in the power supply or ground leads of each individual stage can be isolated and not propagated through the cascaded chain. Finally, the widths of the transistors and the lengths of the MTJ or number of MTJs can be increased without significantly affecting the gain-bandwidth product. Wide transistors or increasing the number of MTJs can reduce both the Johnson noise and the $1/f$ noise.

FIG. 3c depicts a multiple stage cascaded configuration of dual amplifiers **10** further utilizing the duality concept in each successively connected stage. Thereby, the MTJ output of each dual amplifier stage is connected to the FET input of the successive dual amplifier stage. A corresponding cascade configuration is attainable using dual amplifier **40** as depicted in **FIG. 3b**.

The schematic in **FIG. 3d** depicts a small signal model for dual amplifier **10** in **FIG. 3a**. The selective match of device characteristics is readily apparent when compared to the individual FET and MTJ small signal models depicted in **FIG. 1**.

Referring to **FIG. 4**, MTJ **30** is shown in detail. MTJ **30** includes electrode **21**, a free ferromagnet **22**, a tunnel barrier **23**, a pinned ferromagnet **24**, an antiferromagnet **25**, and electrode **26**. Electrode **26**, e.g. Ti, Ti/PD or Ta/Pt, formed on a substrate **27**, e.g. Si, quartz, N58. Antiferromagnet **25**, e.g. MnFe or IrMn, is formed on electrode **26**. Pinned ferromagnet **24**, e.g. CoFe, or NiFe/CoFe, is formed on antiferromagnet **25**. Tunnel barrier **23**, e.g. Al_2O_3 , is formed on pinned ferromagnet **24**. Free ferromagnet **22**, e.g. CoFe/NiFe, is formed on tunnel barrier **23**. Electrode **21**, e.g. Ti, Ti/PD or Ta/Pt, formed on free ferromagnet **22**.

Referring to **FIGS. 5** and **6**, curves **28** are representative of a change in the magnetoresistance of MTJ **30** as an internal magnetic field decreasing in strength is applied parallel to free ferromagnet **22** and pinned ferromagnet **24**. Curves **29** are representative of a change in the magnetoresistance of MTJ **30** as the internal magnetic field of increasing strength is applied parallel to free ferromagnet **22** and pinned ferromagnet **24**. Curves **28** and **29** illustrate an approximate 36% change over a range of ± 20 Oe. Accordingly, for dual amplifying circuit **10** (**FIG. 3a**), the current through FET **20** must be maintained in a range of current levels that generates the internal magnetic field over the range of ± 20 Oe, and for dual amplifying circuit **40** (**FIG. 3b**), a current input signal I_1 must be maintained in a range of current levels that generates the internal magnetic field over the range of ± 20 Oe.

From the description of desirable electronic characteristics attributed to FET 20 in connection with **FIGS. 3a** and **3b**, one skilled in the art will be able to make and use dual amplifying circuits in accordance with the present invention wherein the FETs are replaced by a different type of field effect device. Additionally, from the description of MTJs **30** and **50** in connection with **FIGS. 3a** and **3b**, one skilled in the art will be able to make and use dual amplifying circuits in accordance with the present invention wherein the MTJs are replaced by a different type of active magnet or spintronic device.

While the embodiments of the present invention disclosed herein are presently considered to be preferred, various changes and modifications can be made without departing from the spirit and scope of the invention. The scope of the invention is indicated in the appended claims, and all changes that come within the meaning and range of equivalents are intended to be embraced therein.

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CLAIMS

1. A amplifying circuit, comprising:

a two or more pairs of active devices, each pair of active devices comprising a field effect device and a magnetic tunnel junction active device; and configured so that one type of active device is the input for all of the active pairs and the other is the output; and

an electrical connection between said pairs of active devices whereby a output of a preceding pair of active devices is an input to a subsequent pair of active devices.

2. The dual amplifying circuit of claim 1, further comprising:

a current source device connected in an output path of each magnetic tunnel junction active device.

3. The dual amplifying circuit of claim 1 or 2, further comprising:

a supply of voltage connected in an output path of field effect active device.

4. The amplifying circuit of claim 1, 2 or 3 wherein

each field effect active device is a field effect transistor.

5. The amplifying circuit of claim 4, wherein

a source/drain electrode of said field effect transistor is coupled to drive an input electrode of said magnetic tunnel junction active device.

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6. The amplifying circuit of claim 5, further comprising:

a current source, wherein

an input signal is coupled to a gate electrode of said field effect transistor,
and

an output signal is detected from an electrode coupled between an output
electrode of said magnetic tunnel junction active device and said current source.

7. The amplifying circuit of claim 1, wherein

an output electrode of each magnetic tunnel junction active device is coupled
to drive a gate electrode of each field effect transistor.

8. The amplifying circuit of claim 7, wherein an input signal is coupled to an
input electrode of the magnetic tunnel junction active device and the gate electrode
of the field effect transistor is coupled between the output electrode of the magnetic
tunnel junction active device and a current source.