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A Lead Frame for a Semiconductor Device and a Method for Manufacturing a Semiconductor Device Using the Lead Frame

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a lead frame for a semiconductor device and a method for manufacturing a semiconductor device using the lead frame and, more specifically, it relates to a lead frame employed in a method for manufacturing a resin-sealed type semiconductor device and to a method for manufacturing a semiconductor device using the lead frame.

Description of the Prior Art

Fig. 1 shows a lead frame employed in a method of manufacturing a conventional integrated circuit. The lead frame has a prescribed pattern which is formed by etching or pressing a thin metal plate. Referring to the figure, a tie bar 1 connects outer leads 2. Inner leads 3 extend to the side of a central dice pad 4 and after sealing, they will be contained in the resin. Meanwhile, hatched portions in the figure show the Ag or Au plated portions which facilitate the junction of semiconductor chips and the connection by Au wire, etc., between the electrodes of the semiconductor chip and the inner leads 3.

Referring to Fig. 2, a chip 5 is attached to the dice pad 4 and the electrodes of the chip 5 and the inner leads 3 are in electrical connection to each other by fine lead wires 6 of, for example, Au. After the structure of Fig. 2 is obtained, a lead frame 11 is interposed between the upper mold 9 and the lower mold 10 of an injection mold, as shown in Fig. 3. Then, a thermosetting resin such as epoxy resin is injected to the cavity using the low pressure transfer molding, etc., to form a resin layer 8. The molded frame is shown in Fig. 4.

12 denotes a thin film (hereinafter referred to as a bur) which is formed by the resin entered the gap between the mold and the frame. The bur 12 occurs according to the flatness precision of the mold, the dispersion of plate thickness of the lead frame, uniformity of pressure of the press clamping the mold, the fluidity of the sealing resin and the die ware due to the frame treatment. The bur causes an inconvenience that the plating can not be carried out on the outer lead in a subsequent process. Therefore, the bur 12 is eliminated by the dry honing or the wet honing after the molding. In addition, a bur eliminating method using high water pressure is employed after the electrolytic flash cutting.

A conventional lead frame is formed as described above. However, the bur eliminating process as above is

essentially an undesired one. Meanwhile, when the honing is carried out, a package as well as the bur is damaged, the surface of the lead frame is made rough and the frame becomes slender, causing a problem such as the generation of plating needle deposition or less lead strength. There is also a problem in the bur eliminating method using electrolysis and high water pressure. Namely, a thick bur can not perfectly be eliminated according to the method. In addition, the necessary bur eliminating process and facilities as above rises the cost of the products.

SUMMARY OF THE INVENTION

The present invention was made to eliminate the above described problems and a principal object of the present invention is to suppress the generation of bur as little as possible during the resin sealing process, and to dispense with a special bur eliminating process and facilities, without damaging the resin and the lead.

A lead frame according to the present invention comprises a dice pad for mounting a chip placed in the central portion, inner leads, a tie bar and outer leads disposed around the dice pad, a thin metal layer which is hard to melt and easily transformed, formed on the surface of that portion of the inner leads, outer leads and tie bar which is not covered by the sealing resin.

The thin metal layer of the present invention has less hardness so that it is transformed to fill the gap between the mold and the lead frame when the lead frame is clamped with the mold in the molding process. When the resin is injected into the cavity of the mold, the resin hardly enters the gap between the mold and the lead frame since the thin metal layer occupies the gap. Consequently, undesired generation of the bur can be prevented.

These objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a perspective view of a conventional lead frame.

Fig. 2 is a perspective view showing a step of a method for manufacturing a semiconductor device using the conventional lead frame of Fig. 1.

Fig. 3 is a cross sectional view showing another step of the manufacturing method using the conventional lead frame.

Fig. 4 is a perspective view showing a further step of the manufacturing method using the conventional lead frame.

Fig. 5 is a perspective view showing a step of a method for manufacturing a semiconductor device using a lead frame of one embodiment of the present invention.

Fig. 6 is a perspective view showing another step of the manufacturing method using the lead frame of the present invention.

Fig. 7 is a cross sectional view showing a further step of the manufacturing method using the lead frame of the present invention.

Figs. 8 and 9 are perspective views showing the resin sealing process.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to Fig. 5, a lead frame 20 is formed of a thin metal plate and it has a prescribed pattern formed by etching or pressing. The lead frame 20 has a dice pad 21 for mounting a chip in the central portion. A plurality of inner leads 22 are disposed around the dice pad 21 with a spacing with each other. A plurality of outer leads 23 are formed near the dice pad 21 far off from the inner leads 22. The inner leads 22 and the outer leads 23 are connected integrally by a tie bar 24.

Lead plated portions 25 are formed on the surface of those portions of the inner leads 22, the outer leads 23 and the tie bar 24 which will not be covered with the sealing resin (package) in the subsequent process. The lead plated portions 25 are formed on the upper surface, the rear surface and the side of the inner leads 22, the outer leads 23 and the tie bar 24 from the external periphery of the sealing resin which is provided in the subsequent process to the portion slightly extend over the tie bar 24. The range usually corresponds to that range of the final product which remains exposed with no covering of the sealing resin. The plating thickness of the lead plating portion 25 is in the range of about 1μ ~ 20μ, according to the dimension accuracy of the mold or the lead frame and to the pressure of clamping of the press. A range of 5μ ~ 10μ is preferable.

Referring to Fig. 5, the hatched portions are the Ag or Au plated portions 26 which facilitate the junction of the semiconductor chip and the connection between the electrodes of the semiconductor chip and the inner leads 22 by, for example, Au wires. The above described lead plated portions 25 can be more easily formed by simultaneously plating in the plating process of the plated portion 26.

Next, a method for manufacturing a semiconductor device using the said lead frame 20 will be described.

First, a semiconductor chip 27 is attached to the dice pad 21 in the central portion of the lead frame 20 of Fig. 5, as shown in Fig. 6, and then a fine wire 28 of for example Au is applied to electrically connect the electrode of the chip 27 and the inner leads 22. The junction temperature of the semiconductor chip 27 is about 200°C when resin junction is carried out, while the junction temperature of the fine wire 28 is about 250°C.

Then, as shown in Fig. 7, the lead frame 20 is interposed between the upper mold 30 and the lower mold 31 of the metal mold. Then, a thermosetting resin such as epoxy resin is injected in the cavity 32 using, for example, the low pressure transfer molding, forming a resin layer 33. The temperature of the mold is about 180°C at the time of resin sealing.

Now, the melting point of the lead is 327°C, so that the lead plated portion 25 do not melt during the manufacturing process. Meanwhile, lead has less hardness so that it is easily transformed when the lead frame 20 is pressed by the mold and it eliminates the gap between the mold and the lead frame 20. Therefore, the lead plated portions 25 occupies the gap between the metal mold and the lead frame 20, preventing of the entrance of the

introduced resin. Consequently, the undesired bur is not generated at that portion. Namely, the lead plated portions 25 occupy the gap between the lead frame 20 and the upper mold 30 and the lower mold 31 by the transformation due to the clamping pressure of the press, preventing the out flow of the resin which forms the bur. Meanwhile, if the resin outflows between the lead plated portion 25 and the mold, the bur will be deposited on the lead plated portion 25.

After the resin sealing, usually a solder plating is carried out on the outer leads 23 in order to enhance the facility of lead soldering. During this process, by dipping the lead plating into a solution for pealing or removing the layer (15% solution of nitric acid), the lead plating can be easily removed and, at the same time, the bur deposited on the lead plating is completely eliminated. Fig. 8 is a perspective view of the lead frame 20 after the molding process. When this structure is subjected to the peeling process, the lead plated portions 25 on the leads 22, 23 and the tie bar 24 are completely eliminated as shown in Fig. 9. Even if the resin is deposited on the lead plated portions 25, it will be completely eliminated with the melting of the lead plated portions 25.

As described above, by providing a soft thin metal layer such as lead on the lead frame of the resin outflowing portion during the resin sealing of the manufacturing process of a semiconductor device, the generation of burs during the sealing process can be prevented and, if there is a little outflow, it will be completely eliminated during the peeling process of the plating process. In addition, conventional bar eliminating process and facilities such as honing can be eliminated.

Although lead is used as a plating material in the above described embodiment, other metals (for example Ag, Sn) can be used. These metals must not be melt at the temperature of the semiconductor chip junction, the fine wire connection for electrically connecting the electrodes of the semiconductor chip and the inner leads and the resin sealing. They must also have the hardness such that it is easily transformed when the lead frame is pressed by the metal mold during the molding process. Although plating is employed in the above described embodiment as a method for depositing lead onto the lead frame 20, other method such as pressure welding of a thin film or frame coating can be employed.

Although the present invention has been described and illustrated in detail, it is clearly understood that the

same is by way of illustration and example only and is not to be taken by way of limitation, the scope of the present invention being limited only by the terms of the appended claims.



CLAIMS:

1. A lead frame for a semiconductor device comprising:

a dice pad disposed in a central portion for mounting a semiconductor chip;

an inner lead, a tie bar and an outer lead disposed around the dice pad to be at least partly covered by sealing resin for encapsulating the semiconductor chip; and

a thin metal layer which is hard to melt and is more easily deformed by pressure than the metal of the lead frame formed on the surface of that portion of the inner lead, outer lead and tie bar which is not covered with the sealing resin.

2. A lead frame for a semiconductor device according to claim 1, wherein said thin metal layer comprises a lead plated layer.

3. A lead frame for a semiconductor device according to claim 1, wherein the thickness of said thin metal layer is 1μ - 20μ.

4. A method for manufacturing a semiconductor device comprising the steps of:

preparing a lead frame for a semiconductor device comprising: a dice pad disposed in a central portion for mounting a semiconductor chip; an inner lead, a tie bar and an outer lead disposed around the dice pad to be at least partly covered by sealing resin for encapsulating the semiconductor chip; and a thin metal layer which is hard to melt and is more easily formed on the surface of that portion of the inner lead, outer lead and tie bar which is not covered with the sealing resin;

mounting a semiconductor chip on said lead frame;

sandwiching said lead frame containing the semiconductor chip within an upper mould and a lower mould of an injection mould so that a gap between said lead frame and said upper mould and said lower mould is filled while said thin metal layer is deformed by clamping pressure;

injecting a resin material into the cavity of said injection mould; and

ejecting said resin moulded lead frame out of said injection mould; and

removing said thin metal layer of said lead frame.

5. A method for manufacturing a semiconductor device according to claim 4, wherein said step of removing said thin metal layer comprises the step of dipping the lead frame into a solution for removing said thin metal layer before solder plating of the lead frame.

6. A method for manufacturing a semiconductor device according to claim 5, wherein said thin metal layer is a

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layer of lead and, said solution for removing the layer is of a 15% solution of nitric acid.

7. A lead frame for a semiconductor device, substantially as described with reference to, or as shown in, Figures 5 to 9 of the drawings.

8. A method of manufacturing a semiconductor device, substantially as described with reference to Figures 5 to 9 of the drawings.