

**METHOD AND SYSTEM FOR TESTING INTEGRATED CIRCUIT
DEVICES AT THE WAFER LEVEL**

ABSTRACT

A method and system are disclosed that utilize a passive electrical network for wafer-level testing of integrated circuit devices. According to the present invention, multiple integrated circuit devices (24) are formed on a semiconductor wafer (10) in a fabrication process. During, and as a part of the process by which the integrated circuit devices (10) are fabricated on the wafer (10), conductive traces (160, 180), conductive straps (220) and test pads (300) are deposited onto otherwise unoccupied areas (14) of the wafer (10). The conductive straps (220) are utilized both to strategically interconnect the conductive traces (160, 180) and also to connect the traces (160, 180) to input/output contacts (18, 22) on the integrated circuit devices (24). The test pads (300) are formed on the unused peripheral regions of the wafer (10) and are electrically connected to the conductive trace (160, 180) network. An on-wafer electrical testing structure is thereby formed from which the integrated circuit devices (24) can be tested prior to being cut from the wafer. (10).

FIG 1