

SPECIFICATION

Amplifier circuit arrangement

5 The invention relates to an amplifier circuit arrangement.

An amplifier described in the book "Precision Electronics" by Klein and Zaalberg van Zelst, Centrex, Eindhoven, 1967, p. 164-165, comprises first
10 and second amplifier elements whose outputs are connected to a load. The output signal of the first amplifier element is compared with the input signal thereto in a differencing circuit comprising an attenuator, and the resulting signal is applied to the
15 second amplifier element. In this amplifier the two amplifier elements have substantially equal gain factors and the second amplifier element functions as a correction amplifier for the first amplifier element. The output signal of the first amplifier element is
20 attenuated in the attenuator by a factor equal to the reciprocal of the gain factor of each amplifier element, and is then compared with the input signal in a comparator. The output of the comparator constitutes a correction signal which is added to the output
25 signal of the first amplifier element via the second amplifier. Thus the known "adding-what-is-missing" principle is employed, the relative error of the complete amplifier arrangement being equal to the product of the relative errors of the two amplifier ele-
30 ments.

Such an arrangement may give rise to only a very small overall distortion and may be stable.

It has now been recognised that it is possible to employ both of two such amplifier elements to pro-
35 duce correction signals in a stable manner, in spite of the fact that the entire arrangement will contain a number of feedback loops if this is done.

Accordingly, the invention provides an amplifier circuit arrangement comprising first and second
40 power amplifiers whose outputs are connected to a common load, a signal input terminal coupled to inputs of said first and second power amplifiers in such manner that output signals produced by said first and second power amplifiers in response to the
45 application of an input signal to said signal input terminal will drive the load in the same sense, a first signal combining circuit having first and second inputs connected to the input to and the output of said first power amplifier respectively, which first
50 signal combining circuit is constructed in such manner as to produce an output signal in which the contribution thereto derived from the output of said first power amplifier is at least partially cancelled by the
55 corresponding contribution thereto derived from the input to said first power amplifier, a second signal combining circuit having first and second inputs connected to the input to and the output of said second power amplifier respectively, which second
60 signal combining circuit is constructed in such manner as to produce an output signal in which the contribution thereto derived from the output of said second power amplifier is at least partially cancelled by the corresponding contribution thereto derived from the input to said second power amplifier, a
65 coupling from the output of said first signal combin-

ing circuit to the input of said second power amplifier in such manner that any component of the output signal of said first signal combining circuit derived from the output of said first power amplifier will, after passage through said second power amplifier, drive the load in the opposite sense to that in which the corresponding component of the output signal of the first power amplifier drives the load, and a coupling from the output of said second signal combining circuit to the input of said first power amplifier in such manner that any component of the output signal of said second signal combining circuit derived from the output of said second power amplifier will, after passage through said first power
75 amplifier, drive the load in the opposite sense to that in which the corresponding component of the output signal of the second power amplifier drives the load.

In comparison with the known amplifier arrangement, such an arrangement may have the following advantages:

- the overall distortion percentage may be reduced, possibly even to a value which is hardly measurable, provided that each power amplifier can always transfer a signal to its output,
- the power amplifiers may be of a kind which give rise to a relatively high distortion percentage,
- because the total power delivered is divided between two power amplifiers and because the arrangement can be symmetrical the arrangement can be more suitable for construction as an integrated circuit.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings, in which

- Figure 1 shows a first embodiment,
- Figure 2 shows a second embodiment,
- Figure 3 and 4 show possible constructions for the arrangement of Figure 1 in more detail,
- Figure 5 shows a specific construction for a variant of the arrangement of Figure 2, and
- Figure 6 shows a variant of the arrangement of Figure 1.

The amplifier circuit arrangement of Figure 1 comprises two amplifier elements 1 and 2, which are preceded by preamplifiers 3 and 4 respectively.

The amplifier elements 1 and 2 are final power stages, which may each operate in class A or class B, or even in class D in conjunction with a low-pass filter. They operate to produce a voltage output, i.e. they have low output impedances.

A load 7, for example a loudspeaker, is included directly between the respective outputs 5 and 6 of the power amplifiers 1 and 2.

The preamplifiers 3 and 4 take the form of differential amplifiers and each has a non-inverting input (denoted by a + sign) and an inverting input (denoted by a - sign). Preamplifier 3 receives an input signal S at its inverting input; preamplifier 4 receives this signal at its non-inverting input.

The amplifiers 1 and 2 are also connected to auxiliary, in this case differencing, circuits A and B respectively, each of which consists of an attenuator and a signal combining circuit in the form of a comparator. The inverting input of the comparator 9 of the auxiliary circuit A associated with power amp-

lifier 1 is supplied with a part of the output voltage available at the output terminal 5 of the power amplifier 1 via the attenuator of auxiliary circuit A. This attenuator takes the form of a potentiometer 8, and the comparator 9 takes the form of a differential amplifier. The output of the comparator 9 is connected to the inverting input of preamplifier 4 for applying a correction signal thereto.

- The non-inverting input of the comparator 11 of the auxiliary circuit B associated with power amplifier 2 is similarly supplied with a part of the output voltage available at the output terminal 6 of the power amplifier 2 via the attenuator of auxiliary circuit B. This attenuator takes the form of a potentiometer 10, and the comparator 11 takes the form of a differential amplifier. The output of comparator 11 is connected to the non-inverting input of preamplifier 3 for applying a correction signal thereto. The other ends of the potentiometers 8 and 10 are both connected to earth. The input terminal 12 of the power amplifier 1 is connected to the non-inverting input of the comparator 9, and the input terminal 13 of the power amplifier 2 is connected to the inverting input of the second comparator 11.
- The differential amplifiers 3, 4, 9 and 11 are linear operational amplifiers, the voltage gain of each of which may be unity.

The amplifier arrangement of Figure 1 drives the load 7 in push-pull, and operates as follows. The input signal S to be amplified is subtracted from the correction signal from comparator 11 in preamplifier 3, and the result is applied to the input 12 of the power amplifier 1. Power amplifier 1 amplifies its input signal by a factor α , and also results in a distortion or error signal E being added to the amplified signal, where E represents the linear and the non-linear distortion produced by power amplifier 1.

A part of the resulting output signal at point 5 is fed to comparator 9 via attenuator 8 and is compared therein with the input signal at terminal 12. Attenuator 8 gives rise to an attenuation δ , where δ is the voltage on the tapping of potentiometer 8 divided by the voltage applied to said potentiometer, i.e. the attenuation factor thereof.

The resulting correction signal produced by comparator 9 is subtracted in preamplifier 4 from the signal S applied thereto and the result is applied to the input 13 of amplifier 2. The resulting signal at point 13 is amplified in amplifier 2 by a factor β . This amplifier results in a distortion or error signal F being added to the amplified signal.

A part of the resulting output signal is taken from output terminal 6 via attenuator 10, which gives rise to an attenuation γ , where γ is the voltage on the tapping of potentiometer 10 divided by the voltage applied to said potentiometer, i.e. the attenuation factor thereof. The attenuated signal is compared with the input signal at terminal 13 in the comparator 11, and the resulting correction signal is fed to amplifier 1 via preamplifier 3.

The voltage ultimately obtained across the load 7, i.e. between the output terminals 5 and 6 is given by:

$$\frac{2\alpha + 2\beta - \alpha\beta\gamma - \alpha\beta\delta}{\alpha\delta + \beta\gamma - \alpha\beta\gamma\delta} \cdot S - \frac{E\beta(\gamma - \delta) - F\alpha(\delta - \gamma)}{\alpha\delta + \beta\gamma - \alpha\beta\gamma\delta}$$

in which the first term represents the undistorted

signal and the second term the distortion.

It is evident that the last term becomes zero if

$$E\beta(\gamma - \delta) = F\alpha(\delta - \gamma)$$

This requirement is met if

$$\gamma = \delta$$

i.e. if the attenuations given by the attenuators 8 and 9 are equal to each other. If this is so the overall gain will be $2/\gamma$.

It should be pointed out that the above expression for the output voltage is only valid if:

- the distortion percentages to which the differential amplifiers (which may be linear operational amplifiers) give rise are substantially smaller, for example tens of dBs smaller, than that to which each power amplifier 1 and 2 gives rise.
- the resistance of the load is several times smaller than that of each attenuator, i.e. than the total resistance of each of the potentiometers 8 and 10.
- the power amplifiers can always transfer a signal to their outputs.
- the so-called "slew rate", i.e. the pulse response time of the power amplifiers and the differential amplifiers, is smaller than or equal to the maximum "slew rate" of the input signal.
- If the gains of the power amplifiers are the same the attenuation factors δ are smaller than $2/\alpha$. (This condition is necessary to obtain stability.)

It will be evident that either or both of the comparators in Figure 1 may be connected the other way around. For example, the output signal taken from terminal 5 via attenuator 8 may be applied to the non-inverting input of comparator 9 and the input signal taken from terminal 12 may be applied to the inverting input thereof, the correction signal from comparator 9 then being applied to a non-inverting input of preamplifier 4 instead of to the inverting input thereof.

Figure 2 shows an amplifier circuit arrangement which is similar to that of Figure 1 but in which the power amplifiers 1 and 2 operate to produce a current output rather than a voltage output. Thus they have high output impedances. In Figure 2 the output terminals 5 and 6 are connected to a common output terminal 22 via resistors 20 and 21 respectively, and the load 7 is connected between terminal 22 and earth.

The circuit of Figure 2 again comprises comparators 9 and 11 and attenuators included in comparators or differential amplifiers 8 and 10, the connections of these to the power amplifiers 1 and 2 and to the preamplifiers 3 and 4 being similar to those of Figure 1 after taking into account that the power amplifiers 1 and 2 are required to operate in phase with each other in the circuit of Figure 2, which results in changes to the polarities of some of the inputs to the various differential amplifiers.

The resistors 20 and 21 in the amplifier circuit of Figure 2 function as current-to-voltage converters, the voltages appearing there-across being attenuated by the correct amounts in the attenuators in the differential amplifiers 8 and 10 respectively and being applied to the comparators 9 and 11 respectively in the same phases as those in which the corresponding input signals of amplifiers 1 and 2 respectively, which are derived from input terminals

12 and 13 respectively, are applied thereto.

The resistors 20 and 21 have values which are several times smaller than that of the load 7.

Figure 3 shows one possible construction for the 5 arrangement of Figure 1 in more detail.

The gain factors α and β of the power amplifiers 1 and 2 respectively are substantially identical. The attenuators 8 and 10 consist of potentiometers, which are adjusted to give attenuations which are 10 substantially equal to the reciprocals of these gain factors α and β , i.e. $\gamma = \delta = 1/\alpha = 1/\beta$.

Potentiometer 8 consists of a fixed resistor 30 and a variable resistor 31, whilst potentiometer 10 consists of fixed resistors 32 and 33. The resistors 30 and 15 32 have identical values, and the value of resistor 31 is slightly larger than that of resistor 33.

The attenuations γ and δ can be exactly equalized by adjusting the tapped resistor 31.

The input signal S is applied to a linear operational 20 amplifier 34, which functions as an impedance matching stage.

The gain factors of the linear operational amplifiers which constitute the preamplifiers 3 and 4, the comparators 9 and 11 and the amplifier 34 are each 25 unity.

The values of the resistors which are designated R are each 2200 Ω . The value of the resistors 30 and 32 is 7500 Ω , and those of resistors 31 and 33 are 100 Ω and 90 Ω respectively.

30 Each power amplifier 1 and 2 can deliver 100 Watts into a 2 ohm load at an input voltage of 200 mV, i.e. it has a gain factor of approximately 70. Each of these power amplifiers may be of the class B type SQ 4 (Philips).

35 The linear operational amplifiers may be of the type TDA 1034 (Philips), it being assumed that they are required to operate in the audio frequency range, i.e. up to 20 kHz, only.

The load 7 may be constituted by a loudspeaker 40 having an impedance of 4 ohms. As the class B amplifiers 1 and 2 are effectively included in a bridge circuit a power of 200 Watts is available.

Measurements of harmonic and intermodulation distortion produced by such a push-pull output amplifier at full drive, using a spectrum analyzer type HP 45 3580 A, gave the following results, two signals of the same amplitude but different frequency (14 kHz and 15 kHz respectively) being applied to the amplifier during the measurement of intermodulation distortion: 50

harmonic distortion

f	^d tot. non-comp.	^d tot. comp.
1 kHz	0.33%	"0"
10 kHz	0.43%	0.03%

intermodulation distortion

^d tot. non comp.	^d tot. comp.
0.5%	0.02%

("^dtot. comp." is the relevant distortion obtained with the circuit of Figure 3 and "^dtot. non-comp." is the corresponding relevant distortion with the feedback loops including the comparators 9 and 11 open).

60 It will be seen that these distortions are substantially reduced by closure of the feedback loops, i.e. by the provision of the auxiliary circuits comprising 65 the attenuators and comparators.

Figure 4 shows another possible construction for the amplifier arrangement of Figure 1 in more detail.

In the arrangement of Figure 4 the amplifiers 1 and 2 each consist of a class B output stage provided 70 with npn and pnp Darlington power transistors of the silicon type. The voltage gain factor of each output stage is 0.9. The preamplifiers 3 and 4 and the comparators 9 and 11 each comprise an integrated linear operational amplifier of the TDA 1034 type.

75 The preamplifiers of Figure 4 are voltage amplifiers having gain factors of 19.2, and serve as driver circuits for the corresponding power amplifiers. The correction signals produced by the comparators 9 and 11 are each attenuated to 0.05 of their value by 80 potentiometers formed by resistors 40 and 41 and by resistors 42 and 43 respectively.

The quiescent current through the diodes in each power amplifier (approximately 10 mA) is arranged to be sufficient to ensure that current is always flowing in at least one output transistor of each power amplifier; the quiescent current I_q through the output transistors of each power amplifier is approximately 3.3 mA, which means that both output transistors of each power amplifier will carry current even when 90 the input signal passes through zero, i.e. the gain of the output stages does not then drop to zero.

Distortion measurements on an amplifier arrangement constructed as described with reference to Figure 4 gave the following results:

95 harmonic distortion in %

f kHz	^d tot. non-comp. $I_q = 3.3 \text{ mA}$	^d tot. comp. $I_q = 0$	^d tot. comp. $I_q = 3.3 \text{ mA}$
V_u	0.3 15.	0.3 15.	0.3 15
1	24 1.6	12 0.25	0.5 '0'
10	25 1.8	6 0.15	1.0 0.05

In these results ^dtot. non-comp. and ^dtot. comp. have the same meanings as given previously. Two distortion figures are given for each condition, these being obtained when the effective voltage V_u across the 100 (6 Ω) load 7 is 0.3 volts and 15 volts respectively. Figures are also given for ^dtot. comp. obtained if the quiescent current is zero, for comparison. In this case, when $V_u = 0.3 \text{ V}$ and the Darlington output transistors are hence substantially turned off, the 105 distortion figures are very high, although the effect of the compensation is noticeable even in this case. The intermodulation distortion figures obtained for the circuit of Figure 4 when $I_q = 3.3 \text{ mA}$ were:

intermodulation distortion in %

	$V_u = 7.5 V_{r.m.s.}$	$V_u = 1 V_{r.m.s.}$
$f_1 = 14 \text{ kHz}$ $f_2 = 15 \text{ kHz}$	0.28	0.18
$f_1 = 60 \text{ kHz}$ $f_2 = 8 \text{ kHz}$	'0'	0.45

The resistors included in the amplifier of Figure 4 are specified therein for the most part in fractions of R, where $R = 2200\Omega$. The value of the attenuator resistor 41 was 135Ω .

5 Figure 5 shows a specific construction for a variant of the amplifier of Figure 2, but in which the power amplifiers comprise the same Darlington transistors as those in the amplifier of Figure 4.

The current-to-voltage conversion resistors 20 and 21 each have a value of 0.1Ω . The values of most of the resistors in the amplifier are specified in factors of R, where $R = 2200\Omega$. The gain of each of the comparators 9 and 11 is 10.

The overall attenuation from the output of each power amplifier 1 and 2 to the input of the corresponding signal combining circuit is determined by the value of the corresponding resistor 20 or 21 and by the gain of the associated comparator 9 or 11.

Figure 6 shows a variant of the amplifier arrangement of Figure 1, in which the power amplifiers 1 and 2 are now each of the inverting type. (In all the other embodiments described so far the power amplifiers 1 and 2 are non-inverting.) In the arrangement of Figure 6 the incoming signal at the input 12 of the power amplifier 1 and the signal at the output 5 thereof are applied to point 50 via equal-value resistors 20R. The sum thereof (the difference signal), attenuated by 20:1, is applied from point 50 to the inverting input of preamplifier 4. These resistors 20R thus constitute a signal combining circuit.

The other difference signal is obtained in a similar way at point 51 and is applied to the inverting input of preamplifier 3 with the same attenuation.

In an experimental version of this amplifier the same operational amplifiers and power amplifiers were used as in the amplifier arrangement of Figure 4.

CLAIMS

1. An amplifier circuit arrangement comprising first and second power amplifiers whose outputs are connected to a common load, a signal input terminal coupled to inputs of said first and second power amplifiers in such manner that output signals produced by said first and second power amplifiers in response to the application of an input signal to said signal input terminal will drive the load in the same sense, a first signal combining circuit having first and second inputs connected to the input to and the output of said first power amplifier respectively, which first signal combining circuit is constructed in such manner as to produce an output signal in which the contribution thereto derived from the output of said first power amplifier is at least partially cancelled by the corresponding contribution thereto derived from the input to said first power amplifier, a second signal combining circuit having first and second inputs connected to the input to and the output of said second power amplifier respectively, which second signal combining circuit is constructed in such manner as to produce an output signal in which the contribution thereto derived from the output of said second power amplifier is at least partially cancelled by the corresponding contribution thereto derived from the input to said second power amplifier, a coupling from the output of said first

signal combining circuit to the input of said second power amplifier in such manner that any component of the output signal of said first signal combining circuit derived from the output of said first power amplifier will, after passage through said second power amplifier, drive the load in the opposite sense to that in which the corresponding component of the output signal of the first power amplifier drives the load, and a coupling from the output of said second signal combining circuit to the input of said first power amplifier in such manner that any component of the output signal of said second signal combining circuit derived from the output of said second power amplifier will, after passage through said first power amplifier, drive the load in the opposite sense to that in which the corresponding component of the output signal of the second power amplifier drives the load.

2. An arrangement as claimed in Claim 1, wherein the signal input terminal is coupled to the inputs of the first and second power amplifiers via first and second preamplifiers respectively, wherein the first inputs of the first and second signal combining circuits are coupled to the outputs of the first and second preamplifiers respectively, and wherein the outputs of the first and second signal combining circuits are coupled to inputs of the second and first preamplifiers respectively.

3. An arrangement as claimed in Claim 2, wherein the signal input terminal is coupled to inverting and non-inverting inputs of said first and second preamplifiers respectively, and wherein said power amplifiers are connected to the load in such manner as to drive it in push-pull in response to the application of an input signal to said input terminal.

4. An arrangement as claimed in Claim 2, wherein the signal input terminal is coupled either to inverting inputs of said first and second preamplifiers or to non-inverting inputs thereof, wherein the outputs of the first and second power amplifiers are connected to the same terminal of the load via first and second resistors respectively so that said power amplifiers will drive the load in parallel in response to the application of an input signal to said input terminal, wherein the second input of the first signal combining circuit is coupled to the output of a first comparator the respective inputs of which are coupled to opposite ends of said first resistor, and wherein the second input of the second signal combining circuit is coupled to the output of a second comparator the respective inputs of which are coupled to opposite ends of said second resistor.

5. An arrangement as claimed in any preceding Claim, wherein each signal combining circuit comprises a pair of resistors, one resistor of each pair coupling the first input of the corresponding signal combining circuit to a corresponding common point and the other resistor of each pair coupling the second input of the corresponding signal combining circuit to the corresponding common point, each said common point constituting the output of the corresponding signal combining circuit.

6. An arrangement as claimed in Claim 5 when appended to Claim 3, wherein each power amplifier is of the inverting type and has a gain of substantially unity, wherein the two resistors of each said



The resistors included in the amplifier of Figure 4 are specified therein for the most part in fractions of R, where $R = 2200\Omega$. The value of the attenuator resistor 41 was 135Ω .

5 Figure 5 shows a specific construction for a variant of the amplifier of Figure 2, but in which the power amplifiers comprise the same Darlington transistors as those in the amplifier of Figure 4.

The current-to-voltage conversion resistors 20 and 10 21 each have a value of 0.1Ω . The values of most of the resistors in the amplifier are specified in factors of R, where $R = 2200\Omega$. The gain of each of the comparators 9 and 11 is 10.

The overall attenuation from the output of each 15 power amplifier 1 and 2 to the input of the corresponding signal combining circuit is determined by the value of the corresponding resistor 20 or 21 and by the gain of the associated comparator 9 or 11.

Figure 6 shows a variant of the amplifier arrangement 20 of Figure 1, in which the power amplifiers 1 and 2 are now each of the inverting type. (In all the other embodiments described so far the power amplifiers 1 and 2 are non-inverting.) In the arrangement of Figure 6 the incoming signal at the input 12 of the 25 power amplifier 1 and the signal at the output 5 thereof are applied to point 50 via equal-value resistors $20R$. The sum thereof (the difference signal), attenuated by 20:1, is applied from point 50 to the inverting input of preamplifier 4. These resistors $20R$ 30 thus constitute a signal combining circuit.

The other difference signal is obtained in a similar way at point 51 and is applied to the inverting input of preamplifier 3 with the same attenuation.

In an experimental version of this amplifier the 35 same operational amplifiers and power amplifiers were used as in the amplifier arrangement of Figure 4.

CLAIMS

1. An amplifier circuit arrangement comprising 40 first and second power amplifiers whose outputs are connected to a common load, a signal input terminal coupled to inputs of said first and second power amplifiers in such manner that output signals produced by said first and second power amplifiers in 45 response to the application of an input signal to said signal input terminal will drive the load in the same sense, a first signal combining circuit having first and second inputs connected to the input to and the output of said first power amplifier respectively, 50 which first signal combining circuit is constructed in such manner as to produce an output signal in which the contribution thereto derived from the output of said first power amplifier is at least partially cancelled by the corresponding contribution thereto 55 derived from the input to said first power amplifier, a second signal combining circuit having first and second inputs connected to the input to and the output of said second power amplifier respectively, which second signal combining circuit is constructed 60 in such manner as to produce an output signal in which the contribution thereto derived from the output of said second power amplifier is at least partially cancelled by the corresponding contribution thereto derived from the input to said second power 65 amplifier, a coupling from the output of said first

signal combining circuit to the input of said second power amplifier in such manner that any component of the output signal of said first signal combining circuit derived from the output of said first power amplifier will, after passage through said second power amplifier, drive the load in the opposite sense to that in which the corresponding component of the output signal of the first power amplifier drives the load, and a coupling from the output of said second signal combining circuit to the input of said first power amplifier in such manner that any component of the output signal of said second signal combining circuit derived from the output of said second power amplifier will, after passage through said first power amplifier, drive the load in the opposite sense to that in which the corresponding component of the output signal of the second power amplifier drives the load.

2. An arrangement as claimed in Claim 1, wherein the signal input terminal is coupled to the 85 inputs of the first and second power amplifiers via first and second preamplifiers respectively, wherein the first inputs of the first and second signal combining circuits are coupled to the outputs of the first and second preamplifiers respectively, and wherein the 90 outputs of the first and second signal combining circuits are coupled to inputs of the second and first preamplifiers respectively.

3. An arrangement as claimed in Claim 2, wherein the signal input terminal is coupled to 95 inverting and non-inverting inputs of said first and second preamplifiers respectively, and wherein said power amplifiers are connected to the load in such manner as to drive it in push-pull in response to the application of an input signal to said input terminal.

4. An arrangement as claimed in Claim 2, wherein the signal input terminal is coupled either to 100 inverting inputs of said first and second preamplifiers or to non-inverting inputs thereof, wherein the outputs of the first and second power amplifiers are 105 connected to the same terminal of the load via first and second resistors respectively so that said power amplifiers will drive the load in parallel in response to the application of an input signal to said input terminal, wherein the second input of the first signal 110 combining circuit is coupled to the output of a first comparator the respective inputs of which are coupled to opposite ends of said first resistor, and wherein the second input of the second signal combining circuit is coupled to the output of a second 115 comparator the respective inputs of which are coupled to opposite ends of said second resistor.

5. An arrangement as claimed in any preceding Claim, wherein each signal combining circuit comprises a pair of resistors, one resistor of each pair 120 coupling the first input of the corresponding signal combining circuit to a corresponding common point and the other resistor of each pair coupling the second input of the corresponding signal combining circuit to the corresponding common point, each 125 said common point constituting the output of the corresponding signal combining circuit.

6. An arrangement as claimed in Claim 5 when appended to Claim 3, wherein each power amplifier is of the inverting type and has a gain of substantially unity, wherein the two resistors of each said 130



pair have substantially equal values, wherein the said common point of the resistors of the first signal combining circuit is coupled to an inverting input of the second preamplifier via an attenuator, and
 5 wherein the said common point of the resistors of the second signal combining circuit is coupled to an inverting input of the first preamplifier via an attenuator.

7. An arrangement as claimed in any of Claims 1 to 4, wherein each signal combining circuit comprises a comparator.

8. An arrangement as claimed in Claim 7, wherein each comparator is constituted by a differential amplifier.

15 9. An arrangement as claimed in Claim 8, wherein each differential amplifier is constituted by a linear operational amplifier.

10. An arrangement as claimed in any of Claims 7 to 9 when appended to Claim 4, wherein the first
 20 input of the first signal combining circuit is connected to the input of the comparator of the first signal combining circuit which has the same polarity as the input of the comparator of the second signal combining circuit to which the first input of the sec-
 25 ond signal combining circuit is connected, and wherein the outputs of the first and second signal combining circuits are connected to inputs of the second and first preamplifiers respectively which have the same polarity as one another.

30 11. An arrangement as claimed in any of Claims 7 to 9 when appended to Claim 3, wherein the second input of the first signal combining circuit is connected to the input of the comparator of the first signal combining circuit of one polarity, wherein the
 35 second input of the second signal combining circuit is connected to the input of the comparator of the second signal combining circuit of the opposite polarity, wherein the output of the first signal combining circuit is connected to an input of said second
 40 preamplifier which has said one polarity, and wherein the output of the second signal combining circuit is connected to an input of said first preamplifier which has said opposite polarity.

12. An arrangement as claimed in any of Claims
 45 1 to 4 or 7 to 11, including first and second attenuators in the signal paths from the output of the first power amplifier to the second input of the first signal combining circuit and from the output of the second power amplifier to the second input of the
 50 second signal combining circuit respectively.

13. An arrangement as claimed in Claim 12, wherein each attenuator consists of a potentiometer.

14. An arrangement as claimed in Claim 12 or
 55 Claim 13, wherein the attenuation factors of said attenuators are substantially equal.

15. An arrangement as claimed in any preceding claim, wherein the gain factors α of the power amplifiers are substantially equal.

16. An arrangement as claimed in Claim 15 when
 60 appended to Claim 14, wherein each attenuation factor is less than $2/\alpha$.

17. An amplifier circuit arrangement substantially as described herein with reference to any of Figures 1 to 6 of the drawings.