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DEFINITION OF ANTI-FUSE CELL FOR PROGRAMMABLE GATE ARRAY APPLICATION

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method of defining an anti-fuse cell window in the fabrication of integrated circuits.

(2) Description of the Prior Art

In the fabrication of anti-fuse cells for programmable gate arrays, the current process uses a thin silicon nitride film as a mask in defining the anti-fuse cell window. Because of poor center to edge etching uniformity, silicon nitride residues are often left. Fig. 1 illustrates a partially completed integrated circuit device. On a semiconductor substrate, a layer of silicon nitride 15 has been deposited over a layer of silicon oxide 14. In the cell area A, a window 19 is etched, using the silicon nitride layer 15 as a mask. The window is then filled with an insulating layer 26 and polysilicon layer 28. However, in the active area B, because of the poor etching uniformity, silicon nitride residues 17 are left.

U.S. Patent 4,796,074 to Roesner and U.S. Patent 5,322,812 to Dixit et al show anti-fuse methods and resulting structures.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of fabricating an anti-fuse cell for programmable gate array.

A further object of the invention is to provide a method of fabricating an anti-fuse cell for programmable gate array without nitride residues.

Yet another object is to provide a method of fabricating an anti-fuse cell using an undoped polysilicon film as a mask in defining the anti-fuse window.

In accordance with the objects of this invention a method for fabricating an anti-fuse cell using an undoped polysilicon film as a mask in defining the anti-fuse window is achieved. A layer of silicon oxide is provided over the surface of a semiconductor substrate. A first undoped polysilicon layer is deposited overlying the silicon oxide layer. The first undoped polysilicon layer is

covered with a photoresist layer patterned to form a mask. The first undoped polysilicon layer and a portion of the silicon oxide layer are etched away where they are not covered by the mask to form a cell opening. The mask and the remaining silicon oxide within the cell opening are removed. An insulating layer is deposited over the surface of the first undoped polysilicon layer and within the cell opening. A second polysilicon layer is deposited overlying the insulating layer and doped. The second polysilicon layer is patterned to form an anti-fuse cell. Gate electrodes and source and drain regions are formed completing the fabrication of the integrated circuit device.

Also in accordance with the objects of this invention, an anti-fuse cell device is described. A first undoped polysilicon layer overlies a silicon oxide layer on the surface of a semiconductor substrate. An insulating layer overlies the first undoped polysilicon layer and contacts the semiconductor substrate at the bottom of a cell opening through the first undoped polysilicon and the silicon oxide layers. A patterned second polysilicon layer overlies the insulating layer within the cell opening to form the anti-fuse cell.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Fig. 1 schematically illustrates in cross-sectional representation an anti-fuse cell of the prior art.

Figs. 2 through 6 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

Fig. 7 schematically illustrate in cross-sectional representation a completed anti-fuse cell of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now more particularly to Fig. 2, there is shown an illustration of a portion of a partially completed integrated circuit. The semiconductor substrate 10 is preferably composed of silicon having a Si(100) crystallographic orientation. Field Oxide regions 12 are formed as are conventional in the art. The surface of the silicon substrate 10 is thermally oxidized to form the

desired pad oxide 14 thickness. The preferred thickness is between about 500 to 1500 Angstroms.

N+ active area 20 is formed by ion implantation and diffusion drive-in. For example, phosphorus ions are implanted with a dosage of between about 2 E 13 to 1 E 14 atoms/cm^2 at an energy of between about 40 to 60 KeV. Alternatively, arsenic ions are implanted with a dosage of between about 1 E 15 to 5 E 15 atoms/cm^2 at an energy of between about 40 to 60 KeV.

In the conventional process of the prior art, a thin silicon nitride film is used as a mask for the cell window definition. In the process of the present invention, a layer of undoped polysilicon or amorphous silicon 16 is deposited by low pressure chemical vapor deposition (LPCVD) to a thickness of between about 400 to 1500 Angstroms.

A layer of photoresist is coated over the polysilicon layer 16 and patterned as is conventional in the art to form a photoresist mask 18, as illustrated in Fig. 2.

Referring now to Fig. 3, the polysilicon or amorphous silicon layer 16 is etched selectively with respect to the pad oxide until between about 200 to 600 Angstroms of

the pad oxide 14 remains within the cell openings. A one step dry etch is all that is necessary to etch both the polysilicon and the pad oxide. Using a nitride film instead of the undoped polysilicon or amorphous silicon requires a two step wet and dry etch. The one step etch saves cycle time. Also, the elimination of the wet etch step eliminates an undercutting of the pad oxide during the cell opening wet etch.

LPCVD silicon nitride film deposition is much dirtier, in terms of particle count, than LPCVD polysilicon or amorphous silicon deposition. Therefore, etching the undoped polysilicon or amorphous film is easier and cleaner than etching a nitride film. Also, polysilicon and amorphous silicon have better sidewall control and there better process control for oxide remaining in the present invention.

The photoresist mask 18 is stripped and the remaining pad oxide within the openings is wet etched away using a buffered oxide etch (BOE), as shown in Fig. 4. The BOE etch is performed with an etch rate of between about 300 to 360 Angstroms/minute for between about 4 to 6 minutes. The slight undercutting of the silicon oxide layer results from the BOE etch.

Referring now to Fig. 5, an insulating layer 26 is deposited overlying the undoped polysilicon layer 16 and within the cell openings. This insulating layer may be ONO (silicon oxide, silicon nitride, silicon oxide) or NO (silicon nitride, silicon oxide) with a total thickness of between about 40 to 120 Angstroms. Next a layer 28 of polysilicon is deposited over the insulating layer 26 to a thickness of between about 2500 to 4000 Angstroms. The polysilicon layer 28 is doped by $POCl_3$ and arsenic or phosphorus to a dopant concentration of between about 1 E 19 to 1 E 21 atoms/cm^3.

A layer of photoresist is coated over the doped polysilicon layer 28 and patterned to form a mask 30. Referring now to Fig. 6, the polysilicon layer 28, insulating layer 26, undoped polysilicon or amorphous silicon layer 16, and a portion of the silicon oxide 14 and/or field oxide region 12 are etched away where they are not covered by the mask 30 and the photoresist is stripped.

This completes the formation of the anti-fuse cell. The integrated circuit device is completed as is conventional in the art. For example, as illustrated in Fig. 7, a spacer oxide 30 is deposited conformally over the polysilicon 28. In the active portion of the integrated

circuit device B, gate electrode 32 and source and drain regions 34 are formed. An insulting layer 36 is blanket deposited over all. Openings are etched through the insulting layer 36 where electrical contacts are to be made, for example to source and drain regions 34 and to the anti-fuse cell 28. A conducting layer 38 is deposited and patterned to complete the electrical connections, followed by the deposition of passivation layer 40.

The process of the invention provides an effective method of fabricating an anti-fuse cell without nitride residues. The process of the invention is a simplified process. Etching a stack containing undoped polysilicon or amorphous silicon rather than silicon nitride is easier, cleaner, and more controllable.

In accordance with another aspect of the present invention, an anti-fuse cell for a programmable gate array is described with reference to Fig. 7. In the cell area A, a first layer 16 of undoped polysilicon or amorphous silicon overlies a silicon oxide layer 14 on the surface of a semiconductor substrate 10. An insulating layer 26 overlies the first undoped polysilicon layer and contacts the semiconductor substrate at the bottom of the cell opening through the first undoped polysilicon or amorphous silicon

and the silicon oxide layers. A patterned second polysilicon layer 28 overlies the insulating layer within the cell opening to form the anti-fuse cell. In the active area, gate electrode 32 and source and drain regions 34 are covered by insulating layer 36 which also covers the anti-fuse cell 28. Patterned conducting layer 38 electrically connects the anti-fuse cell and the source and drain regions.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of fabricating an integrated circuit device comprising:

providing a layer of silicon oxide over the surface of a semiconductor substrate wherein said semiconductor substrate has a cell area and an active area;

in said cell area:

depositing a first undoped silicon layer overlying said silicon oxide layer;

covering said first undoped silicon layer with a photoresist layer and patterning said photoresist layer to form a mask;

etching away said first undoped silicon layer and a portion of said silicon oxide where it is not covered by said mask to form a cell opening;

removing said mask and remaining silicon oxide within said cell opening;

depositing an insulating layer over the surface of said first undoped silicon layer and within said cell opening;

depositing a second polysilicon layer overlying said insulating layer and doping said second polysilicon layer; and

patterning said second polysilicon layer to form an anti-fuse cell; and

in said active area forming gate electrodes and

source and drain regions completing the fabrication of said integrated circuit device.

2. The method according to Claim 1 wherein said silicon oxide layer has a thickness of between about 500 to 1500 Angstroms.

3. The method according to Claim 1 wherein said first undoped silicon layer is deposited by low pressure chemical vapor deposition to a thickness of between about 400 to 1500 Angstroms.

4. The method according to Claim 1 wherein said first undoped silicon layer comprises polysilicon.

5. The method according to Claim 1 wherein said first undoped silicon layer comprises amorphous silicon.

6. The method according to Claim 1 wherein said etching away of said first undoped silicon layer and a portion of said silicon oxide layer comprises a dry etch using one or more of the group containing C_2F_6, SF_6, Cl_2, and HBr.

7. The method according to Claim 1 wherein said remaining portion of said silicon oxide layer has a thickness of between about 200 to 600 Angstroms.

8. The method according to Claim 1 wherein said remaining silicon oxide within said cell openings is removed with a buffered oxide etch (BOE) with an etch rate of between about 300 to 360 Angstroms/minute for between about 4 to 6 minutes.

9. The method according to Claim 1 wherein said insulating layer comprises silicon oxide, silicon nitride, and silicon oxide (ONO) with a total thickness of between about 40 to 120 Angstroms.

10. The method according to Claim 1 wherein said insulating layer comprises silicon oxide and silicon nitride (NO) with a total thickness of between about 40 to 120 Angstroms.

11. The method according to Claim 1 wherein said second polysilicon layer is deposited by LPCVD to a thickness of between about 2500 to 4000 Angstroms.

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12. The method according to Claim 1 wherein said second polysilicon layer is doped with a $POCl_3$ plus arsenic implant to a dopant concentration of between about 1 E 19 to 1 E 21 atoms/cm^3.

13. The method according to Claim 1 wherein said second polysilicon layer is doped with a $POCl_3$ plus phosphorus implant to a dopant concentration of between about 1 E 19 to 1 E 21 atoms/cm^3.

14. A method of forming an anti-fuse cell in the fabrication of an integrated circuit device comprising:

providing a layer of silicon oxide over the surface of a semiconductor substrate;

depositing a first undoped silicon layer overlying said silicon oxide layer;

covering said first undoped silicon layer with a photoresist layer and patterning said photoresist layer to form a mask;

etching away said first undoped silicon layer and a portion of said silicon oxide where it is not covered by said mask to form cell openings;

removing said mask and remaining silicon oxide within said cell openings;

depositing an insulating layer over the surface of

said first undoped silicon layer and within said cell openings;

depositing a second polysilicon layer overlying said insulating layer and doping said second polysilicon layer; and

patterning said second polysilicon layer to complete the formation of an anti-fuse cell in the fabrication of said integrated circuit device.

15. The method according to Claim 14 wherein said silicon oxide layer has a thickness of between about 500 to 1500 Angstroms.

16. The method according to Claim 14 wherein said first undoped silicon layer is deposited by low pressure chemical vapor deposition to a thickness of between about 400 to 1500 Angstroms.

17. The method according to Claim 14 wherein said first undoped silicon layer comprises polysilicon.

18. The method according to Claim 14 wherein said first undoped silicon layer comprises amorphous silicon.

19. The method according to Claim 14 wherein said etching away of said first undoped silicon layer and a portion of said silicon oxide layer comprises a dry etch using one or more of the group containing C_2F_6, SF_6, Cl_2, and HBr.

20. The method according to Claim 14 wherein said remaining portion of said silicon oxide layer has a thickness of between about 200 to 600 Angstroms.

21. The method according to Claim 14 wherein said remaining silicon oxide within said cell openings is removed with a buffered oxide etch (BOE) with an etch rate of between about 300 to 360 Angstroms/minute for between about 4 to 6 minutes.

22. The method according to Claim 14 wherein said insulating layer comprises silicon oxide, silicon nitride, and silicon oxide (ONO) with a total thickness of between about 40 to 120 Angstroms.

23. The method according to Claim 14 wherein said insulating layer comprises silicon oxide and silicon nitride (NO) with a total thickness of between about 40 to 120 Angstroms.

24. The method according to Claim 14 wherein said second polysilicon layer is deposited by LPCVD to a thickness of between about 2500 to 4000 Angstroms.

25. The method according to Claim 14 wherein said second polysilicon layer is doped with a $POCl_3$ plus arsenic implant to a dopant concentration of between about 1 E 19 to 1 E 21 atoms/cm^3.

26. The method according to Claim 14 wherein said second polysilicon layer is doped with a $POCl_3$ plus phosphorus implant to a dopant concentration of between about 1 E 19 to 1 E 21 atoms/cm^3.

27. An anti-fuse cell in an integrated circuit device comprising:

a first undoped silicon layer overlying a silicon oxide layer on the surface of a semiconductor substrate;

an insulating layer overlying said first undoped silicon layer and contacting said semiconductor substrate at the bottom of a cell opening through said first undoped silicon and said silicon oxide layers; and

a patterned second polysilicon layer overlying said insulating layer within said cell opening which forms said anti-fuse cell in said integrated circuit device.

28. A device according to Claim 27 wherein said silicon oxide layer has a thickness of between about 500 to 1500 Angstroms.

29. A device according to Claim 27 wherein said first undoped silicon layer has a thickness of between about 400 to 1500 Angstroms.

30. A device according to Claim 27 wherein said first undoped silicon layer comprises polysilicon.

31. A device according to Claim 27 wherein said first undoped silicon layer comprises amorphous silicon.

32. A device according to Claim 27 wherein said insulating layer comprises silicon oxide, silicon nitride, and silicon oxide (ONO) with a total thickness of between about 40 to 120 Angstroms.

33. A device according to Claim 27 wherein said insulating layer comprises silicon oxide and silicon nitride (NO) with a total thickness of between about 40 to 120 Angstroms.

34. A device according to Claim 27 wherein said second polysilicon layer has a thickness of between about 2500 to 4000 Angstroms and a dopant concentration of between about 1 E 19 to 1 E 21 atoms/cm^3.