STACKED MICROELECTRONIC DEVICES AND METHODS FOR MANUFACTURING STACKED MICROELECTRONIC DEVICES

TECHNICAL FIELD

[0001] The present disclosure is related to stacked microelectronic devices and methods for manufacturing stacked microelectronic devices.

BACKGROUND

[0002] Processors, memory devices, imagers and other types of microelectronic devices are often manufactured on semiconductor workpieces or other types of workpieces. In a typical application, several individual dies (e.g., devices) are fabricated on a single workpiece using sophisticated and expensive equipment and processes. Individual dies generally include an integrated circuit and a plurality of bond pads coupled to the integrated circuit. The bond pads provide external electrical contacts on the die through which supply voltage, signals, and other electrical parameters are transmitted to and from the integrated circuit. The bond pads are usually very small, and they are arranged in an array having a fine pitch between bond pads. The dies can also be quite delicate. As a result, after fabrication, the dies are packaged to protect the dies and to connect the bond pads to another array of larger terminals that is easier to connect to a printed circuit board.

[0003] Conventional processes for packaging dies include electrically coupling the bond pads on the dies to an array of pins, ball pads, or other types of electrical terminals, and then encapsulating the dies to protect them from environmental factors (e.g., moisture, particulates, static electricity, and physical impact). In one application, the bond pads are electrically connected to contacts on an interposer substrate that has an array of ball pads. For example, Figure 1A schematically illustrates a conventional packaged microelectronic device 6, including a microelectronic die 10, an interposer substrate 60 attached to the die 10, a plurality of wire bonds 90

electrically coupling the die 10 to the interposer substrate 60, and a casing 70 protecting the die 10 from environmental factors.

[0004] Figure 1B schematically illustrates another conventional packaged microelectronic device 6a having two stacked microelectronic dies 10a-b. The microelectronic device 6a includes a substrate 60a, a first microelectronic die 10a attached to the substrate 60a, a spacer 30 attached to the first die 10a with a first adhesive 22a, and a second microelectronic die 10b attached to the spacer 30 with a second adhesive 22b. The spacer 30 is a precut section of a semiconductor wafer. Other types of conventional stacked microelectronic device packages include an epoxy spacer, rather than a section of a semiconductor wafer, to space apart the first and second dies 10a-b. The epoxy spacer is formed by dispensing a discrete volume of epoxy onto the first die 10a and then pressing the second die 10b downward onto the epoxy. Epoxy spacers, however, are not rigid until cured, and thus the second dies may not be uniformly spaced apart from the corresponding first dies.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1A schematically illustrates a conventional packaged microelectronic device in accordance with the prior art.

[0006] Figure 1B schematically illustrates another conventional packaged microelectronic device in accordance with the prior art.

[0007] Figure 2A is an isometric view of a stacked microelectronic die assembly having two-tiered metal spacers at the corners of the dies in accordance with one embodiment of the disclosure.

[0008] Figure 2B is a cross-sectional view of the assembly of Figure 2A showing metal spacers positioned on spacer bond sites.

[0009] Figure 2C is another cross-sectional view of the assembly of Figure 2A showing interconnects passing between the stacked dies.

[0010] Figure 2D is another cross-sectional view of the assembly of Figure 2A showing electrical isolation of the metal spacers.

[0011] Figures 3A-C are cross-sectional views of metal spacers in accordance with several embodiments of the disclosure.

[0012] Figure 4 is an isometric view of a microelectronic die having metal spacers placed on an interior portion of the die in accordance with another embodiment of the disclosure.

[0013] Figure 5A is an isometric view of a stacked die assembly having stitched metal spacers in accordance with another embodiment of the disclosure.

[0014] Figure 5B is a cross-sectional view of the assembly of Figure 5A showing the stitched metal spacers passing between the stacked dies.

[0015] Figure 5C is a cross-sectional view of the assembly of Figure 5B showing electrical isolation of the stitched metal spacers.

[0016] Figures 6A-F illustrate stages of a method of forming a metal spacer in accordance with several embodiments of the disclosure.

[0017] Figure 7 is an isometric view of a microelectronic die having wire bond metal bumps and stitched metal spacers in accordance with another embodiment of the disclosure.

[0018] Figure 8 is a cross-sectional view of a packaged microelectronic device having differently sized microelectronic dies and three-tiered metal spacers in accordance with another embodiment of the disclosure.

[0019] Figure 9 is a cross-sectional view of a packaged microelectronic device having three stacked microelectronic dies and corresponding two-tiered and three-tiered metal spacers in accordance with another embodiment of the disclosure.

[0020] Figure 10 is a cross-sectional view of the packaged microelectronic device of Figure 8 further including interior metal spacers.

[0021] Figure 11 is a schematic illustration of a system in which the microelectronic devices may be incorporated.

DETAILED DESCRIPTION

[0022] Specific details of several embodiments of the disclosure are described below with reference to semiconductor devices and methods for fabricating semiconductor devices. The semiconductor components are manufactured on semiconductor wafers that can include substrates

on which and/or in which microelectronic devices, micromechanical devices, data storage elements, optics, read/write components, and other features are fabricated. For example, SRAM, DRAM (e.g., DDR/SDRAM), flash memory (e.g., NAND flash memory), processors, imagers, and other types of devices can be constructed on semiconductor wafers. Although many of the embodiments are described below with respect to semiconductor devices that have integrated circuits, other types of devices manufactured on other types of substrates may be within the scope of the invention. Moreover, several other embodiments of the invention can have different configurations, components, or procedures than those described in this section. A person of ordinary skill in the art, therefore, will accordingly understand that the invention may have other embodiments with additional elements, or the invention may have other embodiments without several of the features shown and described below with reference to Figures 2A-11.

[0023] Figure 2A is an isometric view of one embodiment of a stacked die assembly 100 that includes a first microelectronic die 102a having a front side (e.g., an active side) separated from a back side of a second microelectronic die 102b by metal spacers 104. The metal spacers 104 can be multi-tiered metal spacers comprising at least two spacer elements, and in the specific embodiment shown in Figure 2A the spacers 104 are two-tiered metal spacers with first spacer elements and second spacer elements stacked on the first spacer elements. The metal spacers 104 are located at electrically isolated spacer sites 106 adjacent to the corners of the first die 102a. The first and second dies 102a-b can further include bond pads 108a and 108b, respectively, for electrically coupling the first and second dies 102a-b to bond pads 114 of an interposer substrate 110 (e.g., a printed circuit board). Accordingly, a plurality of first wire bonds 112a and a plurality of second wire bonds 112b, respectively, couple the first and second dies 102a-b to the bond pads 114. In addition to these electrical couplings, an adhesive layer 116 physically couples the first die 102a to the substrate 110 and a filler layer 118 adheres the second die 102b to the first die 102a. The filler layer 118 can also physically and electrically isolate individual first wire bonds 112a from each other. The filler layer 118 may comprise, for example, an epoxy, epoxy acrylic, polymide, or other suitable material, and it may be used to further attach the first die 102a to the second die 102b.

[0024] Figures 2B-D are cross-sectional views of the assembly 100 shown in Figure 2A. Figure 2B shows the metal spacers 104 attached to both a front-side surface 120 of the first die 102a

and a back-side surface 122 of the second die 102b. In this embodiment, the metal spacers 104 have two separate elements in a stacked, two-tiered configuration. The filler layer 118 encapsulates the metal spacers 104 and fills an interior portion 124 of the assembly 100. Figure 2C shows partial schematic diagrams associated with the first die 102a, the second die 102b, and the substrate 110. The first and second dies 102a-b, respectively, include integrated circuits (ICs) 126a and 126b and interconnect networks 127a and 127b. In general, the interconnect networks 127a-b each include stacked layers of metal lines (e.g., copper, aluminum, titanium, cobalt, etc.) and vias (e.g., copper or tungsten) that route an IC to appropriate external bond pad connections on a die. Accordingly, the interconnect network 127a routes the IC 126a to the bond pads 108a and the interconnect network 127b routes the IC 126b to the bond pads 108b. The substrate 110 couples the bond pads 108a-b through the top-side bond pads 114 to bottom-side bond pads 128. Figure 2D shows a side view of the interconnect networks 127a-b, and electrical couplings with the corresponding bond pads 108a-b. Figure 2D also shows electrical isolation of the spacer sites 106 from the interconnect network 127a. The spacer sites 106 are electrically isolated, at least in part, by a dielectric layer 129 that surrounds and isolates the spacer sites 106 from the bond pads 108a. The spacer sites 106 are further electrically isolated by the lack of an internal connection to the first interconnect network 127a in the first die 102a. The dielectric layer 129 can comprise a non-conductive oxide, such as deposited silicon dioxide, and the spacer sites 106 and bond pads 108a-b may comprise a variety of conventional metals or metal alloys (e.g., aluminum, copper, gold, or an alloy of these materials). The spacer sites 106, for example, can be formed during fabrication of the first die 102a concurrently with the bond pads 108a.

[0025] Because the spacer sites 106 are metallic, a conventional wire bonding and/or soldering process may be used to attach the metal spacers 104 to the spacer sites 106 for spacing the first and second dies 102a-b from each other. Returning again to Figure 2A, a process for attaching the metal spacers 104 and stacking the first and second dies 102a-b may include, for example, forming the adhesive layer 116 on the substrate 110; attaching the first die 102a to the adhesive layer 116; forming wire bonds between the bond pads 108a and the bond pads 114; attaching the metal spacers 104 to the spacer sites 106; depositing a filler material on the front-side surface of the first die 102a; and attaching the second die 102b to the metal spacers 104.

[0026] The metal spacers 104 may be formed in a variety of ways. In one embodiment, the metal spacers 104 are made from a wire bond material and formed concurrently with a wire bonding process. In this embodiment, each tier of the individual metal spacers 104 comprises a metal bump formed by a wire bonder. In another embodiment, a soldering process could be used to form a single tier of metal bumps on the spacer sites 106 and optionally on the bond pads 108a as well. The metal bumps on the spacer sites 106 serve as a first tier of the metal spacers 104. On other hand, the metal bumps on the bond pads 108a can be used to electrically couple a wire to the first die 102a. The metal spacers 104 of this embodiment are completed by forming a second tier of metal bumps on top of the first tier of metal bumps. An alternative embodiment for forming the metal spacers 104 includes individually soldering or otherwise positioning preformed single- or multi-tiered metal spacers on the spacer sites 106. Also, in further embodiments, a packaged microelectronic device may be created by forming a casing over the assembly 100 to encapsulate the first and second dies 102a-b, the wire bonds 112a-b, and a top-side surface portion of the substrate 110. Embodiments of packaged devices are illustrated in further detail with reference to Figures 8-10.

[0027] The embodiment of the assembly 100 shown in Figures 2A-D, as well as several alternative embodiments, can mitigate or eliminate several challenges of stacking dies on each other. For example, several embodiments of the metal spacers 104 provide incompressible spacers that can be fabricated during the wire bonding process without additional equipment or processing steps. Many embodiments of the metal spacers 104 accordingly act like a silicon spacer without the cost and processing equipment needed for silicon spacers. Additionally, several embodiments of the metal spacers 104 may be placed adjacent to wire bonds or at outermost edges of a die to ensure that the first and second dies 102a-b in the assembly 100 are substantially parallel with respect to each other. Such embodiments of the metal spacers 104 accordingly avoid misalignment errors associated with epoxy spacers.

[0028] Figures 3A-C are cross-sectional views showing several examples of metal spacers that can be used in the stacked die assembly 100 shown in Figures 2A-D, or in any of the alternative embodiments described below. Figure 3A, for example, shows an embodiment of the metal spacer 104 having first and second spacer elements, such as spherical metal bumps 130 and 131

with respective diameters d_1 and d_2. The sum of the diameters d_1 and d_2 establish a spacing distance h_1 between the first and second dies 102a-b. The spherical metal bumps 130 and 131 may comprise a variety of materials, such as gold, aluminum, tin, silver, lead, an alloy of these materials, or other suitable dimensionally stable materials. In one specific embodiment, the diameters d_1 and d_2 of the metal bumps can be about 10 to 75 micrometers. Thus, the spacing distance h_1 of such an embodiment can be approximately 20 to 150 micrometers. Figure 3B shows an alternative embodiment of the metal spacer 104 comprising stacked metal bumps 130 and 131. Each of the metal bumps 130 and 131 is compressed along an axis creating respective minor diameters d_3 and d_4 that establish a spacing distance h_2 between the first and second dies 102a-b. Such compressed, flattened, or "coined" metal bumps may provide increased stability relative to purely spherically metal bumps. However, a variety of other metal bump stack configurations may be used. For example, Figure 3C shows an embodiment of the metal spacer 104 comprising a flattened metal bump 130 that provides a wider base on which to deposit a spherical metal bump 131.

[0029] Figure 4 is an isometric view of an embodiment showing alternative placements of the metal spacers 104 on the first die 102a. The second die 102b has been removed to show a tripod arrangement of the metal spacers 104 on an interior surface portion of the first die 102a. The arrangement of metal spacers 104 shown in Figure 4 may allow more room for additional bond pads 136 at edges of the die 102a, and the tripod arrangement uses only three metal spacers for supporting and spacing an attached die. Other arrangements of metal spacers are also possible; alternative arrangements could include using more than three metal spacers 104 or placing metal spacers on both the interior surface and the edge surface portions of the die 102a.

[0030] Figures 5A-C illustrate an alternative embodiment of a stacked die assembly 140 having a first die 144a, a second die 144b stacked on one side of the first die 144a, and an interposer substrate 147 at the other side of the first die 144a. The first and second dies 144a-b are generally similar to the first and second dies 102a-b, but the first and second dies 144a-b do not have electrically isolated spacer sites. Instead, as best shown in Figure 5B, the assembly 140 has "stitched" metal spacers 142 at the front side of the first die 144a and below the back side of the second die 144b. Referring to Figure 5B, individual metal spacers 142 have a first spacer element 142a and a second spacer element 142b. The assembly 140 further includes stitched wire

bonds 143 projecting from individual first spacer elements 142a. The bond pads 108a accordingly define spacer sites in lieu of the spacer sites 106 shown in Figure 2A. In the specific embodiment shown in Figure 5A, the stitched wire bonds 143 and metal spacers 142 are positioned only near the corners of the first and second dies 144a-b. The metal spacers 142 are also electrically active because they are on the bond pads 108a, and thus the assembly 140 further has a dielectric layer 145 on the back side of the second die 144b to electrically isolate the second die 144b from the metal spacers 142. The assembly 140 may be manufactured similarly to the process of manufacturing the assembly 100 of Figure 2A.

[0031] Figure 5C shows a cross-sectional view of interconnect networks 127a-b and electrical couplings with the corresponding bond pads 108a-b. Figure 5C also shows the dielectric layer 145 on the backside of the second die 144b electrically isolating the second die 144b from the metal spacers 142. The dielectric layer 145 may comprise a variety of materials, such as, for example, an adhesive material for attaching the second die 144b to the metal spacers 142. Alternatively, the dielectric layer 145 may comprise a non-conductive oxide that has been thermally grown or deposited on the back side of the second die 144b. In general, the dielectric layer 145 should be substantially non-conductive to prevent electrical conduction between the metal spacers 142 and the second die 144b.

[0032] Figures 6A-E are cross-sections showing stages of an embodiment of a method for forming stitched metal spacers. In Figure 6A, a tip 158 of a first metal wire 160a is melted to form a first metal bump 162a. The first bump 162a serves as a bottom or first spacer element of the stitched metal spacer. The diameter of the first bump 162a may be tailored by heating the tip 158 until a desired diameter is achieved. Alternatively, the overall height of a metal spacer may be adjusted by flattening a metal bump to a desired size (described further with reference to Figure 6C). Figure 6B shows the first wire 160a after it has been bent and pressed against a bond pad 164, for example, by a wire bonding tool. The wire bonding tool applies mechanical force, heat, and/or ultrasonic energy until a metallic connection is created between the first bump 162a and the bond pad 164. The remaining portion of the first wire 160a may then be stitched to external bond pads of the interposer substrate. In an alternative embodiment, Figure 6C shows the first bump 162a after it has been flattened or coined by applying mechanical pressure to the top and bottom sides of the first

bump 162a. An individual metal bump may be flattened immediately after formation, or all of the metal bumps on a die may be simultaneously flattened by compressing the metal bumps against a flat surface.

[0033] Figure 6D shows a second metal bump 162b on the first bump 162a and a second wire 160b projecting from the second bump 162b. Figure 6E shows the first and second bumps 162a-b and the metal wire 160a after the metal wire 160b has been removed, which may leave a small wire tail 166 that projects away from the metal bump 162b. The wire tail 166 may be pressed into the metal bump (i.e., via a flattening process) or the wire tail 166 may be sufficiently small so as to be negligible. The first and second bumps 162a-b form the stitched metal spacer 142. To ensure that the first wire 160a does not contact a microelectronic die stacked on the stitched metal spacer 142, the second bump 162b should extend above the first wire 160a. Figure 6E shows a separation distance h_3 between the top of the second bump 162b and the first wire 160a. In certain embodiments, larger diameter metal bumps may be needed for wires having significant curvature. Alternatively, three or more stacked metal bumps may create an appropriate separation distance between the back side of a die and a curved wire (described further with reference to Figures 8-10).

[0034] Figure 6F shows an embodiment of the spacer 104 that has been adapted from the stitched metal spacer 142. In this embodiment both the first and second wires 160a-b have been removed to create stacked metal bumps 162a-b. Figure 6F also shows wire tails 166a-b projecting away from the respective metal bumps 162a-b. The wire tails 166a-b may be removed, for example, by a flattening process.

[0035] Figure 7 is an isometric view of stitched metal spacer placement according to an alternative embodiment. The second die 144b (Figures 5A-C) has been removed in this figure to show an arrangement of the stitched metal spacers 142 on front-side bond pads 108a. The bond pads 108a alternate between conventional wire bond couplings 174 and the stitched metal spacers 142. Relative to the embodiment of the assembly 140 in Figures 5A-C, in which the stitched metal spacers 142 are at the corners of the dies, the arrangement of stitched and conventional wire bonds shown in Figure 7 provides support between the first and second dies 144a-b along more points. It is also contemplated that a variety of additional arrangements are possible, such as metal spacers with both stitched and non-stitched spacer elements, and/or stitched and non-stitched spacers. For

example, stitched metal spacers may be formed along edges of the first die 144a and non-stitched metal spacers may be formed at interior surface portions of the first die 144a.

[0036] Figure 8 is a cross-sectional view of an embodiment of a packaged microelectronic device 180 that includes a first microelectronic die 186, a second microelectronic die 188 spaced apart from the first die 186 by stitched metal spacers 190, and a casing 182 formed over the first and second dies 186 and 188. The first die 186 has a larger perimeter than the second die 188. First and second wires 192a and 192b, respectively, couple the first and second dies 186 and 188 to an interposer substrate 194. The metal spacers 190 in this embodiment include three-tiered metal spacers to provide more spacing between the first wires 192a and the second die 188. Additionally, the first wires 192a are coupled to second-tier metal bumps 190b so that the first wires 192a extend above the corner and surface portions of the first die 186. In alternative embodiments, and depending on the relative perimeter sizes of the first and second dies 186 and 188, the wires 192 can be coupled with first-tier metal bumps 190a or third-tier metal bumps 190c.

[0037] Figure 9 is a cross-sectional view of another embodiment of a packaged microelectronic device 200 that includes three microelectronic dies 204a-c and a casing 202 formed over the dies 204a-c. The device 200 can have two-tiered stitched metal spacers 206 separating the first die 204a from the second die 204b and three-tiered stitched metal spacers 208 separating the second die 204b from the third die 204c. In this embodiment, the two-tiered metal spacers 206 prevent the first wires 210a from contacting a surface of the second die 204b. Because second wires 210b have a smaller radius of curvature than the first wires 210a, the additional metal bump in the three-tiered metal spacers 208 spaces the second wires 210b sufficiently apart from a back side surface of the third die 204c to prevent contact therebetween. In additional or alternative embodiments, metal spacers comprising four or more metal bumps may be used to separate individual microelectronic dies. Furthermore, other embodiments may include four or more stacked microelectronic dies.

[0038] Figure 10 is a cross-sectional view of the packaged microelectronic device 200 comprising non-stitched interior metal spacers 210 and 212. In this embodiment, dies supported by multi-tiered metal spacers having three or more metal bumps may receive increased structural support with interior metal spacers.

[0039] Any one of the packaged microelectronic devices described above with reference to Figures 2A-10 can be incorporated into any of a myriad of larger and/or more complex systems 490, a representative one of which is shown schematically in Figure 11. The system 490 can include a processor 491, a memory 492 (e.g., SRAM, DRAM, Flash, and/or other memory device), input/output devices 493, and/or other subsystems or components 494. Microelectronic devices may be included in any of the components shown in Figure 11. The resulting system 490 can perform any of a wide variety of computing, processing, storage, sensor, imaging, and/or other functions. Accordingly, representative systems 490 include, without limitation, computers and/or other data processors, for example, desktop computers, laptop computers, Internet appliances, hand-held devices (e.g., palm-top computers, wearable computers, cellular or mobile phones, personal digital assistants), multi-processor systems, processor-based or programmable consumer electronics, network computers, and mini computers. Other representative systems 490 include cameras, light or other radiation sensors, servers and associated server subsystems, display devices, and/or memory devices. In such systems, individual dies can include imager arrays, such as CMOS imagers. Components of the system 490 may be housed in a single unit or distributed over multiple, interconnected units, e.g., through a communications network. Components can accordingly include local and/or remote memory storage devices, and any of a wide variety of computer-readable media.

[0040] From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the invention. For example, many of the elements of one embodiment can be combined with other embodiments in addition to or in lieu of the elements of the other embodiments. Additionally, in several embodiments, the metal spacers can be single, dimensionally stable posts or other stanchion-like members projecting from discrete spacer sites. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

I/We claim:

[c1] 1. A method of manufacturing a microelectronic device, the method comprising:

forming a plurality of multi-tiered metal spacers having first spacer elements on a front-side surface of a first microelectronic die and second spacer elements on corresponding first spacer elements;

attaching a back-side surface of a second microelectronic die to the second spacer elements; and

wherein at least one of the first and second spacer elements is electrically isolated from at least one of the front-side surface of the first die and the back-side surface of the second die.

[c2] 2. The method of claim 1, wherein the first spacer elements are formed by forming wire bond balls on the first die.

[c3] 3. The method of claim 1, further comprising constructing individual wires coupled to at least one of the first and second spacer elements.

[c4] 4. The method of claim 1, wherein attaching the back-side surface of the second die includes depositing a filler material on the front-side surface of the first die and pressing the second die onto the filler material.

[c5] 5. The method of claim 1, further comprising forming at least three metal spacers.

[c6] 6. The method of claim 1, wherein the first and second dies have equivalent exterior perimeters.

[c7] 7. The method of claim 1, wherein the first die has an exterior perimeter that is larger than an exterior perimeter associated with the second die.

[c8] 8. The method of claim 1, wherein the first and second spacer elements comprise a stack of first and second metal bumps.

[c9] 9. The method of claim 1, wherein a portion of the metal spacers is positioned at an interior portion of the first die.

[c10] 10. The method of claim 9, wherein the metal spacers further comprise a third metal bump.

[c11] 11. The method of claim 1, wherein the first die has metal spacer sites and bond sites at the front-side surface, the metal spacer sites being electrically isolated from the bond sites and integrated circuitry of the first die, and the process of forming the multi-tiered spacers comprises forming first metal bumps on the spacer sites and second metal bumps on the first metal bumps.

[c12] 12. The method of claim 1, wherein the first die has integrated circuitry and bond pads at the front side surface electrically coupled to the integrated circuitry, and the process of forming the multi-tiered spacers comprises forming first metal bumps on the bond pads and second metal bumps on the first metal bumps.

[c13] 13. A method of manufacturing a microelectronic device, the method comprising:

forming a non-compressible metal spacer on a surface of a spacer site at a front side of a first microelectronic die, wherein the spacer site is electrically isolated from an integrated circuit of the first die; and

attaching a second microelectronic die to the metal spacer.

[c14] 14. The method of claim 13, wherein the spacer comprises a metal spacer having at least two tiers of spacer elements.

[c15] 15. The method of claim 13, wherein the spacer sites comprise metal pads.

[c16] 16. The method of claim 13, wherein forming the spacer comprises:
attaching a first metal bump to the spacer site; and
depositing a second metal bump on top of the first metal bump.

[c17] 17. The method of claim 16, further comprising increasing a spacing distance between the first die and the second die by disposing a third metal bump on top of the second metal bump.

[c18] 18. The method of claim 16, further comprising flattening at least one of the first metal bump and the second metal bump.

[c19] 19. A method of manufacturing a microelectronic device, the method comprising:
attaching first wire bonds to bond sites at a front-side surface of a first microelectronic die, wherein a portion of individual first wire bonds are bottom-tier spacer elements;
covering at least a portion of a back side of a second microelectronic die with a dielectric material;
coupling top-tier spacer elements to the bottom-tier spacer elements; and
attaching the electrically insulated portion of the second die to the top-tier spacer elements.

[c20] 20. The method of claim 19, wherein coupling the top-tier spacer elements further comprises:
attaching second wire bonds to individual bottom-tier spacer elements; and
removing excess wire from the second wire bonds.

[c21] 21 A microelectronic device, comprising:

a first microelectronic die having a front side with bond sites and wire bonds coupled to the bond sites;

a second microelectronic die having a back side; and

a plurality of metal spacers interposed between the first and second dies, wherein the metal spacers are coupled with the front-side surface of the first die and the back-side surface of the second die, and wherein the metal spacers are electrically isolated from at least one of the first and second dies.

[c22] 22. The microelectronic device of claim 21, wherein the metal spacers comprise first spacer elements and second spacer elements stacked on the first spacer elements.

[c23] 23. The microelectronic device of claim 22, wherein individual first spacer elements comprise a metal ball and a wire bond projection from the metal ball.

[c24] 24. The microelectronic device of claim 20, further comprising:

a casing housing the first and second dies;

a filler layer interposed between the first and second dies; and

an interposer substrate attached to the casing and the first die, wherein the substrate routes electrical connections within the casing to bond pads exterior to the casing.

[c25] 25. The microelectronic device of claim 21, further comprising metal spacer sites at the front side of the first die that are electrically isolated from integrated circuitry of the first die, wherein individual metal spacers are attached to individual metal spacer sites.

[c26] 26. The microelectronic device of claim 21, further comprising a dielectric layer on the back side of the second die and contacting the metal spacers.

[c27] 27. A computing system, comprising a processor, a memory, and an input/output device, wherein the computing system includes the microelectronic device according to claim 21.

[c28] 28. A microelectronic device, comprising:

an interposer substrate with bond pads;

a first microelectronic die on the interposer substrate, the first die comprising an integrated circuit and a front-side surface that includes a plurality of spacer sites, wherein the spacer sites are electrically isolated from the integrated circuit;

a plurality of metal spacers coupled to the spacer sites;

a second microelectronic die having a back-side surface coupled to the metal spacers; and

a plurality of first and second wire bonds respectively electrically coupling the first and second dies to the interposer substrate, wherein a portion of the first wire bonds is between the first and second dies.

[c29] 29. The microelectronic device of claim 28, wherein the first die comprises a dielectric layer electrically isolating the spacer sites from the integrated circuit.

[c30] 30. The microelectronic device of claim 29, further comprising:

an interconnect network coupled to the integrated circuit; and

a plurality of metal bond pads coupled to the interconnect network, wherein the dielectric layer isolates the metal bond pads from the spacer sites.

[c31] 31. A microelectronic device, comprising:

a first microelectronic die having a front-side surface and a plurality of wire bonds coupled thereto;

a second microelectronic die having a back-side surface and a dielectric layer on the back-side surface; and

a plurality of metal spacers contacting the dielectric layer and having individual wire bonds.

[c32] 32. The microelectronic device of claim 31, wherein the insulating layer comprises at least one of an oxide film and an adhesive layer.

[c33] 33. The microelectronic device of claim 31, wherein individual first metal spacers comprise stitched metal bumps.

[c34] 34. The microelectronic device of claim 33, wherein individual second metal spacers comprise non-stitched metal bumps.