

ANTI-FUSE STRUCTURE, ANTI-FUSE ARRAY AND MEMORY

ABSTRACT

Embodiments of the disclosure relate to an anti-fuse structure, which includes: a first unit and a second unit, the first unit including a first selection transistor, a first anti-fuse (AF) cell and a second AF cell, the second unit including a second selection transistor, a third AF cell and a fourth AF cell. The first unit and the second unit share an active region, the active region is provided with a first extension part and a second extension part which are independent of each other at a first side, and the active region is provided with a third extension part and a fourth extension part which are independent of each other at a second side, the first side being opposite to the second side. The first AF cell is arranged at the first extension part, the second AF cell is arranged at the second extension part, the third AF cell is arranged at the third extension part, and the fourth AF cell is arranged at the fourth extension part. The anti-fuse structure can improve the distribution density of AF cells and meet the miniaturization requirements.

[Fig. 1A]