

RF SIGNAL PARAMETER MEASUREMENT IN AN INTEGRATED CIRCUIT FABRICATION CHAMBER

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INCORPORATION BY REFERENCE

[0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in its entirety and for all purposes.

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BACKGROUND

[0002] Fabrication of integrated circuit devices may involve the processing of semiconductor wafers in a semiconductor processing chamber. Typical processes may involve deposition, in which a semiconductor structure may be built on or over a substrate such as by way of a layer-by-layer process. Typical processes may also involve removal (e.g., etching) of material from certain regions of the semiconductor wafer. In commercial-scale manufacturing processes, each wafer contains many copies of a set of semiconductor devices, and many wafers may be utilized to achieve the required volumes of semiconductor devices. Accordingly, the commercial viability of a semiconductor processing operation may depend, at least to some extent, upon within-wafer uniformity and upon wafer-to-wafer repeatability of process conditions. Consequently, efforts are made to ensure that each portion of a given wafer, as well as each wafer processed in a semiconductor processing chamber, is subjected to tightly-controlled processing conditions. Variations in processing conditions can bring about undesirable variations in deposition and etch rates, which, in turn, may bring about unacceptable variations in overall fabrication processes. Such variations may degrade circuit performance which, in turn, may give rise to unacceptable variations in performance of higher-level systems that utilize the integrated circuit devices. Accordingly, techniques for monitoring semiconductor processes with increased granularity, as well as an ability to make fine adjustments to process variables during fabrication, continues to be an active area of investigation.

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[0003] The background description provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not

otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

SUMMARY

- 5 [0004] In one embodiment an apparatus is utilized to estimate parameters of a radio frequency (RF) signal coupled to an integrated circuit fabrication chamber. The apparatus may include a voltage sensor configured to provide an indication of a voltage of the RF signal. The apparatus also includes a current sensor configured to provide an indication of a current conducted by the RF signal. The apparatus also includes an analog-to-digital conversion
- 10 module coupled to an output port of the voltage sensor and to an output port of the current sensor, the analog-to-digital converter is configured to provide digital representations of an instantaneous voltage and an instantaneous current of the RF signal. The apparatus also includes one or more processors configured to transform the digital representations of the instantaneous voltage and the digital representations of the instantaneous current into frequency
- 15 domain representations of a complex voltage corresponding to the RF signal voltage and into frequency domain representations of a complex current corresponding to the RF signal current. The one or more processors are additionally configured to combine frequency domain representations of a complex voltage and the complex current.
- [0005] In other implementations, the one or more processors of the apparatus are configured
- 20 to perform a Fast Fourier Transforms (FFT) of the digital representation of the instantaneous voltage of the RF signal and of the instantaneous current of the RF signal. In another implementation, the voltage sensor of the apparatus includes a capacitive voltage sensor. In another implementation, the current sensor includes an inductive current transformer. In an implementation, the analog-to-digital conversion module is configured to apply a successive-
- 25 approximation technique. In another implementation, the RF signal is provided by an RF power generator, which provides at least 2 frequency components. In an implementation, the at least 2 frequency components include a first component having a frequency of about 400 kHz and a second component having a frequency of about 13.56 MHz. In an implementation, the one or more processors of the apparatus are additionally configured to apply one or more
- 30 calibration coefficients to the frequency domain representations of the complex voltage and to apply one or more calibration coefficients to the frequency domain representations of the complex current. In an implementation, the one or more processors are additionally configured to aggregate the complex voltage and the complex current to form root mean square voltage

and rms current. In an implementation, the apparatus is exclusive of a voltage divider. In an implementation, the apparatus is exclusive of a peak detector. In an implementation, apparatus is exclusive of a buffer amplifier. In an implementation, the frequency domain representations of the complex voltage and the complex current are combined to obtain actual power delivered to a process station. In an implementation, the frequency domain representations of the complex voltage and the complex current are combined to obtain power factor at the process station.

[0006] In another embodiment an apparatus may be adapted or configured to estimate radio frequency (RF) power coupled to a station of an integrated circuit fabrication chamber. The apparatus may include a voltage sensor configured to provide an indication of a voltage of the RF signal. The apparatus also includes a current sensor configured to provide an indication of the current conducted by the RF signal. The apparatus also includes an analog-to-digital conversion module coupled to an output port of the voltage sensor and to an output port of the current sensor, the analog-to-digital converter configured to provide digital representations of an instantaneous voltage and an instantaneous current of the RF signal. The apparatus may include one or more processors configured to obtain the digital representations of the instantaneous voltage of the RF signal and the digital representations of the instantaneous current conducted by the RF signal. The one or more processes may transform the obtained digital representations of the instantaneous voltage of the RF signal and the obtained instantaneous current of the RF signal into frequency domain representations of a complex voltage corresponding to the voltage of the RF signal and into frequency domain representation of a complex current corresponding to the current conducted by the RF signal. In an implementation, the apparatus is additionally configured to combine the complex voltage of the RF signal and the complex current of the RF signal.

[0007] In an implementation, the one or more processors of the apparatus is configured to transform the obtained digital representations of the instantaneous voltage of the RF signal and the instantaneous current conducted by the RF signal utilizing a Fast Fourier Transform. In an implementation, the one or more processors of the apparatus is additionally configured to apply one or more calibration coefficients to the complex voltage of the RF signal and the complex current conducted by the RF signal. In an implementation, the one or more processors of the apparatus is additionally configured to aggregate the complex voltage of the RF signal and the complex current of the RF signal to form root mean square voltage and root mean square current. In an implementation, the one or more processors of the apparatus is additionally

configured to utilize the complex voltage of the RF signal and the complex current of the RF signal to obtain power delivered to a station of the integrated circuit fabrication chamber. In an implementation, the one or more processors of the apparatus is additionally configured to utilize the complex voltage of the RF signal and the complex current of the RF signal to obtain a ratio of power delivered to forward power at the station of the integrated circuit fabrication chamber. In an implementation, the apparatus is exclusive of a buffer amplifier.

5 [0008] In an implementation, an integrated circuit fabrication chamber, includes a radio frequency (RF) signal generator configured to couple an RF signal to the integrated circuit fabrication chamber. The integrated circuit fabrication chamber also includes a first sensor
10 configured to sense voltage of the RF signal. The integrated circuit fabrication chamber also includes a second sensor configured to sense current conducted via the RF signal. The integrated circuit fabrication chamber also includes one or more analog-to-digital converters coupled to an output port of the first sensor and to an output port of the second sensor, the one or more analog-to-digital converters configured to convert sensed voltages and currents to
15 digital representations. The integrated circuit fabrication chamber also includes one or more processors configured to transform the digital representations to frequency domain representations of the complex voltage of the RF signal and to transform the digital representations to frequency domain representations of the complex current conducted via the RF signal, the one or more processors additionally configured to combine the complex voltage
20 of the RF signal and the complex current of the RF signal.

[0009] In an implementation, the integrated circuit fabrication chamber is configured to perform Fast Fourier Transform of the digital representation of the instantaneous voltage of the RF signal and of the instantaneous current conducted via the RF signal. In an implementation, the RF signal generator of the integrated circuit fabrication chamber is configured to provide 2
25 or more frequency components to the integrated circuit fabrication chamber. In an implementation, the integrated circuit fabrication chamber receives 2 or more frequency components including a signal below about 2 MHz a signal above about 2 MHz. In an implementation, the integrated circuit fabrication chamber includes 2 or more process stations. In an implementation, the integrated circuit fabrication chamber includes 4 process stations. In
30 an implementation, the integrated circuit fabrication chamber is exclusive of a peak detector. In an implementation, the integrated circuit fabrication chamber is exclusive of a buffer amplifier.

[0010] In some embodiments, an apparatus is utilized to estimate parameters of an RF signal coupled to an integrated circuit fabrication chamber. The apparatus may include a voltage sensor configured to provide an indication of a voltage of the RF signal. The apparatus may include a current sensor configured to provide an indication of a current conducted by the RF signal. The apparatus may include an analog-to-digital converter configured to receive outputs from the voltage sensor and the current sensor and configured to provide digital representations of the voltage of the RF signal and the current conducted by the RF signal based on the inputs from the voltage sensor and the current sensor. The apparatus may include one or more processors configured to determine, based on the digital representations of the voltage and the current of the RF signal: a peak voltage associated with the digital representation of the voltage, a peak current associated with the digital representation of the current, and power characteristics associated with the RF signal.

[0011] In an implementation, the one or more processors are further configured to determine phases associated with the digital representations of the voltage and the current. In an implementation, the power characteristics are based on the determined phases.

[0012] In an implementation, the one or more processors are further configured to determine an impedance based on the peak voltage and the peak current.

[0013] In an implementation, the apparatus may further include a plurality of voltage sensors included the voltage sensor and a plurality of current sensors associated with the current sensor. The apparatus may include a multiplexer. The multiplexer may be configured to: select a voltage sensor of the plurality of voltage sensors and a current sensor of the plurality of current sensors; and provide outputs of the selected voltage sensor and the selected current sensor to the analog-to-digital converter.

[0014] In an implementation, the voltage sensor comprises a capacitive voltage sensor.

[0015] In an implementation, the current sensor comprises an inductive transformer.

[0016] In an implementation, the RF signal is provided by an RF power generator that provides at least 2 frequency components. In another implementation, the RF signal is provided by an RF power generator that provides one frequency component

[0017] In an implementation, the one or more processors comprise a Field Programmable Gate Array (FPGA).

[0018] In an implementation, the digital representations are at a sampling rate typically greater than about 100 MHz.

[0019] In an implementation, the power characteristics comprise a power factor.

[0020] In an implementation, the one or more processors are further configured to communicate data via a serial communication protocol, via Ethernet, or via another digital communication protocol.

5 [0021] In an implementation, the one or more processors are further configured to provide outputs to an Ethernet for Control Automation Technology (EtherCAT) system. In an implementation, the EtherCAT system is configured to provide instructions to one or more elements in a matching network or other RF distribution system.

[0022] In an implementation, the one or more processors are configured to: 1) provide calibration coefficients to the voltage sensor for storage in memory associated with the voltage
10 sensor; or 2) provide calibration coefficients to the current sensor for storage in memory associated with the current sensor. In an implementation, the calibration coefficients are determined for a plurality of RF signal frequencies. In an implementation, the calibration coefficients are determined using a modular calibration method that comprises: determining an effect of one or more cables that electrically couple the voltage sensor and the current sensor
15 to the analog-to-digital converter; or determining an effect of a controller that receives outputs from the voltage sensor and the current sensor via the one or more cables. In an implementation, the calibration coefficients are determined using an end-to-end calibration method that comprises determining transformation functions that relate outputs of the one or more processors to characteristics of the RF signal.

20 [0023] In an implementation, 1) the voltage sensor is configured to provide identifying information to the one or more processors; or 2) the current sensor is configured to provide identifying information to the one or more processors. In an implementation, the identifying information comprises the calibration coefficients. In an implementation, 1) the voltage sensor is configured to provide identifying information to the one or more processors at a system
25 power on time or a system reset time; or 2) the current sensor is configured to provide identifying information to the one or more processors at the system power on time or the system reset time.

[0024] In an implementation, the one or more processors are further configured to determine a complex representation of the voltage and a complex representation of the current, wherein
30 the peak voltage is determined based on the complex representation of the voltage, and wherein the peak current is determined based on the complex representation of the current. In an implementation, the complex representation of the voltage is determined by mixing the digital representations of the voltage with cosine and sine waveforms associated with the RF signal,

and wherein the complex representation of the current signal is determined by mixing the digital representations of the current with the cosine and sine waveforms associated with the RF signal. In an implementation, the cosine and sine waveforms associated with the RF signal are generated by a Numerically Controlled Oscillator (NCO) that acts as a Local Oscillator. In an implementation, the one or more processors are further configured to determine an estimate of a frequency of the RF signal, and wherein the estimate of the frequency of the RF signal is used to generate the cosine and sine waveforms associated with the RF signal. In an implementation, the one or more processors are further configured to: determine a phase of the digital representation of the voltage or a phase of the digital representation of the current, wherein the frequency estimate is determined based on the phase of the digital representation of the voltage or the phase of the digital representation of the current. In an implementation, the frequency estimate is a derivative of the phase of the digital representation of the voltage or is a derivative of the digital representation of the current. In an implementation, the one or more processors are further configured to inhibit use of outputs of the voltage sensor and/or use of outputs of the current sensor in response to determining that a difference between a current estimate of the frequency and a preceding estimate of the frequency exceeds a predetermined threshold. In an implementation, the one or more processors are further configured to down-sample the complex representation of the voltage and to down-sample the complex representation of the current. In an implementation, the one or more processors are configured to down-sample the complex representation of the voltage and to down-sample the complex representation of the current using a decimation filter.

[0025] In some embodiments, a method is utilized for identifying anomalous conditions associated with a process chamber. The method comprises obtaining indications of one or more trigger events. The method further comprises detecting occurrence of a trigger event of the one or more trigger events. The method further comprises in response to detecting occurrence of the one or more trigger events, obtaining samples of one of: RF voltage signals from a voltage sensor or samples of RF current signals from a current sensor. The method further comprises determining a frequency domain representation of the samples of RF voltage signals or of the samples of RF current signals. The method further comprises identifying an anomaly in the frequency domain representation. The method further comprises causing an indication of the anomaly to be stored in a log.

[0026] In an implementation, the one or more trigger events comprise at least one of: a powering on of an RF signal generator, a change in a process condition, a voltage measured

by the voltage sensor exceeding a voltage threshold, or a current measured by the current sensor exceeding a current threshold.

[0027] In an implementation, determining the frequency domain representation comprises determining a Fast Fourier Transform (FFT) of the samples of the RF voltage signals or the samples of the RF current signals.

[0028] In an implementation, the samples are obtained for a predetermined time period subsequent to detection of the trigger event. In an implementation, the predetermined time period is within a range of about 10 milliseconds – 1 second.

[0029] In an implementation, the anomaly in the frequency domain representation comprises excess energy in a frequency band. In an implementation, the frequency band includes a harmonic of an RF signal generated by an RF signal generator.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] Figure 1A shows a substrate processing apparatus for depositing or etching a film on or over a semiconductor substrate utilizing any number of processes, according to various implementations.

[0031] Figure 1B depicts a schematic view of an implementation of a multi-station processing tool.

[0032] Figure 2 is a schematic diagram showing a circuit involving a fabrication chamber as well as RF signal generation and measurement components, according to an implementation.

[0033] Figure 3 is a diagram showing processes involved in measurement of RF signal current and voltage parameters, according to an implementation.

[0034] Figure 4 is a flowchart for a method of measuring RF signal parameters, according to an implementation.

[0035] Figure 5 is a schematic diagram of an apparatus adapted or configured to measure RF signal parameters, according to an implementation.

[0036] Figure 6 is a flowchart for a method of measuring RF signal parameters in an integrated circuit fabrication chamber, according to an implementation.

[0037] Figure 7 is a block diagram illustrating components of a system for measurement of RF signal current and voltage parameters associated with multiple voltage and current sensors, according to an implementation.

[0038] Figure 8 is a block diagram illustrating components of a system for measurement of RF signal current and voltage parameters, according to an implementation.

[0039] Figure 9 is a block diagram illustrating components for down-converting RF current signals and RF voltage signals, according to an implementation.

[0040] Figure 10 is a block diagram illustrating components for filtering and down-sampling RF current signals and RF voltage signals, according to an implementation.

5 [0041] Figure 11 is a block diagram illustrating components for determining magnitude and phase information of RF current signals and RF voltage signals, according to an implementation.

[0042] Figure 12 is a block diagram illustrating a process for determining magnitude, phase, and power characteristics of RF current and RF voltage signals, according to an
10 implementation.

[0043] Figure 13 is a flowchart for a method of determining magnitude, phase, and power characteristics of RF current and RF voltage signals, according to an implementation.

[0044] Figures 14A and 14B are schematic diagrams illustrating points of interest in calibration of a system for determining magnitude, phase, and power characteristics of RF
15 current and RF voltage signals, according to an implementation.

[0045] Figures 15A and 15B are flowcharts of methods of calibration of a system for determining magnitude, phase, and power characteristics of RF current and RF voltage signals, according to an implementation.

[0046] Figure 16 is a flowchart for a method of using frequency domain representations of
20 RF current and voltage signals, according to an implementation.

DETAILED DESCRIPTION

[0047] In particular implementations, such as implementations related to plasma-enhanced or plasma-assisted integrated circuit manufacturing processes, one or more high-power RF
25 signals may be utilized to form an ionized plasma material. Formation of an ionized plasma material may enable precursor gases to undergo appropriate chemical reactions, which result in deposition or removal of semiconductor material from a wafer undergoing processing. Accordingly, accurate determination of RF signal parameters, such as RF voltage, RF current, as well as phase relationships between RF current and voltage, may be useful in determining
30 RF power delivered, RF power reflected, for example, which may be utilized to exercise control over various semiconductor processes. Such processes may include deposition of a semiconductor material on or over a substrate as well as removal (e.g., etching) of material at one or more locations of the wafer. For example, in certain plasma-mediated semiconductor

processes, accurate control over RF signal parameters may permit control over rates of material deposition or removal, deposition or etch uniformity across a wafer, stress introduced by deposited materials, and so forth.

[0048] In a multi-station integrated circuit fabrication chamber, in which multiple semiconductor wafers simultaneously undergo deposition or etching processes, measurement of RF signal parameters utilized in the formation of plasma may enhance uniformity of processes among various stations of the multi-station fabrication chamber. In such processing environments, in response to conditions within an individual station of a fabrication chamber resulting in changes to input impedance of the individual station, component values of an RF matching network may be adjusted so as to reduce variations in RF power coupled to the individual stations. Such precise adjustment of component values of the impedance matching network may enable coupling of a specific quantity of power into the fabrication chamber while minimizing power reflected from the fabrication chamber. Consequently, semiconductor processes conducted within a multi-station fabrication chamber may be performed with greater accuracy, which may, in turn, result in lower defect ratios and higher yields of devices formed utilizing the fabrication chamber.

[0049] In certain implementations, accurate determination of parameters of a signal from an RF power generator may allow characterization of current and voltage waveforms that may be prone to bringing about undesirable or abnormal operation of an integrated circuit fabrication chamber. For example, in certain situations, if RF power coupled to a process station of a multi-station fabrication chamber exceeds a threshold level, an anomalous plasma event (e.g., formation of an electric arc) may occur. In some instances, such an event may bring about formation of unwanted gaseous compounds, which may impede a semiconductor process. In some instances, an anomalous plasma event (e.g., formation of an electric arc) may damage a semiconductor wafer undergoing processing, which may necessitate inspection of the affected wafer outside of the process station. In certain other situations, if RF power coupled to a process station drops below a threshold level, plasma formation may be degraded or extinguished entirely. In some instances, extinguishing of an ionized plasma material may bring about an imbalance in deposition rates occurring at stations of a multi-station fabrication chamber. Consequently, at least in certain instances, responsive to the extinguishing of a plasma at a process station, the process station may be required to undergo plasma restarting operations. Such plasma restarting or re-initiation operations may delay fabrication processes (e.g., material deposition, material etch, and so forth).

- [0050] In particular instances, accurate measurement the power of an RF signal coupled to a fabrication chamber may additionally impact operations conducted at other process stations of a multi-station fabrication chamber. For example, if power from an RF power generator is distributed among 2 or more process stations, an increase in RF power coupled to a first process station may bring about a corresponding reduction in power coupled to one or more other process stations. In some instances, in response to an increase in power coupled to a first station of a multi-station fabrication chamber, power to a second station of the fabrication chamber may fall below a threshold amount, which may cause plasma extinguishing in the second station. In such an instance, as previously alluded to, fabrication processes at the second station may consume longer periods of time, which may increase cost, decrease equipment availability for other processing operations, and/or decrease quality of a deposited film. In some instances, excessive occurrences of plasma extinguishing may bring about the need for additional processing and/or metrology to determine if quality of a fabricated wafer has been negatively impacted.
- [0051] Particular implementations may represent improvements over alternative approaches of measuring or estimating power coupled from an RF signal utilized in plasma-assisted/plasma-enhanced fabrication processes. For example, in one or more of such alternative approaches, power of an RF signal may be estimated utilizing techniques that employ voltage division, peak detection, and/or use of buffer amplifiers. Consequently, especially with respect to the use of peak detection, such alternative approaches may give rise to inaccurate measurement of the current and voltage present in an RF signal. Such inaccuracies may distort the computing of the power of an RF signal which may, in turn, bring about unwarranted increases/decreases in power output of an RF signal generator. Such unwarranted increases/decreases in RF power coupled to stations of a multi-station fabrication chamber may bring about unwanted and/or unproductive variations in processes conducted at stations of the fabrication chamber. Such variations may affect the quality and cost of fabricated integrated circuit wafers, impede processing operations, and give rise to additional undesirable consequences. Certain embodiments herein do not employ voltage division, peak detection, and/or buffer amplifiers. Certain embodiments herein use the entire current and voltage signals (e.g., full wave signals) obtained from sensors conveying power, such as RF power, to a plasma reactor. In some cases, these signals are obtained in plasma reactors employing plasma generated by application of multiple radio frequencies.

[0052] Certain implementations may be utilized in conjunction with a number of wafer fabrication processes, such as various plasma-enhanced atomic layer deposition (ALD) processes, various plasma-enhanced chemical vapor deposition (CVD) processes, or may be utilized on-the-fly during single deposition processes. In certain implementations, an RF power generator having multiple output ports may be utilized at any signal frequency, such as at frequencies between about 300 kHz and about 60 MHz, which may include frequencies of about 400 kHz, about 1 MHz, about 2 MHz, about 13.56 MHz, and/or about 27.12 MHz. However, in other implementations, RF power generators having multiple output ports may operate at any signal frequency, which may include relatively low frequencies, such as between about 50 kHz and about 300 kHz, as well as higher signal frequencies, such as frequencies between about 60 MHz and about 100 MHz.

[0053] It should be noted that although particular implementations described herein may show and/or describe multi-station semiconductor fabrication chambers having 4 (four) process stations, implementations are intended to embrace multi-station integrated circuit fabrication chambers having or utilizing any number of process stations. Thus, in certain implementations, individual output ports of an RF power generator having multiple output ports may be assigned to a process station of a multi-station fabrication chamber having, for example, 2 process stations or 3 process stations. In other implementations individual output ports of an RF power generator having multiple output ports may be assigned to process stations of a multi-station integrated circuit fabrication chamber having a larger number of process stations, such as 5 process stations, 6 process stations, 8 process stations, 10 process stations, or any other number of process stations. Further, embodiments of the disclosure apply to chambers having only a single process station. Additionally, although particular implementations described herein may show and/or describe utilization of a single, relatively low frequency RF signal, such as a frequency of between about 300 kHz and about 2 MHz, as well as a single, relatively high-frequency RF signal, such as a frequency of between about 2 MHz and about 100 MHz, the disclosed implementations are intended to embrace the use of any number of frequencies below about 2 MHz as well as any number of frequencies above about 2 MHz.

[0054] Turning now to the figures, Figure 1A shows a substrate processing apparatus 100 for depositing films on or over a semiconductor substrate utilizing any number of processes, according to various implementations. Processing apparatus 100 of Figure 1A may employ a single process station 102 of a process chamber with a single substrate holder 108 (e.g., a pedestal) in an interior volume, which may be maintained under vacuum by vacuum pump 118.

Showerhead 106 and gas delivery system 101, which may be fluidically coupled to the process chamber, may permit the delivery of film precursors, for example, as well as carrier and/or purge and/or process gases, secondary reactants, etc. Equipment utilized in the generation of plasma within the process chamber is also shown in Figure 1A. The apparatus schematically illustrated in Figure 1A may be adapted for performing, in particular, plasma-enhanced CVD.

[0055] In Figure 1A, gas delivery system 101 includes a mixing vessel 104 for blending and/or conditioning process gases for delivery to showerhead 106. One or more mixing vessel inlet valves 120 may control introduction of process gases to mixing vessel 104. Particular reactants may be stored in liquid form prior to vaporization and subsequent delivery to process station 102 of a process chamber. The implementation of Figure 1A includes a vaporization point 103 for vaporizing liquid reactant to be supplied to mixing vessel 104. In some implementations, vaporization point 103 may include a heated liquid injection module. In some other implementations, vaporization point 103 may include a heated vaporizer. In yet other implementations, vaporization point 103 may be eliminated from the process station. In some implementations, a liquid flow controller upstream of vaporization point 103 may be provided for controlling a mass flow of liquid for vaporization and delivery to process station 102.

[0056] Showerhead 106 may operate to distribute process gases and/or reactants (e.g., film precursors) toward substrate 112 at the process station, the flow of which may be controlled by one or more valves upstream from the showerhead (e.g., valves 120, 120A, 105). In the implementation depicted in Figure 1A, substrate 112 is depicted as located beneath showerhead 106, and is shown resting on a pedestal 108. Showerhead 106 may include any suitable shape, and may include any suitable number and arrangement of ports for distributing process gases to substrate 112. In some implementations involving 2 or more stations, gas delivery system 101 includes valves or other flow control structures upstream from the showerhead, which can independently control the flow of process gases and/or reactants to each station so as to permit gas flow to one station while prohibiting gas flow to a second station. Furthermore, gas delivery system 101 may be configured to independently control process gases and/or reactants delivered to each station in a multi-station apparatus such that the gas composition provided to different stations is different; e.g., the partial pressure of a gas component may vary between stations at the same time.

[0057] In the implementation of Figure 1A, gas volume 107 is depicted as being located beneath showerhead 106. In some implementations, pedestal 108 may be raised or lowered to

expose substrate 112 to gas volume 107 and/or to vary the size of gas volume 107. Optionally, pedestal 108 may be lowered and/or raised during portions of the deposition process to modulate process pressure, reactant concentration, etc., within gas volume 107. Showerhead 106 and pedestal 108 are depicted as being electrically coupled to RF signal generator 114 and matching network 116 for coupling power to a plasma generator. Thus, showerhead 106 may function as an electrode for coupling radio frequency power into process station 102. In some implementations, the plasma energy is controlled (e.g., via a system controller having appropriate machine-readable instructions and/or control logic) by controlling one or more of a process station pressure, a gas concentration, power output of an RF signal generator, and so forth. For example, RF signal generator 114 and matching network 116 may be operated at any suitable RF power level, which may operate to form plasma having a desired composition of radical species. In addition, RF signal generator 114 may provide RF power having more than one frequency component, such as a low-frequency component (e.g., less than about 2 MHz) as well as a high frequency component (e.g., greater than about 2 MHz).

[0058] In some implementations, plasma ignition and maintenance conditions are controlled with appropriate hardware and/or appropriate machine-readable instructions in a system controller which may provide control instructions via a sequence of input/output control instructions. In one example, the instructions for bringing about ignition or maintaining a plasma are provided in the form of a plasma activation portion of a process recipe. In some cases, process recipes may be sequentially arranged, so that at least some instructions for the process can be executed concurrently. In some implementations, instructions for setting one or more plasma parameters may be included in a recipe preceding a plasma ignition process. For example, a first recipe may include instructions for setting a flow rate of an inert (e.g., helium) and/or a reactant gas, instructions for setting a plasma generator to a power set point and time delay instructions for the first recipe. A second, subsequent recipe may include instructions for enabling the plasma generator and time delay instructions for the second recipe. A third recipe may include instructions for disabling the plasma generator and time delay instructions for the third recipe. It will be appreciated that these recipes may be further subdivided and/or iterated in any suitable way within the scope of the present disclosure. In some deposition processes, a duration of a plasma strike may correspond to a duration of a few seconds, such as from about 3 seconds to about 15 seconds, or may involve longer durations, such as durations of up to about 30 seconds, for example. In certain implementations described herein, much shorter plasma strikes may be applied during a processing cycle. Such plasma

strike durations may be on the order of less than about 50 milliseconds, with about 25 milliseconds being utilized in a specific example.

- [0059] For simplicity, processing apparatus 100 is depicted in Figure 1A as a standalone station (102) of a process chamber for maintaining a low-pressure environment. However, it may be appreciated that a plurality of process stations may be included in a multi-station processing tool environment, such as shown in Figure 1B, which depicts a schematic view of an implementation of a multi-station processing tool. Processing tool 150 employs an integrated circuit fabrication chamber 165 that includes multiple fabrication process stations, each of which may be used to perform processing operations on a substrate held in a wafer holder, such as pedestal 108 of Figure 1A, at a particular process station. In the implementation of Figure 1B, the integrated circuit fabrication chamber 165 is shown as having four process stations 151, 152, 153, and 154. However, in certain other implementations, multi-station processing apparatuses may have more or fewer process stations depending on the implementation and, for instance, the desired level of parallel wafer processing, size/space constraints, cost constraints, etc. Figure 1B additionally shows substrate handler robot 175, which may operate under the control of system controller 190, configured to move substrates from a wafer cassette (not shown in Figure 1B) from loading port 180 and into multi-station integrated circuit fabrication chamber 165, and onto one of process stations 151, 152, 153, and 154.
- [0060] Figure 1B also depicts an implementation of a system controller 190 employed to control process conditions and hardware states of process tool 150. System controller 190 may include one or more memory devices, one or more mass storage devices, and one or more processors. The one or more processors may include a central processing unit, analog and/or digital input/output connections, stepper motor controller boards, etc. In some implementations, system controller 190 controls all of the activities of process tool 150. System controller 190 executes system control software stored in a mass storage device, which may be loaded into a memory device, and executed by a processor of the system controller. Software to be executed by a processor of system controller 190 may include instructions for controlling the timing, mixture of gases, fabrication chamber and/or station pressure, fabrication chamber and/or station temperature, wafer temperature, substrate pedestal, chuck and/or susceptor position, number of cycles performed on one or more substrates, and other parameters of a particular process performed by process tool 150. These programmed processes may include various types of processes including, but not limited to, processes related to determining an

amount of accumulation on a surface of the chamber interior, processes related to deposition of film on substrates including numbers of cycles, determining and obtaining a number of compensated cycles, and processes related to cleaning the chamber. System control software, which may be executed by one or more processors of system controller 190, may be configured in any suitable way. For example, various process tool component subroutines or control objects may be written to control operation of the process tool components necessary to carry out various tool processes.

[0061] In some implementations, software for execution by way of a processor of system controller 190 may include input/output control sequencing instructions for controlling the various parameters described above. For example, each phase of deposition and deposition cycling of a substrate may include one or more instructions for execution by system controller 190. The instructions for setting process conditions for an ALD/CFD deposition process phase may be included in a corresponding ALD/CFD deposition recipe phase. In some implementations, the recipe phases may be sequentially arranged, so that all instructions for a process phase are executed concurrently with that process phase.

[0062] Other computer software and/or programs stored on a mass storage device of system controller 190 and/or a memory device accessible to system controller 190 may be employed in some implementations. Examples of programs or sections of programs for this purpose include a substrate positioning program, a process gas control program, a pressure control program, a heater control program, and a plasma control program. A substrate positioning program may include program code for process tool components that are used to load the substrate onto pedestal 108 (of Figure 1A) and to control the spacing between the substrate and other parts of process tool 150. A positioning program may include instructions for appropriately moving substrates in and out of the reaction chamber as necessary to deposit films on substrates and clean the chamber.

[0063] A process gas control program may include code for controlling gas composition and flow rates and for flowing gas into one or more process stations prior to deposition to bring about stabilization of the pressure in the process station. In some implementations, the process gas control program includes instructions for introducing gases during formation of a film on a substrate in the reaction chamber. This may include introducing gases for a different number of cycles for one or more substrates within a batch of substrates. A pressure control program may include code for controlling the pressure in the process station by regulating, for example, a throttle valve in the exhaust system of the process station, a gas flow into the process station,

etc. The pressure control program may include instructions for maintaining the same pressure during the deposition of differing numbers of cycles on one or more substrates during the processing of the batch.

5 **[0064]** A heater control program may include code for controlling the current to heating unit 110 that is used to heat the substrate. Alternatively, the heater control program may control delivery of a heat transfer gas (such as helium) to the substrate.

10 **[0065]** In some implementations, there may be a user interface associated with system controller 190. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

15 **[0066]** In some implementations, parameters adjusted by system controller 190 may relate to process conditions. Non-limiting examples include process gas composition and flow rates, temperature, pressure, plasma conditions, etc. These parameters may be provided to the user in the form of a recipe, which may be entered utilizing the user interface. The recipe for an entire batch of substrates may include compensated cycle counts for one or more substrates within the batch in order to account for thickness trending over the course of processing the batch.

20 **[0067]** Signals for monitoring the process may be provided by analog and/or digital input connections of system controller 190 from various process tool sensors. The signals for controlling the process may be output by way of the analog and/or digital output connections of process tool 150. Non-limiting examples of process tool sensors that may be monitored include mass flow controllers, pressure sensors (such as manometers), thermocouples, etc. Sensors may also be included and used to monitor and determine the accumulation on one or more surfaces of the interior of the chamber and/or the thickness of a material layer on a substrate in the chamber. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain process conditions.

30 **[0068]** System controller 190 may provide program instructions for implementing the above-described deposition processes. The program instructions may control a variety of process parameters, such as DC power level, pressure, temperature, number of cycles for a substrate, amount of accumulation on at least one surface of the chamber interior, etc. The instructions may control the parameters to operate in-situ deposition of film stacks according to various implementations described herein.

[0069] For example, the system controller may include control logic for performing the techniques described herein, such as determining an amount of accumulated deposition material currently on at least an interior region of the deposition chamber interior, applying the amount of accumulated deposition material determined in (a), or a parameter derived therefrom, to a relationship between (i) a number of ALD cycles required to achieve a target deposition thickness, and (ii) a variable representing an amount of accumulated deposition material, in order to obtain a compensated number of ALD cycles for producing the target deposition thickness given the amount of accumulated deposition material currently on the interior region of the deposition chamber interior, and performing the compensated number of ALD cycles on one or more substrates in the batch of substrates. The system may also include control logic for determining that the accumulation in the chamber has reached an accumulation limit and stopping the processing of the batch of substrates in response to that determination, and for causing a cleaning of the chamber interior.

[0070] In addition to the above-identified functions and/or operations performed by system controller 190 of Figure 1B, the controller may additionally control and/or manage the operations of RF signal generator 114. RF signal generator 114 may provide an output signal, which may be conveyed to an RF signal distribution unit 195, which may divide the power of the input signal into, for example, 4 output signals. Output signals from RF signal distribution unit 195 may exhibit similar levels of RF voltage and RF current, which may be conveyed to multi-station integrated circuit fabrication chamber 165 via input ports 167. In certain implementations, as described further herein, operations controlled via system controller 190 may relate to determining upper and lower thresholds for RF signal power to be delivered to integrated circuit fabrication chamber 165, determining actual (such as real-time) levels of RF signal power delivered to integrated circuit fabrication chamber 165, RF signal power activation/deactivation times, RF signal on/off duration, duty cycle, operating frequency, and so forth. Additionally, system controller 190 may determine one or more normal operating parameters of RF power to be delivered to integrated circuit fabrication chamber 165 by way of input ports 167. Such parameters may include upper and lower thresholds of, for example, power reflected from one or more of input ports 167 in terms of a reflection coefficient (e.g., the scattering parameter S_{11}), voltage standing wave ratio, upper and lower thresholds of a voltage applied to one or more of input ports 167, upper and lower thresholds of current conducted through one or more of input ports 167, as well as an upper threshold for a magnitude of a phase angle between a voltage and a current conducted through input ports 167. Such

thresholds may be utilized in defining “out-of-range” RF signal characteristics. For example, reflected power greater than an upper threshold may indicate an out-of-range RF power parameter. Likewise, an applied voltage or conducted current having a value below a lower threshold or greater than an upper threshold may indicate out-of-range RF signal characteristics. Similarly, a phase angle between an applied voltage and conducted current being greater than an upper threshold may indicate an out-of-range RF power parameter.

[0071] In particular implementations, multi-station integrated circuit fabrication chamber 165 may include input signal ports in addition to input ports 167 (additional input ports not shown in Figure 1B). In particular implementations, process stations of integrated circuit fabrication chamber 165 may utilize first and second input ports in which a first input port may convey a signal having a first frequency and in which a second input port may convey a signal having a second frequency. Use of 2 or more frequencies may bring about enhanced plasma characteristics, which may give rise to deposition rates within particular limits and/or more easily controlled deposition rates. Use of 2 or more frequencies may bring about other desirable consequences. In certain implementations, frequencies of between about 300 kHz and about 100 MHz may be utilized. In some implementations, signal frequencies of about 2 MHz or less may be referred to as low frequency (LF) while frequencies greater than about 2 MHz may be referred to as high frequency (HF).

[0072] It may be appreciated that regardless of the frequencies of RF voltage and current signals coupled to multi-station integrated circuit fabrication chamber 165, it may be advantageous to measure such signals with an increased degree of accuracy. For example, for sinusoidal voltage and current signals that are in phase with each other, average RF power coupled to multi-station integrated circuit fabrication chamber 165 may be computed substantially in accordance with expression (1) below:

$$P_{avg} = \frac{1}{2} V_{peak} \times I_{peak} \quad (1)$$

Wherein V_{peak} corresponds to a peak voltage signal, and wherein I_{peak} corresponds to a peak current signal. However, it may be appreciated that power computed by way of expression (1), which specifies the use of peak RF voltage and peak RF current, may introduce inaccuracies since steady state or root mean square (RMS) levels of RF voltage and RF current may deviate significantly from peak values. For example, if RF voltage and current waveforms do not exhibit purely sinusoidal behavior, such that RF voltage and RF current achieve peak values for only a brief instant, computation of average RF power may overestimate actual power coupled to a fabrication chamber. Similarly, responsive to non-sinusoidal RF voltage and RF

current waveforms reaching peak values for significant durations may result in underestimation of actual power coupled to a fabrication chamber. It may be appreciated that in both instances, such as overestimation or underestimation of RF power coupled to a fabrication chamber, any adjustments of parameters of RF signal generator 114 could potentially give rise to incorrect adjustment of RF signal generator output power parameters.

[0073] Accordingly, at least in particular implementations, it may be advantageous to formulate or compute power coupled to a fabrication chamber utilizing instantaneous levels of RF voltage applied by an RF signal and a current conducted by the RF signal. Such computations may more accurately represent levels of RF power coupled to a fabrication chamber which, in turn, may bring about tighter control, greater uniformity, greater repeatability, etc., as these pertain to fabrication processes performed via a fabrication chamber.

[0074] Figure 2 is a schematic diagram showing a circuit involving a fabrication chamber as well as RF signal generation and measurement components, according to an implementation.

Although Figure 2 shows RF signal generator 114 providing a signal to a single process station 151, in other implementations, such as described in relation to Figure 1B, RF signal generator 114 may provide a signal to RF signal distribution unit 195. In an implementations, RF signal distribution unit 195 unit is configured to divide power from a single RF input port to 2 or more output ports for coupling to input ports 167 of fabrication chamber 165 as shown in Figure 2.

To simplify the operations depicted in Figure 2, additional components utilized in association with a fabrication chamber, such as power supplies, impedance matching units, RF power dividers, and so forth are omitted from Figure 2.

[0075] In implementation 200, the complex impedance of a station, such as process station 151, of multi-station integrated circuit fabrication chamber 165 may be modeled and/or characterized by equivalent circuit 151A that includes a series and/or parallel lumped circuit having a capacitance C151 and a resistance R151. Capacitance C151 and resistance R151 are depicted as being in parallel with inductance L151. In some implementations, the complex impedance of a station of a multi-station integrated circuit fabrication chamber, as represented by equivalent circuit 151A may include a capacitance having a value of between about 1.5 nF and about 3.5 nF and may include a resistance of between about 5 ohms and about 10 ohms. In particular implementations, capacitor C151 may assume a value of about 2.0 nF and about 3.0 nF, and resistor R151 may assume a value of between about 6.5 ohms and about 8.5 ohms. However, the disclosed implementations are intended to embrace any real or complex

impedance formed by series and/or parallel combinations of resistive and reactive circuit elements presented by a process station of an integrated circuit fabrication chamber. In certain implementations, a complex impedance presented by process station 151 of multi-station integrated circuit fabrication chamber 165 may be dependent upon one or more reactive gases and/or vapors present in the chamber, partial and total pressures of gases, and other factors. Thus, for certain pressure/gas combinations, chamber 165 may present a predominantly capacitive load while for other pressure/gas combinations, chamber 165 may present a predominantly inductive load, for example.

[0076] In the implementation of Figure 2, voltage sensor 205 is coupled to a transmission line, such as a coaxial cable, for example, disposed between RF signal generator 114 and process station 151 of multi-station integrated circuit fabrication chamber 165 (as represented by equivalent circuit 151A). In particular implementations, voltage sensor 205 may correspond to a capacitive voltage sensor having a relatively high input impedance that occasionally or periodically samples a voltage at node V_{RF} shown in Figure 2 without consuming a significant electric current. The implementation of Figure 2 also includes current sensor 210 (e.g., an inductive current transformer), which may be coupled in series between RF signal generator 114 and multi-station integrated circuit fabrication chamber 165 (as represented by equivalent circuit 151A). In particular implementations, current sensor 210 may correspond to an inductive current transformer having a relatively low input impedance that occasionally or periodically samples a current conducted from RF signal generator 114 without bringing about any significant voltage drop.

[0077] In particular implementations, voltage sensor 205 may include a voltage divider network, in which a voltage may be measured across a known lower resistance in comparison to a total resistance of known higher & lower resistor combination. In such a network, the actual voltage of the RF signal may be scaled by dividing the voltage measured across the known resistance by the sum of the 2 known resistances. In other instances, voltage sensor 205 may include a capacitive voltage divider. In such a network, the voltage of the RF signal may be scaled by dividing the voltage measured across a known capacitance in relation to the sum of the 2 known capacitances combined in series. In certain other implementations, RF signal parameter measurement may involve direct voltage sensing, in which voltage of an RF signal may be directly measured or sampled without (or exclusive of) a voltage divider network and/or without (or exclusive of) a capacitive voltage divider. Implementations may embrace

alternative voltage measurement approaches other than those disclosed, which may result in measurement of voltage between RF signal generator 114 and equivalent circuit 151A.

[0078] In particular implementations, current sensor 210 may include a transformer coil coupled to a conductor conducting an RF current from an RF signal generator 114 to a process station. In such instances, a current conducted via a transmission line between RF signal generator 114 and a process station (e.g. process station 151) may be measured utilizing an inductive coil coupled to the transmission line. In such instances, a relatively small current may be induced in the inductive coil in relation to a current conducted through the transmission line. In such a sensor, the actual current conveyed by the RF signal may be scaled by considering the current measured in the inductive coil in relation to the coupling factor between current sensor 210 and the transmission line between RF signal generator 114 and a process station. Implementations may embrace alternative current measurement approaches other than those disclosed, which may result in measurement of voltage between RF signal generator 114 and a process station.

[0079] As shown in Figure 2, a voltage at node V_{RF} can be characterized as a conventional sinusoidal voltage or as a complex sinusoidal signal, having a peak amplitude indicated by V_{PK} as depicted in graph 205A. Thus, in particular implementations, V_{RF} may be characterized as a sinusoidal signal superimposed on a pulse train in which intermittently-pulsed sinusoidal RF signals are conveyed to a process station (e.g., process station 151). Alternatively, in certain other implementations, V_{RF} may include a plurality of sinusoidal RF signals, such as signals having a first frequency superimposed on a pulse train, wherein a sinusoidal RF signal of a second frequency is superimposed on the sinusoidal RF signal of the first frequency. Accordingly, V_{RF} of the implementation of Figure 2 is intended to represent any number of composite waveforms having pulsed (e.g., relatively square-wave) components, saw-toothed (e.g., ramped) components, as well as any number of other components, and the disclosed implementations are not intended to be limited in this respect.

[0080] Similarly, graph 210A of Figure 2 also depicts a sinusoidal electric current (I_{RF}) conducted through current sensor 210. As shown in graph 210A, an RF signal conveyed through current sensor 210 (I_{RF}) includes a peak current I_{PK} having a period corresponding to a frequency of between, for example, about 300 kHz and about 100 MHz with an additional $\pm 10\%$ (for example) frequency fine-tuning capability. In certain other implementations, I_{RF} may be characterized by a sinusoidal RF waveform having a first frequency superimposed on a pulse train, wherein a sinusoidal RF signal of a second frequency is superimposed on the

sinusoidal RF signal of the first frequency. Accordingly, I_{RF} of the implementation of Figure 2 is intended to embrace any number of composite waveforms having pulsed (e.g., relatively square wave) components, saw-toothed (e.g., ramped) components, as well as any number of other components.

5 [0081] Figure 3 is a diagram showing processes involved in measurement of RF signal current and voltage parameters, according to an implementation 300. In Figure 3, voltage sensor 305 may include a voltage sensor disposed at a transmission line, such as a coaxial cable, which conveys a high-power RF signal between an RF signal generator and a process station of a multi-station integrated circuit fabrication chamber. As depicted in Figure 3, voltage
10 sensor 305 may interface with voltage divider 315, which may operate to make an output signal of voltage sensor 305 available to a peak detector, such as peak detector 325. An output signal of peak detector 325 may be conveyed to buffer amplifier 335, which may operate to provide a input high impedance so as not to distort an output signal from peak detector 325. Output signals from buffer amplifier 335 may be calibrated, such as via applying calibration
15 coefficients stored by way of a lookup table, for example, by two-dimensional calibration circuit 345. In particular implementations, two-dimensional calibration circuit 345 includes frequency dependent coefficients that operate to adjust the levels of signals representing peak voltages provided by peak detector 325.

[0082] Similarly, current sensor 310 may include a current sensor disposed at a transmission
20 line, such as a coaxial cable, which conveys a high-power RF signal between an RF signal generator and a process station of a multi-station integrated circuit fabrication chamber. As depicted in Figure 3, current sensor 310 may interface with voltage divider 320, which may operate to make an output signal of voltage sensor 305 available to a peak detector, such as peak detector 330. An output signal of peak detector 330 may be conveyed to buffer amplifier
25 340, which may operate to provide a input high impedance so as not to distort an output signal from peak detector 330. Output signals from buffer amplifier 340 may be calibrated, such as via applying calibration coefficients stored by way of a lookup table, for example, by two-dimensional calibration circuit 350. In particular implementations, two-dimensional calibration circuit 350 includes frequency dependent coefficients that operate to adjust the
30 levels of signals representing peak current levels provided by peak detector 330. Thus, in particular implementations, average RF power coupled to a station of multi-station integrated circuit fabrication chamber 165 may be computed substantially in accordance with expression (2) below:

$$P_{avg} = \frac{1}{2} V_{PK(CAL)} \times I_{PK(CAL)} \quad (2)$$

Wherein $V_{PK(CAL)}$ and $I_{PK(CAL)}$ correspond to calibrated output signals from two-dimensional calibration circuits 345 and 350, respectively.

[0083] Figure 4 is a flowchart for a method of measuring RF signal parameters, according to an implementation 400. It should be noted that the disclosed implementations, such as those of Figure 4 and Figure 6, are intended to embrace variations of the respective figures, including methods that include actions in addition to those depicted in the figures, actions performed in an order different than those depicted in the figures, as well as methods including fewer steps than those depicted. The method of Figure 4 begins at 410, which may include sensing of voltage and current magnitudes, such as by way of voltage sensor 305 and current sensor 310 as indicated in Figure 3. The method of Figure 4 may additionally include application of bandpass filter, such as at 420, which may operate to remove noise and/or out-of-band signals as well as other signal distortions in measured current and voltage magnitudes. At 430, a filtered voltage may be applied to a peak detector, which may employ a sample-and-hold technique to measure a peak voltage and/or a peak current of an RF signal conveyed from an RF signal generator to one or more stations of a multi-station integrated circuit fabrication chamber. At 440, an output of a peak detector may be measured and digitized. At 450, parameters from detected voltage and current peaks may be computed. In some instances, computing operations of 450 may include computing real and/or imaginary power conveyed in a signal from an RF signal generator as well as voltage and current values, phase relationships between voltage and current signals, and so forth.

[0084] It may be appreciated that, at least under particular circumstances, the apparatus and method of Figures 3 and 4 may apply to RF signals having frequencies within particular ranges. It may also be appreciated that particular processes referred to in Figures 3 and 4 may provide RF current and voltage measurements having at least some degree of accuracy when RF signal waveforms are at least approximately sinusoidal. Accordingly, if RF voltage and current measurements are performed utilizing waveforms that deviate significantly from sinusoidal waveforms, accuracy of voltage and current measurements may degrade. It may also be appreciated that, at least in particular instances, signal construction may be dependent upon the bandwidth of any analog-to-digital converters, which might be utilized at 440 of Figure 4. Further, in response to noise signals being present in RF signal waveforms, accuracy of sensed voltages and currents may be negatively impacted.

[0085] Thus, particular implementations of RF current and voltage measurements may represent an improvement over techniques identified utilizing the apparatus and method of Figures 3 and 4. Hence, Figure 5, which avoids at least some of the drawbacks brought about by the apparatus and method of Figures 3 and 4, shows a schematic diagram of an apparatus adapted or configured to measure RF signal parameters, according to an implementation 500. In Figure 5, waveforms corresponding to voltage of an RF signal as well as current conducted by an RF signal may be coupled to an analog-to-digital conversion module 510. In the implementation of Figure 5, voltage and current waveforms may be represented by approximately sinusoidal waveforms (e.g., waveforms 205A and 210A), although the disclosed implementations are not limited to sinusoidal variations in RF voltage and current.

[0086] As depicted in Figure 5, voltage and current waveforms 205A and 210A may be converted to digital representations, such as by way of analog-to-digital conversion module 510. In particular instances, analog-to-digital conversion module 510 may involve a successive-approximation technique to arrive at digital representations of analog voltages of an RF signal as well as digital representations of current conducted by an RF signal. In such instances, an input voltage or current signal is held steady by a sample-and-hold circuit while a flash analog-to-digital converter quantizes the sampled signal into a relatively small number of binary digits (e.g., 3 binary digits, 4 binary digits, 5 binary digits, etc.). The sampled binary digits are then coupled to a digital-to-analog converter, which may be accurate to, for example, 12 binary digits. An analog output signal from the digital-to-analog converter may then be subtracted from the input signal to the analog-to-digital converter. The difference between the analog output signal from the digital-to-analog converter and the input signal to the analog-to-digital converter, which may be considered a “residue,” is amplified and coupled to a subsequent stage of the analog-to-digital converter, and the above-described process may be repeated. In such a successive-approximation architecture, the amplified residue is conveyed through successive stages of the converter, thereby providing small number of binary digits at each stage (e.g., 3 binary digits, 4 binary digits, 5 binary digits, etc.), until the residue reaches a subsequent flash analog-to-digital converter, which operates to resolve the least-significant binary digits.

[0087] It should be noted that although analog-to-digital conversion module 510 is shown as a single module, in some implementations, analog-to-digital conversion module 510 may include separate analog-to-digital modules, such as computing modules. For example, in some implementations, analog-to-digital conversion module 510 may include a first analog-to-digital

module to perform conversion of an analog voltage waveform to a stream of instantaneous values of a digitized voltage. A second analog-to-digital module may perform conversion of an analog current waveform to a stream of instantaneous values of a digitized current.

[0088] Responsive to conversion of signals representing instantaneous voltages and instantaneous currents of signals from an RF signal generator, signals from analog-to-digital conversion module 510 can be conveyed to input ports of a processor module 520. Processor module 520 may include signal processor 522 and general-purpose processor 524, which may operate to transform the digital representations of the instantaneous voltage into frequency domain representations of a complex voltage corresponding to the RF signal voltage. Signal processor 522 may additionally operate to transform the digital representations of the instantaneous analog current into frequency domain representations of a complex current corresponding to the RF signal current. Accordingly, in a particular example, a purely sinusoidal waveform of voltage ($V(t)$) having a period of about 1 μ s may be transformed, such as by signal processor 522, to a frequency domain representation having a corresponding single frequency of about 1 MHz. In at least certain implementations, off-the-shelf equipment may perform at least some of the functions performed by processor 520.

[0089] In particular implementations, frequency domain representations of complex voltage and complex current may be represented by a polar or phasor notation, in which a magnitude of the complex current and/or the complex voltage may be expressed in conjunction with a phase angle (e.g., phasor notation). In other implementations, frequency domain representations of complex voltage and complex current may be represented by a real component (e.g., real voltage) and an imaginary component (e.g., imaginary voltage). Thus, signal processor 522 of processor module 520 may operate to extract real and imaginary voltage (V_{RF}) components and/or to extract real and imaginary current components (I_{RF}) of an RF signal. In particular implementations, signal processor 522 is capable of extracting voltage and current waveforms ($V(t)$ and $I(t)$) such as of Figure 2 to form complex voltage and complex current values, which may be represented as:

$$V(t) = V_{RE}(k) + jV_{IM}(k) \quad (2A)$$

$$I(t) = I_{RE}(k) + jI_{IM}(k) \quad (2B)$$

In which the quantities $V_{RE}(k)$ and $jV_{IM}(k)$ correspond to real and imaginary components that correspond to instantaneous values of voltage and current sampled utilizing signal processor 522. In expressions (2A) and (2B), k is a descriptor corresponding to a value sampled at a particular sampling interval. In particular implementations, signal processor 522 may perform

a transform that corresponds to a Fast Fourier Transform (FFT). However, in alternative implementations, signal processor 522 may perform other types of mathematical operations, such as a Discrete Fourier Transform, for example.

[0090] In the implementation of Figure 5, following transformation of instantaneous values of voltage and current waveforms into digitized representations of such waveforms, general-purpose processor 524 may obtain such digitized representations. In certain implementations, general-purpose processor may access a database, for example, which may store a lookup table to provide calibration coefficients for digitized representations of current and voltage as a function of frequency. In an example implementation, such calibration coefficients may relate to corrections expressed in terms of a scattering parameter (e.g. S_{21}), such as from a scattering matrix $\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$, which may characterize for frequency-dependent deviations from ideal scattering parameters. In another example implementation, calibration coefficients may relate to frequency-dependent corrections expressed in terms of conventions other than scattering parameters, such as parameters of the "transmission" or $\begin{bmatrix} A & B \\ C & D \end{bmatrix}$ matrix, a "hybrid" or $\begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix}$ matrix, etc.

[0091] In particular implementations, general-purpose processor 524 may combine digitized representations corresponding to voltage and current signals generated by an RF signal source to form, for example, root mean square (RMS) voltage (V_{RMS}) and RMS current (I_{RMS}). In particular implementations, RMS current may be expressed as a summation of sampled values of real and imaginary current, obtained substantially in accordance with expression (3) below:

$$I_{RMS} = \sqrt{\sum_{i=0}^{\frac{k}{2}-1} (I_{Re}^2(i) + I_{Im}^2(i))} \quad (3)$$

Wherein $I_{Re}^2(i)$ and $I_{Im}^2(i)$ refer to values of instantaneously-sampled current, in which "k" samples may be obtained over a sampling period, such as 1 second. In particular implementations, RMS current may be expressed as a summation of sampled values of real and imaginary voltage, obtained substantially in accordance with expression (4), below:

$$V_{RMS} = \sqrt{\sum_{i=0}^{\frac{k}{2}-1} (V_{Re}^2(i) + V_{Im}^2(i))} \quad (4)$$

Wherein $V_{Re}^2(i)$ and $V_{Im}^2(i)$ refer to values of instantaneously-sampled voltage, in which “ k ” samples may be obtained over a sampling period, such as 1 second.

[0092] General-purpose processor 524 of Figure 5 may be additionally be configured to combine digitized representations corresponding to voltage and current signals from an RF source to generate instantaneous values of RF power conveyed to a process station. In particular implementations, RF power may be computed substantially in accordance with expression (4), below:

$$P_{FWD} = I_{rms} * V_{rms} \quad (4)$$

General-purpose processor 524 of Figure 5 may additionally be configured to determine actual power delivered, which may be computed via combining sampled values of real and imaginary voltage and currents in which “ k ” samples may be obtained over a sampling period, such as 1 second. Actual power delivered may be computed substantially in accordance with expression (5), below:

$$P_{DEL} = \sum_{i=0}^{\frac{k}{2}-1} (V_{RE}(i) * I_{RE}(i) + V_{IM}(i) * I_{IM}(i)) \quad (5)$$

Wherein the quantities V_{RE} and I_{RE} represent real voltage and current components (respectively) and wherein V_{IM} and I_{IM} represent imaginary voltage and current components (respectively). Further, computed forward and delivered power may be combined to compute a power factor, which refers to a ratio of power coupled to a load impedance (e.g., a process station of a multi-station fabrication chamber) versus power incident at the process station. Power factor at the process station, which may degrade responsive to incident power being reflected from the process station back to the RF signal generator, may be computed substantially in accordance with expression (6) below:

$$Power\ Factor = \frac{P_{DEL}}{P_{FWD}} \quad (6)$$

[0093] Figure 6 is a flowchart for a method of measuring RF signal parameters in an integrated circuit fabrication chamber, according to an implementation. The method of Figure 6 may be performed utilizing the apparatus of Figure 5 described herein as well as utilizing voltage sensor 205 and current sensor 210 of Figure 2. The method of Figure 6 may begin at 610, which may include obtaining samples (e.g., analog samples) of magnitudes of current and voltage of RF signals. Such signals may include signal frequencies, for example, or may include a composite of 2 or more frequencies, such as frequencies between about 300 kHz and

about 500 kHz, as well as frequencies in the megahertz range, such as frequencies of 13.56 MHz and/or about 27.12 MHz.

[0094] At 620, the obtained samples of voltage and current magnitudes may be converted to digital representations of voltage and current samples. In particular implementations, conversion operations of 620 may be performed by 2 separate (e.g., standalone) converters, which may operate as analog-to-digital converters. In certain implementations, a first analog-to-digital converter may digitize an output signal from a voltage sensor and a second analog-to-digital converter may digitize an output signal from a current sensor. In other implementations, analog-to-digital conversion operations at 620 may be performed by a single analog-to-digital conversion module, which may employ a time division multiplex approach in which a single analog-to-digital converter is utilized to digitize voltage magnitudes of both current and voltage.

[0095] The method of Figure 6 may continue at 630, in which digital representations of sampled voltage and current magnitudes may be transformed to a frequency domain. In certain implementations, 630 may involve a use of a Fast Fourier Transform. In certain other implementations, 630 may involve use of a different transform, such as a Discrete Fourier Transform, for example. The method may continue at 640, which may involve combining frequency domain representations of current and voltage magnitudes to obtain RMS values of voltage and current. In some instances, combining of frequency domain representations of voltage and current magnitudes may involve computing such magnitudes substantially in accordance with expressions (3) and (4) to obtain I_{RMS} and V_{RMS} , described hereinabove.

[0096] The method may continue at 650, in which RMS values of voltage and current may be combined, such as substantially in accordance with expression (5) described hereinabove, to obtain forward power (P_{FWD}). The method may continue at 660, in which frequency domain representations of voltage and/or current magnitudes may be combined to obtain power delivered and/or a power factor that expresses a ratio of power delivered to a load (such as a process station) with respect to forward power. Computation of power factor may be conducted substantially in accordance with expression (6), described hereinabove.

[0097] In some embodiments, characteristics of RF voltage signals and/or RF current signals may be determined using one or more integrated circuits such as programmable logic devices or Application Specific Integrated Circuits (ASICs). Some implementations employ Field Programmable Gate Array (FPGA) integrated circuits. In some embodiments, an integrated circuit may be used to implement one or more blocks that calculate or determine: 1) voltage

and/or current magnitude; 2) voltage and/or current phase; 3) power characteristics associated with an input RF signal (e.g., a power factor, or the like); 4) a change in RF frequency; and/or 5) impedance characteristics.

5 [0098] In some embodiments, characteristics RF signals from multiple voltage and/or current sensors can be determined. For example, as shown in and described above in connection with Figure 2, each process chamber of semiconductor manufacturing equipment that includes multiple process chambers may be associated with a voltage sensor and/or a current sensor. Continuing with this example, in some embodiments, voltage and/or current signals from each sensor may be multiplexed such that the integrated circuit cycles through
10 samples from voltage and/or current sensors associated with each process chamber.

[0099] In some embodiments, blocks of an integrated circuit can determine characteristics of RF voltage signals and/or RF current signals by being programmed to: 1) down-convert RF voltage signals and/or RF current signals to determine real and imaginary parts of the RF voltage signals and/or RF current signals; 2) filter and down-sample the down-converted RF
15 voltage signals and/or RF current signals; and 3) determine magnitude and phase information corresponding to the real and imaginary parts of the RF voltage signals and/or RF current signals.

[0100] In some embodiments, the phase information of the RF voltage signals and/or RF current signals can be used to determine power characteristics. For example, a power factor
20 can be determined based on a comparison of the phase of an RF voltage signal to a phase of an RF current signal. As a more particular example, the power factor can be determined as the cosine of the difference between the phase of the RF voltage signal and the phase of the RF current signal.

[0101] In some embodiments, the phase of an RF voltage signal and/or the phase of an RF current signal can be used to determine a magnitude of a change of frequency of an RF signal.
25 For example, in some embodiments, the frequency of the RF signal can be determined as a derivative the phase of the RF voltage signal or the phase of the RF current signal.

[0102] Figure 7 is a block diagram illustrating components of a system for measurement of voltage and current parameters of an input RF signal using multiple voltage and current sensors,
30 according to an implementation.

[0103] Figure 7 illustrates a set of sensors 712. Set of sensors 712 includes RF voltage sensors and RF current sensors, as shown in and described above in connection with Figure 2.

Set of sensors 712 includes individual RF voltage sensor/RF current sensor pairs, such as RF voltage sensor/RF current sensor pair 714.

[0104] A set of amplifiers 702 receives RF voltage signals and RF current signals from the RF voltage sensor/RF current sensor pairs included in set of sensors 712. It should be understood that any suitable number of voltage and current sensors can be used. Similarly, a number of amplifiers that corresponds to a number of voltage and current sensors can be used. In some implementations, a number of RF voltage sensor/RF current sensor pairs may correspond to a number of process chambers in a multi-process chamber configuration, as shown in and described above in connection with Figures 1B and 2.

[0105] Each sensor in set of sensors 712 may include a connector that allows the sensor to connect to an amplifier in set of amplifiers 702. Examples of connectors include 7/16 DIN connectors, SQS connectors, and the like.

[0106] A multiplexer 704 receives RF voltage and current signals from set of amplifiers 702. Multiplexer 704, together with a buffer 706, can act as a switch that selects one pair of voltage and current signals from set of amplifiers 702 to be provided as input to an Analog-to-Digital Converter (ADC) 708. Multiplexer 704 may be configured to switch between the sensors included in set of sensors 712 at a multiplexing rate. Examples of a suitable multiplexing rate include 0.8 msec, 1 msec, 1.5 msec, or the like. The multiplexing rate may depend on a number of sensors in set of sensors 712 and on a desired data update rate. For example, in an instance in which a desired data update rate is 1 msec, and in which there are 5 sensors in set of sensors 712, the multiplexing rate is 1 msec/5 sensors, or 0.2 msec. In some implementations, the multiplexing rate may have a relationship with a signal to noise ratio. For example, the multiplexing rate may be lowered to sample each sensor for a longer duration of time, thereby increasing the signal to noise ratio. In some implementations, the multiplexing rate may be determined based on a current signal to noise ratio. For example, in some implementations, the multiplexing rate may be lowered in response to determining that a current signal to noise ratio is below a threshold. As another example, in some implementations, the multiplexing rate may be increased in response to determining that a current signal to noise ratio is above a threshold.

[0107] ADC 708 can generate digitized representations of the selected RF voltage and current signals. In some embodiments, ADC 708 can sample an input signal at a predetermined sampling frequency. Examples of sampling frequencies include 150 MHz, 200 MHz, 250 MHz, and the like. ADC 708 can provide the digitized representations to an integrated circuit 710. It should be noted that, in some embodiments, ADC 708 may be implemented as a portion

or region of code or circuitry of an integrated circuit (e.g., an ASIC, an FPGA, or the like). Such an integrated circuit may include additional other portions or additional other regions of code. For example, ADC 708 may be implemented as part of integrated circuit 710.

- [0108]** Integrated circuit 710 may be programmed to determine characteristics of the selected RF voltage and current signals, such as magnitude information, phase information, power characteristics, and the like. For example, integrated circuit 710 can be programmed to perform the method shown in and described below in connection with Figure 13. In some embodiments, integrated circuit 710 may include modules similar to the modules shown in and described below in connection with Figures 8-11.
- [0109]** In some embodiments, integrated circuit 710 may communicate with RF voltage sensors and/or RF current sensors included in set of sensors 712 via a communication block 716. Communication block 716 may be configured to implement a communication protocol to transmit information between sensors in set of sensors 712 and integrated circuit 710. An example communication protocol that may be used is the MAXIM ONE-WIRE protocol. In some embodiments, integrated circuit 710 may cause calibration information (e.g., calibration coefficients, or the like) to be stored in memory of individual RF voltage sensors and/or individual RF current sensors in set of sensors 710 via communication block 716. As another example, in some embodiments, individual RF voltage sensors and/or individual RF current sensors may be configured to provide identification information to integrated circuit 710 (e.g., at system turn-on, or other similar times). Examples of sensor identification information may include a sensor identifier (e.g., serial number, part number, etc.), a port location, a revision number, or the like. In some embodiments, integrated circuit 710 may be configured to verify that a particular RF voltage sensor or particular RF voltage sensor has not been erroneously used in the system by verifying the sensor identifier.
- [0110]** Outputs of integrated circuit 710 may be provided to various components or modules. For example, outputs of integrated circuit 710 may be provided to a second communication block 718. Second communication block 718 may be configured to implement a communication protocol that transmits data from integrated circuit 710 to various other devices. For example, communication block 718 may be configured to implement a serial communication protocol for transmitting data from integrated circuit 710 to one or more other devices via a serial interface. As a more particular example, in some embodiments, communication block 718 may be implemented as a Universal Asynchronous Receiver/Transmitter (UART) microchip.

[0111] Additionally or alternatively, outputs of integrated circuit 710 may be provided to Ethernet block 720 and/or Ethernet for Control Automation Technology (EtherCAT) block 722. In some embodiments, data provided from integrated circuit 710 to Ethernet block 720 and/or EtherCAT block 722 may be used as feedback to provide instructions to one or more elements (e.g., tuning elements) in a matching network. For example, instructions may be provided to a motion controller PCB. In some such embodiments, the motion controller PCB may control an RF match capacitor rotational position. For example, the RF match capacitor rotational position may be controlled based on RF impedance information determined by integrated circuit 710, power information determined by integrated circuit 710, or the like. It should be noted that feedback provided via EtherCAT block 722 may be provided at a sub-millisecond rate.

[0112] It should be noted that, in some embodiments, physical shields may be placed around RF voltage sensors and/or RF current sensors in set of sensors 712. Additionally or alternatively, in some embodiments, physical shields may be placed between RF voltage sensors and/or RF current sensors in set of sensors 712 and integrated circuit 710. Such shields may provide isolation and grounding. Accordingly, such shields may minimize potential electrical field interference on current measurement. Similarly, such shields may minimize potential magnetic field interference on voltage measurement. A physical shield may be a metal shield (e.g., substantially made of aluminum).

[0113] Figure 8 is a block diagram illustrating components of a system for measurement of RF voltage and current parameters, according to an implementation. In particular, Figure 8 illustrates modules of an integrated circuit that may be programmed to measure RF voltage and current parameters. It should be noted that, as used herein, “modules” of an integrated circuit refer to individual blocks of the integrated circuit that are each configured to perform various functions, such as down-conversion, decimation filtering, magnitude and phase determination, or the like. Each module may be specified using software code (e.g., in Hardware Definition Language (HDL)) or other logical representation of hardware elements. In some embodiments, the software code may be compiled. For example, functionality of a module within an FPGA may be configured based on the compiled software code. As implemented, a module of an FPGA or other programmable logic device or of a non-programmable logic device such as an application specific integrated circuit (ASIC, or a digital signal processors (DSP) is a collection of circuits having devices (e.g., transistors, memory elements, LUTs, etc.) and interconnects

between the devices. As illustrated, the integrated circuit may take, as inputs, an RF frequency signal 802, an RF voltage signal 804, and an RF current signal 806.

[0114] RF frequency signal 802 may be an RF frequency setting that substantially corresponds to a frequency of an RF signal generated by an RF signal generator. The RF signal
5 generator may be an RF signal generator that provides a high-power RF signal to a process chamber or a group of process chambers. In some embodiments, RF frequency signal 802 may track a frequency of the RF signal generated by the RF signal generator. For example, in an instance in which the RF signal generator operates at a variable frequency, RF frequency signal 802 tracks the variable frequency of the RF signal generator.

10 [0115] RF voltage signal 804 may be an output of an RF voltage sensor. RF current signal 806 may be an output of an RF current sensor.

[0116] RF frequency signal 802 and RF voltage signal 804 can be processed by a first branch 808. First branch 808 can generate, as outputs, a peak magnitude 810 of RF voltage signal 804 and a phase of RF voltage signal 804. In some embodiments, first branch 808 can include a
15 down-conversion module 824, one or more filtering and down-sampling modules (e.g., a real-part filtering and down-sampling module 826 and/or an imaginary-part filtering and down-sampling module 828), and/or a magnitude/phase determination module 830.

[0117] RF frequency signal 802 and RF current signal 806 can be processed by a second branch 812. Second branch 812 can generate, as outputs, a peak magnitude 814 of RF current
20 signal 806 and a phase of RF current signal 806. In some embodiments, second branch 812 can include a down-conversion module 832, one or more filtering and down-sampling modules (e.g., a real-part filtering and down-sampling module 834 and/or an imaginary-part filtering and down-sampling module 836), and/or a magnitude/phase determination module 838.

[0118] It should be noted that modules of first branch 808 may be similar to or substantially
25 the same as modules of second branch 812. More detailed schematic diagrams of a down-conversion module, a filtering and down-sampling module, and a magnitude/phase determination components are shown in Figures 9-11, respectively. Additionally, it should be noted that first branch 808 and second branch 812 may execute substantially in parallel.

[0119] A difference between the phase of RF voltage signal 804 and the phase of RF current
30 signal 806 may be determined at 816 to determine a phase difference 818.

[0120] The cosine of phase difference 818 may be determined at 820 to determine a power factor 822.

[0121] Figure 9 is a block diagram illustrating a down-conversion module for down-conversion of an RF voltage signal and/or an RF current signal, according to an implementation.

[0122] Note that the block diagram shown in Figure 9 may correspond to the down-conversion modules (e.g., down-conversion modules 824 and/or 832) shown in Figure 8.

[0123] As illustrated in Figure 9, a Numerically Controller Oscillator (NCO) 902 can be used as a Local Oscillator to frequency mix an RF signal input 906 (e.g., either an RF voltage signal or an RF current signal) from a carrier frequency to baseband. As illustrated, NCO 902 can take, as an input, an RF frequency setting 904, which is sometimes referred to herein as f_{NCO} .

In some embodiments, RF frequency setting 904 may be variable. In some embodiments, RF frequency 904 may be selected through software control based on a frequency band of interest. In some embodiments, RF frequency setting 904 may be set, modified, or adjusted based on a current estimate of a frequency of an RF signal generated by an RF signal generator, as shown in and described below in connection with Figure 12. That is, in some embodiments, RF frequency setting 904 may substantially track the frequency of the RF signal generated by the RF signal generator.

[0124] Down-conversion of RF signal input 906 may be a complex mix to baseband (e.g., mixing in quadrature). As illustrated in Figure 9, the down-conversion module can therefore generate a real part 908 and an imaginary part 910.

[0125] A down-converted RF signal (e.g., a down-converted RF voltage signal and/or a down-converted RF current signal) may have a lower bandwidth compared to the sampling rate. In some embodiments, the down-converted RF signal may be filtered to eliminate aliasing and then down-sampled to reduce the sampling rate. In some embodiments, a decimation filter is used to filter and down-sample the down-converted RF signal. In some embodiments, a decimation filter may be implemented in an integrated circuit using a Cascade Integrate Comb (CIC) filter.

[0126] Figure 10 is a block diagram illustrating a filtering and down-sampling module for down-sampling of an RF voltage signal and/or an RF current signal, according to an implementation. Note that the block diagram shown in Figure 10 may correspond to the filtering and down-sampling modules (e.g., filtering and down-sampling modules 826, 828, 834, and 846) as shown in Figure 8.

[0127] Figure 10 shows a block diagram for using CIC filtering to filter and down-sample an input signal 1002 (e.g., a down-converted RF voltage signal or a down-converted RF current signal) to generate a down-sampled output signal 1004.

[0128] A magnitude and/or phase of a down-sampled signal may be determined (e.g., a magnitude and/or a phase of a down-sampled RF voltage signal, a magnitude and/or phase of a down-sampled RF current signal, and the like). In some embodiments, the magnitude and/or phase of the RF signal may be determined from real and imaginary parts of the down-sampled RF signal using Volder's algorithm. In some embodiments, Volder's algorithm may be implemented in an integrated circuit using Coordinate Rotation Digital Computer (CORDIC).

[0129] Figure 11 shows a block diagram for determining amplitude and phase of an RF input signal based on real and imaginary parts of the RF input signal.

[0130] Real part 1102 and imaginary part 1104 may correspond to down-sampled real and imaginary parts of an RF input signal. For example, referring to Figure 8, real part 1102 may correspond to an output of filtering and down-sampling module 826 (e.g., in an instance in which the RF signal is an RF voltage signal). As another example, real part 1102 may correspond to an output of filtering and down-sampling module 834 (e.g., in an instance in which the RF signal is an RF current signal). As yet another example, imaginary part 1104 may correspond to an output of filtering and down-sampling module 828 (e.g., in an instance in which the RF signal is an RF voltage signal). As still another example, imaginary part 1104 may correspond to an output of filtering and down-sampling module 836 (e.g., in an instance in which the RF signal is an RF current signal).

[0131] Real part 1102 and imaginary part 1104 may be combined at 1106 to a complex representation. The complex representation may then be used to determine a magnitude 1108 and/or a phase 1110 of the RF signal using CORDIC. In some embodiments, CORDIC may be implemented at 1112 using Hardware Description Language (HDL).

[0132] To mix an RF voltage signal and/or an RF current signal to baseband, the RF voltage signal and/or the RF current signal is mixed with sine and cosine waveforms with frequencies that correspond to the frequency of the input RF signal (e.g., the RF signal generated by an RF signal generator that provides high-power RF signals to one or more process chambers). The sine and cosine waveforms may be generated by an NCO that acts as a Local Oscillator. The frequency of the sine and cosine waveforms is generally referred to as f_{NCO} herein.

[0133] In some instances, the frequency of the RF signal generated by an RF signal generator may vary over time. For example, an RF signal generator operating in a tuning mode may have

an instantaneous frequency that varies over time. For example, an RF signal generator may be set to provide an RF frequency of 13.56 MHz, 27.12 MHz, or the like. However, the RF signal generated by the RF signal generator may have an instantaneous frequency that varies from the set (i.e., expected) RF frequency. Mixing an RF voltage signal or an RF current signal with sine and cosine waveforms having the set RF frequency rather than the actual RF frequency may result in frequency errors at baseband. The frequency errors may lead to voltage and/or current measurement errors. Accordingly, it is desirable to generate sine and cosine waveforms that have frequencies that track the instantaneous RF frequency of the RF signal generated by the RF signal generator. Tracking and updating the RF signal frequency may provide more accurate calculation of RF characteristics, such as magnitude and/or phase, power factor, and the like.

[0134] In some embodiments, the systems and methods described herein allow the sine and cosine waveforms generated by the NCO to track the actual RF frequency of the RF signal generated by the RF signal generator. For example, in some embodiments, the frequency of the RF signal may be determined and/or tracked. Continuing with this example, in some embodiments, the determined RF frequency may be provided to the NCO to generate sine and cosine waveforms for down-converting RF voltage signals and/or RF current sensors using the determined RF frequency.

[0135] In some embodiments, the frequency of the RF signal may be iteratively updated based on a phase of the RF voltage signal or the phase of the RF current signal. For example, in some embodiments, the frequency may be determined as the derivative of the phase as a function of time. An example of an equation to determine the frequency of the RF signal is:

$$f = \frac{d\theta}{dt} \quad (7)$$

[0136] It should be noted that, in some embodiments, other techniques may be used to determine and/or iteratively update the frequency of the RF signal, such as a digital phase-locked loop (PLL), a Fourier analysis, and the like.

[0137] In some embodiments, a change in estimated frequency of an RF signal between two successive time points may be compared to a threshold. In an instance in which the change exceeds the threshold, RF voltage sensor samples and/or RF current sensor samples may be discarded due to inaccuracy.

[0138] Figure 12 shows a block diagram illustrating a process for determining magnitude, phase, and power characteristics of RF current and RF voltage signals, according to an implementation.

[0139] As illustrated, an input corresponding to an RF voltage signal and/or an RF current signal is obtained at 1202. The RF voltage signal and/or the RF current signal may be conditioned in any manner, as described above in connection with Figure 7.

[0140] At 1204, the RF voltage signal and/or the RF current signal are mixed to baseband.

5 The mix to baseband uses sine and cosine waveforms generated at 1206 using an NCO that acts as a Local Oscillator operating at a frequency f_{NCO} . The RF voltage signal and/or the RF current signal that have been mixed to baseband are sometimes referred to herein as a down-converted RF voltage signal and/or a down-converted RF current signal, respectively.

[0141] At 1208, the down-converted RF voltage signal and/or the down-converted RF
10 current signal are down-sampled. Magnitude and/or phase information is derived. For example, as shown in Figure 12, filtering and down-sampling may be performed using a decimation filter (e.g., using a CIC filter). Undesired signals (e.g., noise, or other undesired signals) may be rejected using a narrowband Frequency Impulse Response (FIR) filter. The passband width of the narrowband CIC filter may be 200 kHz, 400 kHz, or the like. The center
15 frequency of the CIC filter may be set based on a tracked frequency determined at block 1214, as described below. Magnitude characteristics, phase characteristics, and/or frequency characteristics may be derived using CORDIC to generate outputs 1210.

[0142] At 1212, the down-converted RF voltage signal and/or the down-converted RF current signal may be applied to a branch parallel to the branch at 1208. As illustrated, the
20 down-converted RF voltage signal and/or the down-converted RF current signal may be filtered using a wide FIR filter. The passband width of the wide FIR filter may be, e.g., +/- 5% of the center frequency, +/- 8% of the center frequency, or the like. The center frequency may correspond to a set frequency of the RF signal generator. Magnitude and phase information may then be derived using CORDIC.

25 [0143] At 1214, an estimate of the current frequency of the RF signal is determined using the derivative of the phase of the RF voltage signal or the phase of the RF current signal.

[0144] In some implementations, the estimate of the current frequency is used to set a center frequency of the narrowband FIR filter shown in and described above in connection with block 1208. That is, in some implementations, the wide FIR filter shown in and described above in
30 connection with block 1212 is used to estimate the current frequency of the RF signal. The estimate of the current frequency of the RF signal is used to configure the narrowband FIR filter shown in and described above in connection with block 1208. The configured

narrowband FIR filter is then used to determine the voltage/current characteristics, the power characteristics, etc. at block 1210.

[0145] At 1216 and 1218, the estimate of the current frequency is integrated over multiple samples obtained at different time points.

- 5 [0146] At 1220, a difference between the frequency estimate and a reference frequency (indicated in Figure 12 as “Ref LO”) is determined. The difference between the frequency estimate and the reference frequency may then be used to adjust f_{NCO} at 1206.

- [0147] The speed at which the feedback loop adjusts to changes in frequency is determined by the loop gain, which is indicated as “Loop K” in Figure 12. Higher values of K may cause
10 a faster response to changes in instantaneous frequency. However, higher values of K may cause an increase in noise and/or a higher likelihood of instability. Conversely, lower values of K may cause a slower response to changes in frequency. However, lower values of K may yield less noise in voltage and/or current measurements.

- [0148] In some embodiments, the estimate of the current frequency is compared at 1222 to
15 a threshold (indicated in Figure 12 as “blinking threshold”). In response to determining that the current frequency exceeds the threshold, a black-out timer may be applied at 1224. For example, in some embodiments, measurement of RF voltage signals and/or RF current signals may be paused for a predetermined duration of time. In other words, measurements of RF voltage signals and/or RF current signals may be paused when a frequency of the RF signal is
20 changing at a rate that exceeds a threshold.

[0149] Figure 13 is a flowchart for a method 1300 of determining magnitude, phase, and power characteristics of RF current and RF voltage signals, according to an implementation.

- [0150] At 1310, method 1300 obtains RF voltage signal samples and RF current signal samples. The RF voltage signal samples and RF current signal samples may be samples from
25 a voltage sensor and/or a current sensor, as shown in and described above. In some embodiments, the RF voltage signal samples and/or RF current signal samples may be conditioned.

- [0151] At 1320, method 1300 down-converts the RF voltage signal and the RF current signal to baseband. Down-conversion may be performed using a complex mix to baseband. That is,
30 the down-converted RF voltage signal and the down-converted RF current signal may be represented as having imaginary and real parts. The mixing waveforms may be sine and cosine waveforms generated using an NCO that acts as a Local Oscillator operating at a frequency f_{NCO} . The frequency f_{NCO} may be updated or adjusted to substantially track the actual frequency

of an RF signal generated by an RF signal generator. An example schematic diagram for down-converting the RF voltage signal and/or the RF current signal is shown in and described above in connection with Figure 9.

5 [0152] At 1330, method 1300 filters and reduces the sampling rate of the down-converted RF voltage signal and the down-converted RF current signal. For example, the down-converted RF voltage signal and the down-converted RF current signal may be filtered and down-sampled using decimation filtering. In some embodiments, decimation filtering may be applied using a CIC filter. An example schematic diagram for reducing the sampling rate of an RF voltage signal and/or an RF current signal is shown in and described above in connection with Figure
10 10.

[0153] At 1340, method 1300 determines magnitude and phase information for each of the RF voltage signal and the RF current signal based on the imaginary and real parts of the down-sampled, down-converted signal. Magnitude and phase information may be determined from imaginary and real parts of the signal using Volder's algorithm. In some embodiments,
15 Volder's algorithm may be implemented using CORDIC. An example schematic diagram for using CORDIC to determine magnitude and phase information of an RF voltage signal and/or an RF current signal is shown in and described above in connection with Figure 11. In some embodiments, the magnitude of the RF voltage signal may be considered the peak voltage. In some embodiments, the magnitude of the RF current signal may be considered the peak current.

20 [0154] It should be noted that, in some embodiments, an impedance associated with an input RF signal may be determined based on the magnitude of the RF voltage signal and the magnitude of the RF current signal. For example, in some embodiments, the impedance may be determined as the ratio of the magnitude of the RF voltage signal to the magnitude of the RF current signal.

25 [0155] At 1350, method 1300 determines a power factor based on the difference between the phase of the RF voltage signal and the phase of the RF current signal. For example, the power factor may be determined as the cosine of the phase difference. The power factor may express a ratio of power delivered to a load (such as a process station) with respect to forward power.

30 [0156] At 1360, method 1300 obtains a current estimate of the RF signal frequency (e.g., the RF signal frequency generated by an RF signal generator) based on the RF voltage signal phase or the RF current signal phase. For example, the current RF signal frequency may be estimated based on a derivative of the phase.

[0157] The method may then loop back to 1310. Method 1300 may then obtain updated RF voltage signal samples and updated RF current signal samples. The current estimate of the RF signal frequency may be used to down-convert the RF voltage signal and/or the RF current signal at 1320. It should be noted that, in instances in which multiple voltage sensors and/or multiple current sensors are used (e.g., a different voltage/current sensor pair for each process chamber in a multi-process-chamber piece of equipment), at 1310, the method may obtain RF voltage signal samples and/or RF current signal samples from a different voltage sensor and current sensor.

[0158] A system that includes one or more RF voltage sensors and/or RF current sensors coupled to a controller for analyzing outputs of the RF voltage sensors and/or RF current sensors may be calibrated using various techniques. Calibration may be performed to generate calibration coefficients that transform raw RF voltage sensor measurements and/or raw RF current sensor measurements to controller outputs. Calibration coefficients may be dependent on characteristics of an RF voltage sensor and/or an RF current sensors, characteristics of cables used to couple a sensor to a controller (e.g., cable length, cable thickness, etc.), input characteristics at the controller, and the like. In some embodiments, calibration coefficients may be stored in memory (e.g., EEPROM) of a sensor and/or in memory associated with a controller. In some embodiments, by storing calibration coefficients in sensor memory, sensors may be swapped without having to re-calibrate the entire system. For example, calibration coefficients may be read from the sensory memory in response to detecting a change in power status (e.g., power on, system reset, or the like) of the system or apparatus. It should be noted that “controller,” as used in connection with Figures 14A, 14B, 15A, and 15B refers to a system that receives RF voltage sensor and/or RF current sensor measurements as inputs. The system may include one or more amplifiers, a buffer, a multiplexer, an ADC, an integrated circuit to determine voltage, current, and/or power characteristics. For example, a controller may include 702, 704, 706, 708, 710, 716, 718, 720, and/or 722 of Figure 7.

[0159] It should be noted that calibration may be performed at one or more RF frequencies. In some embodiments, calibration coefficients may be determined for each calibration frequency. In some such embodiments, calibration coefficients may be stored (e.g., in memory of RF voltage sensors and/or memory of RF current sensors) for each calibration frequency. Example calibration frequencies include 0.4 MHz, 13.56 MHz, 27.12 MHz, and the like.

[0160] In some embodiments, calibration may be performed modularly. For example, as shown in and described below in connection with Figures 14A and 15A, calibration coefficients

associated with a sensor may be determined. For example, the calibration coefficients may be based on S-parameters from a vector network analyzer that characterize a sensor circuit. In some embodiments, calibration coefficients associated with sensor(s) may be stored in memory of the sensor(s). Continuing with this example, transformation coefficients that transform

5 sensor outputs to a controller input may be determined. The transformation coefficients may be determined based on calibration coefficients associated with the sensors, cable characteristics that couple the sensors to the controller (e.g., cable length, cable impedance, and the like), etc. In some embodiments, the transformation coefficients may be stored in memory associated with the controller. In some such embodiments, transformation coefficients

10 stored in memory of the controller may be associated with an identifier of a cable (e.g., a cable model number or part number), thereby allowing transformation coefficients associated with a particular cable to be retrieved from memory associated with the controller. An identifier of a cable may indicate cable characteristics, such as length. In some embodiments, a cable may be a “smart” cable. In some such embodiments, an identifier of a cable may indicate a Federal

15 Communication Commission (FCC) identifier, an identifier of an embedded chip of the smart cable, or the like.

[0161] Additionally or alternatively, in some embodiments, calibration may be performed end-to-end such that the entire system is calibrated at once, as shown in and described below in connection with Figures 14B and 15B.

20 **[0162]** Figure 14A shows a schematic diagram for modular calibration of a system for determining magnitude, phase, and power characteristics of RF current and RF voltage signals, according to an implementation. Calibration may be performed to calibrate one or more sensors (e.g., one or more RF voltage sensors and/or one or more RF current sensors) of a sensor circuit 1404 that provide RF voltage and/or RF current inputs to a controller 1416.

25 **[0163]** As illustrated, an RF input signal 1402 may be input to a system that includes sensor circuit 1404. RF input signal 1402 may be an RF input signal generated by an RF signal generator, such as RF signal generator 114 of Figure 1A. The sensor circuit may include an RF voltage sensor 1406 and/or an RF current sensor 1408. A load 1410 may be coupled to measure characteristics of sensor circuit 1404. Load 1410 may be a known load. Examples of

30 load 1410 include a 50 Ω resistance, a 100 Ω resistance, or the like.

[0164] At step 1 of Figure 14A, RF voltage sensor 1406 and RF current sensor 1408 may be calibrated. It should be noted that Figure 14A illustrates a schematic diagram of a system, as well as steps (depicted by the numerals 1-4) of a method for calibrating the system.

- [0165] In some embodiments, a two-port Vector network analyzer may be used to characterize response characteristics of the sensor circuit. Example two-port Vector network analyzers include the Keysight E5061B, the Keysight E5063A, or the like. The Vector network analyzer may be used to determine S-parameters (e.g., S21, S31, S41, and the like). The S-parameters may be used to determine outputs of RF voltage sensor 1406 and RF current sensor 1408 (denoted herein as V1 and I1). For example, V1 and I1 may be determined based on S31 and S41, respectively. In some embodiments, the S-parameters may be used to determine voltage and current components of the RF input signal 1402 (denoted herein as V2 and I2). For example, V2 and I2 may be determined based on S21 and a known value of load 1410. It should be noted that additional loads may be used to determine the transformation coefficients through fitting, in some embodiments. In some embodiments, a two-port Vector network analyzer may be used in multiple steps. For example, V1 may be determined based on S31 in a first step. Continuing with this example, I1 may be determined based on S41 in a second step.
- [0166] In some embodiments, an impedance of the DUT may be determined using an open-short-load paradigm. For example, the corrected impedance of the DUT, referred to herein as Z_{DUT} , may be determined as:

$$Z_{DUT} = \frac{(Z_s - Z_{xm})(Z_{sm} - Z_o)}{(Z_{xm} - Z_o)(Z_s - Z_{sm})} Z_{std} \quad (8)$$

- [0167] In equation (8) above, Z_o represents the measured open-circuit impedance, Z_s represents the measured impedance under short circuit conditions, Z_{sm} represents the measured impedance value of the known load, Z_{std} represents the true (or expected) impedance value of the known load (e.g., 50 Ω), Z_{xm} represents a measured impedance value of the DUT, and Z_{DUT} represents a corrected impedance value of the sensor circuit. Values of Z_o , Z_s , Z_{sm} , and Z_{std} , may be calculated based on the S-parameters.
- [0168] The S-parameters can characterize the RF voltage sensor and/or the RF current sensor. In particular, the S-parameters can provide a transformation from an input voltage (e.g., from an RF signal generator) to the RF voltage produced by the RF voltage sensor. The S-parameters can similarly characterize the RF current sensor.
- [0169] In some embodiments, the values of the calibration coefficients stored in memory of the RF voltage sensor and/or the RF current sensor may correspond to the values of Z_o , Z_s , Z_{sm} , and Z_{std} calculated based on the S-parameters. For example, in some embodiments, the calibration coefficients may be stored in memory (e.g., EEPROM) of RF voltage sensor 1406 and/or RF current sensor 1408. These calibration coefficients may be retrieved at a later time

(e.g., upon detection of an RF voltage sensor 1406 and/or RF current sensor 1408) such that various sensors can be swapped without having to recalibrate the entire system.

[0170] At step 2 of Figure 14A, a transformation function can be determined that transforms the output value of RF voltage sensor 1406 to an input voltage value at controller 1416.

5 Similarly, a transformation function can be determined that transforms the output value of RF current sensor 1408 to an input current value at controller 1416. Each transformation function may be determined based on various characteristics associated with the system. Examples of such characteristics may include characteristics of cables (e.g., cables 1412 and 1414) that couple RF voltage sensor 1406 and/or RF current sensor 1408 to controller 1416, an input
10 impedance to controller 1416, a combination impedance that represents cable impedance and the input impedance to controller 1416, and the like. Example cable characteristics can include cable length, cable impedance, cable radius, cable material, and the like. In some embodiments, transformation coefficients associated with the transformation function(s) may be stored in memory (e.g., EEPROM) associated with the controller. Additionally or
15 alternatively, in some embodiments, transformation coefficients associated with the transformation function(s) may be stored in memory associated with the cables that couple the RF voltage sensor and/or the RF current sensor to the controller.

[0171] At step 3 of Figure 14A, a transformation function can be determined that transforms the input voltage value at controller 1416 to a raw output voltage value generated by controller

20 1416. Similarly, a transformation function can be determined that transforms the input current value at controller 1416 to a raw output current value generated by controller 1416. In some embodiments, the transformation function(s) may be determined using a dual output function generator that inputs a signal into controller 1416 to determine a scaling factor and/or a phase shift associated with the transformation function(s). In some embodiments, transformation
25 coefficients that relate the input voltage value at controller 1416 to the raw output voltage value generated by controller 1416 and/or that relate the input current value at controller 1416 to the raw output current value generated by controller 1416 can be stored in memory associated with the controller.

[0172] At step 4 of Figure 14A, the calibration coefficients associated with the RF voltage sensor and/or the RF current sensor, the transformation function(s) that transform sensor output
30 to controller input, and the transformation function(s) that transform controller input to controller output can be combined to generate overall system transformation function(s). In

some embodiments, transformation coefficients that represent the overall system transformation function(s) can be stored in memory associated with the controller.

[0173] Turning to Figure 15A, an example flowchart for a method 1500 for performing modular calibration is shown, according to an implementation. It should be noted that blocks 1510 and 1520 of method 1500 relate to step 1 of Figure 14A, block 1530 of method 1500 relates to step 2 of Figure 14A, and block 1540 relates to step 3 of Figure 14A.

[0174] At 1510, method 1500 obtains measurements associated with a sensor circuit that includes one or more RF voltage sensors and/or one or more RF current sensors. In some embodiments, the measurements may be obtained using a Vector network analyzer. In some embodiments, the measurements may be made using an open-short-load paradigm. For example, in some embodiments, the measurements may be obtained under three different conditions: 1) an open circuit condition; 2) a short circuit condition; and 3) a known load condition. The known load may be, for example, a 50 Ω resistance, a 100 Ω resistance, or the like. In some embodiments, the known load condition may be repeated with multiple different known loads.

[0175] At 1520, method 1500 determines calibration coefficients associated with the one or more RF voltage sensors and/or the one or more RF current sensors based on the measurements. For example, in some embodiments, the calibration coefficients can be determined based on network characteristics generated by a network analyzer, such as S-parameters, Z-parameters, H-parameters, or the like.

[0176] At 1530, method 1500 determines one or more transformation functions that transform outputs of the RF voltage sensor(s) to an input voltage at a controller and that transforms outputs of the RF current sensor(s) to an input current at the controller. The transformation function(s) may be based on various characteristics, such as an input impedance of the controller, cable characteristics (e.g., a cable length, a cable impedance, a cable material, and the like), a combination of an input impedance of the controller and a cable impedance, and the like.

[0177] At 1540, method 1500 determines one or more transformation functions that transform an input voltage at the controller to a digitized output of the controller and that transforms an input current at the controller to a digitized output of the controller. The one or more transformation functions may be determined using a function generator (e.g., a dual output function generator). For example, the function generator may input a signal into the controller, and a scaling factor and/or a phase shift associated with the output signal may be

measured. Continuing with this example, in some embodiments, the transformation function(s) may be determined based on the scaling factor and/or the phase shift.

- [0178]** At 1550, method 1500 may store parameters associated with the calibration coefficients and/or the transformation function(s) in memory associated with the RF voltage sensor(s), the RF current sensor(s), and/or in memory associated with the controller. For example, in some embodiments, calibration coefficients associated with the RF voltage sensor(s) and/or the RF current sensor(s) that are determined based on parameters generated by a network analyzer (e.g., S-parameters, Z-parameters, H-parameters, or the like) may be stored. Such calibration coefficients may be stored in memory (e.g., EEPROM memory) of the RF voltage sensor(s) and/or the RF current sensor(s). As another example, in some embodiments, coefficients and/or polynomial values associated with the transformation function(s) (e.g., the transformation functions determined at blocks 1530 and/or 1540) may be stored. Method 1500 may store the parameters associated with the transformation functions in memory associated with the controller.
- [0179]** Figure 14B shows a schematic diagram for end-to-end calibration of a system for determining magnitude, phase, and power characteristics of RF current and RF voltage signals, according to an implementation. Calibration may be performed to calibrate one or more sensors (e.g., one or more RF voltage sensors and/or one or more RF current sensors) of sensor circuit 1404 that provide RF voltage and/or RF current inputs to controller 1416.
- [0180]** As illustrated, an RF input signal 1402 may be provided to a matching network 1452. In some embodiments, RF input signal may be an RF signal generator, such as RF signal generator 114 of Figure 1A. In some embodiments, matching network 1452 may be a matching network such as matching network 116 of Figure 1A that performs impedance matching from the RF signal generator that generates RF input signal 1402 to sensor circuit 1404.
- [0181]** System characteristics may be measured based on RF input signal 1402 with various loads simulated by a load simulator 1454. The system characteristics may be measured by independent RF sensors 1456. Independent RF sensors 1456 may have known characteristics. Measurements from an RF voltage sensor and/or an RF current sensor may therefore be compared with measurements from independent RF sensors 1456. Independent RF sensors 1456 may serve to monitor drift in the calibration system. In some embodiments, independent RF sensors 1456 may be commercially available.
- [0182]** Load simulator 1454 may simulate various known loads. In some embodiments, one or more loads simulated by load simulator 1454 may be a high-phase load. Examples of high-

phase loads include loads that are substantially capacitive and/or substantially inductive. In some embodiments, load simulator 1454 may additionally or alternatively simulate a substantially resistive load, such as a 50 Ω load, a 100 Ω load, or the like.

5 [0183] In some embodiments, power characteristics can be measured for the loads simulated by load simulator 1454 using RF input signal 1402. It should be noted that, by using one or more high-phase loads, the system can be calibrated across a span of possible phases of an RF voltage sensor and/or an RF current sensor. By calibrating across the span of possible phases, power characteristics determined by the system may be more accurate.

10 [0184] One or more transfer functions that relate input voltage to the sensor circuit and input current to the sensor circuit to a digitized outputs of controller 1416 (e.g., indicating raw voltage and current measurements) and that relate a phase of input to the sensor circuit to a digitized output of controller 1418 (e.g., indicating raw phase measurements) can be determined based on the system characteristics measured for various known loads generated by load simulator 1454 and as measured by independent RF sensors 1456.

15 [0185] Turning to Figure 15B, an example flowchart for a method 1560 for performing end-to-end calibration is shown, according to an implementation.

[0186] At 1570, method 1560 can obtain measurements associated with a sensor circuit that includes one or more RF voltage sensors and/or one or more RF current sensors. The RF voltage sensor(s) and the RF current sensor(s) may be coupled to a controller via one or more
20 cables, as shown in Figure 14B.

[0187] As shown in Figure 14B, the measurements may be obtained using one or more independent RF sensors. Additionally, as shown in Figure 14B, the measurements may be made with respect to a known load generated by a load simulator. For example, voltage may be measured across the known load. As another example, current may be measured through
25 the known load. In some embodiments, the known load may include one or more high-phase loads. It should be noted that measurements may be obtained with any suitable number of loads (e.g., one, two, five, ten, or the like).

[0188] At 1580, method 1560 can determine one or more transformation function(s). The one or more transformation function(s) can relate: 1) the voltage at the RF voltage sensor(s) and a current going through the RF current sensor(s) to digitized outputs of the controller that
30 represent raw voltage and/or current measurements, respectively; and/or 2) the phase of the input at the RF voltage sensor and/or the phase of the current going through the RF current sensor(s) to digitized phase outputs of the controller..

[0189] The one or more transformation function(s) may be determined based on characteristics of signals measured by the independent RF sensors across the known load(s). For example, the one or more transformation function(s) may be determined based on voltages measured across the known load(s), currents measured through the known load(s), phases of
5 measured voltage or current signals, power at the known load(s), and/or any combination thereof.

[0190] At 1590, method 1560 can store parameters associated with the transformation function(s) in memory associated with the controller. .

[0191] In some embodiments, measurements from one or more RF voltage sensors and/or
10 one or more RF current sensors can be used to identify problems of an associated process chamber. For example, in some embodiments, the measurements may be analyzed to determine if there are any characteristics of the RF energy that may negatively impact deposition during a process (e.g., excessive particles, non-uniformity in deposition, or the like).

[0192] In some embodiments, a frequency domain representation of samples from one or
15 more RF voltage sensors and/or one or more RF current sensors may be analyzed to identify anomalies that correspond to or correlate with particular trigger events. In some embodiments, the frequency domain representation may be determined by calculating an FFT of the RF voltage sensor samples and/or the RF current sensor samples.

[0193] In some embodiments, samples from the RF voltage sensor(s) and/or the RF current
20 sensor(s) may be obtained and/or analyzed in response to detection of a trigger event. Examples of such a trigger event include when an RF signal generator is first turned on, when a measured RF voltage exceeds a predetermined threshold, when a measured RF current exceeds a predetermined threshold, when a power setpoint changes, when a process step or condition changes, and the like. It should be noted that, in some embodiments, multiple trigger
25 events can be specified.

[0194] Examples of anomalies that may be detected in a frequency domain representation of samples of an RF voltage sensor and/or samples of an RF current sensor include energy at particular harmonics of the RF signal frequency exceeding a predetermined threshold, energy at particular inter-modulation products exceeding a threshold that indicate particular RF and
30 plasma chamber interactions, or the like. In some embodiments, an indication of an identified anomaly can be stored or presented in various ways. For example, in some embodiments, information associated with an identified anomaly (e.g., an indication of the RF frequency associated with the anomaly, timestamp information, or the like) may be stored in a log. As

another example, in some embodiments, information associated with an identified anomaly may be presented in a user interface, e.g., to a process engineer.

[0195] Figure 16 shows an example flowchart for a method 1600 for identifying anomalous characteristics of RF signals associated with a process chamber or group of process chambers, according to an implementation.

[0196] At 1610, method 1600 obtains indications of one or more trigger events. As described above, the one or more events can include an RF signal generator being turned on or activated, a measured RF voltage (e.g., measured by an RF voltage sensor associated with a process chamber) exceeding a predetermined threshold, a measured RF current (e.g., measured by an RF current sensor associated with a process chamber) exceeding a predetermined threshold, or the like.

[0197] Method 1600 may obtain the indications of the one or more trigger events, for example, from a file that specifies the one or more trigger events. Such a file may be configured by a process engineer or other person charged with maintenance of the process chamber.

[0198] At 1620, method 1600 detects occurrence of a trigger event of the one or more trigger events. In some embodiments, the trigger event may be detected based on samples from a particular RF voltage sensor or a particular RF current sensor associated with the process chamber.

[0199] At 1630, in response to detecting occurrence of the trigger event, method 1600 obtains samples of RF voltage signals and RF current signals for further analysis. The sampling frequency may be 150 Mhz, 200 Mhz, 250 Mhz, or the like. In some embodiments, method 1600 may obtain samples for a predetermined duration of time after a time point of the trigger event or may obtain a predetermined number of samples after a time point of the trigger event. The duration of time over which samples are obtained may be within a range of 5 msec – 1 sec.

For example, samples may be obtained for 10 msec, 50 msec, 500 msec, 1 sec, or the like.

[0200] At 1640, method 1600 determines frequency domain representations of the samples of the RF voltage signals and/or the samples of the RF current signals. In some embodiments, the frequency domain representations may be determined by calculating an FFT of the sampled RF voltage signals and/or the sampled RF current signals.

[0201] At 1650, method 1600 may identify an anomaly in the frequency domain representation of the RF voltage signals and/or the frequency domain representation of the RF current signals. For example, the anomaly may correspond to energy in a particular frequency band exceeding a predetermined threshold. In some embodiments, the frequency band may

correspond to a particular harmonic (e.g., a second harmonic, or the like) of the RF frequency, a frequency associated with inter-modulation products that indicate a resonance frequency of the system, or the like.

5 [0202] At 1660, method 1600 may present or store information indicating the detected anomaly. The information may include a frequency band associated with the anomaly, an energy in the frequency band associated with the anomaly, timestamp information indicating a time at which the anomaly was detected, and the like. In some embodiments, method 1600 may cause the information indicating the anomaly to be stored in a log that can later be accessed. Additionally or alternatively, in some embodiments, method 1600 may cause
10 information indicating the anomaly to be presented, for example, in a user interface.

[0203] More generally, in many instances, manufacture of semiconductor devices can involve depositing or etching of one or more thin films on or over a planar or non-planar substrate in an integrated fabrication process. In some aspects of an integrated process, it may be useful to deposit thin films that conform to unique substrate topography. As previously
15 mentioned herein, one type of reaction that is useful in many instances may involve chemical vapor deposition (CVD). In typical CVD processes, gas phase reactants introduced into stations of a reaction chamber simultaneously undergo a gas-phase reaction. The products of the gas-phase reaction deposit on the surface of the substrate. Also as previously described, a reaction of this type may be driven by, or enhanced by, presence of a plasma, in which case the
20 process may be referred to as a plasma-enhanced chemical vapor deposition (PECVD) reaction. As used herein, the term CVD is intended to include PECVD unless otherwise indicated. CVD processes have certain characteristics that render them less appropriate in some contexts. For instance, mass transport limitations of CVD gas phase reactions may bring about deposition effects that exhibit thicker deposition at top surfaces (e.g., top surfaces of gate stacks) and thinner deposition at recessed surfaces (e.g., bottom corners of gate stacks). Further, in
25 response to some semiconductor die having regions of differing device density, mass transport effects across the substrate surface may result in within-die and within-wafer thickness variations. Thus, during subsequent etching processes, thickness variations can result in over-etching of some regions and under-etching of other regions, which can degrade device
30 performance and die yield. Another difficulty related to CVD processes is that such processes are often unable to deposit conformal films in high aspect ratio features. This issue can be increasingly problematic as device dimensions continue to shrink.

[0204] In another example, some deposition processes involve multiple film deposition cycles, each producing a discrete film thickness. For example, in ALD, thickness of a deposited layer may be limited by an amount of one or more film precursor reactants, which may adsorb onto a substrate surface, so as to form an adsorption-limited layer, prior to the film-forming chemical reaction itself. Thus, a feature of ALD involves the formation of thin layers of film, such as layers having a width of a single atom or molecule, which are used in a repeating and sequential manner. As device and feature sizes continue to be reduced in scale, and as three-dimensional devices and structures become more prevalent in integrated circuit (IC) design, the capability of depositing thin conformal films (e.g., films of material having a uniform thickness relative to the shape of the underlying structure) continues to gain in importance. Thus, in view of ALD being a film-forming technique in which each deposition cycle operates to deposit a single atomic or molecular layer of material, ALD may be well suited to the deposition of conformal films. Typical device fabrication processes involving ALD may include multiple ALD cycles, which may number into the hundreds or thousands, may then be utilized to form films of virtually any desired thickness. Further, in view of each layer being thin and conformal, a film that results from such a process may conform to a shape of any underlying device structure. In certain implementations, an ALD cycle may include the following steps:

- [0205] Exposure of the substrate surface to a first precursor.
- [0206] Purge of the reaction chamber in which the substrate is located.
- [0207] Activation of a reaction of the substrate surface, typically with a plasma and/or a second precursor.
- [0208] Purge of the reaction chamber in which the substrate is located.
- [0209] The duration of each ALD cycle may typically be less than about 25 seconds or less than about 10 seconds or less than about 5 seconds. The plasma exposure step (or steps) of the ALD cycle may be of a short duration, such as a duration of about 1 second or less.
- [0210] In particular implementations, ALD operations may be controlled and/or managed by system controller 190 (of Figure 1B), which may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality

of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus, as described above, the controller may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0211] In the foregoing detailed description, numerous specific details are set forth to provide a thorough understanding of the presented embodiments or implementations. The disclosed embodiments or implementations may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail so as to not unnecessarily obscure the disclosed embodiments or implementations. While the disclosed embodiments or implementations are described in conjunction with the specific embodiments or implementations, it will be understood that such description is not intended to limit the disclosed embodiments or implementations.

[0212] The detailed description is directed to certain embodiments or implementations for the purposes of describing the disclosed aspects. However, the teachings herein can be applied and implemented in a multitude of different ways. In the foregoing detailed description, references are made to the accompanying drawings. Although the disclosed embodiments or implementation are described in sufficient detail to enable one skilled in the art to practice the embodiments or implementation, it is to be understood that these examples are not limiting; other embodiments or implementation may be used and changes may be made to the disclosed embodiments or implementation without departing from their spirit and scope. Additionally, it should be understood that the conjunction “or” is intended herein in the inclusive sense where appropriate unless otherwise indicated; for example, the phrase “A, B, or C” is intended to

include the possibilities of “A,” “B,” “C,” “A and B,” “B and C,” “A and C,” and “A, B, and C.”

5 [0213] In this application, the terms “semiconductor wafer,” “wafer,” “substrate,” “wafer substrate,” and “partially fabricated integrated circuit” are used interchangeably. One of ordinary skill in the art would understand that the term “partially fabricated integrated circuit” can refer to a silicon wafer during any of many stages of integrated circuit fabrication thereon. A wafer or substrate used in the semiconductor device industry typically includes a diameter of 200 mm, or 300 mm, or 450 mm. The foregoing detailed description assumes embodiments or implementations are implemented on a wafer, or in connection with processes associated with forming or fabricating a wafer. However, the disclosed implementations are not so limited. The work piece may be of various shapes, sizes, and materials. In addition to semiconductor wafers, other work pieces that may take advantage of the disclosed implementations and may include various articles such as printed circuit boards, or the fabrication of printed circuit boards, and the like.

15 [0214] Unless the context of this disclosure clearly requires otherwise, throughout the claims, the words “comprise,” “comprising,” and the like are to be construed in an inclusive sense as opposed to an exclusive or exhaustive sense; that is to say, in a sense of “including, but not limited to.” Words using the singular or plural number also generally include the plural or singular number respectively. When the word “or” is used in reference to a list of 2 or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list. The term “implementation” refers to implementations of techniques and methods described herein, as well as to physical objects that embody the structures and/or incorporate the techniques and/or methods described herein.

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