

METHOD AND APPARATUS FOR FORMING A FLIP CHIP
SEMICONDUCTOR PACKAGE AND METHOD FOR PRODUCING A
SUBSTRATE FOR THE FLIP CHIP SEMICONDUCTOR PACKAGE

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ABSTRACT

Specifications of a flip chip package and mold compound for a package are provided to a mold flow simulator and locations of void formation in the package during molding, identified. Subsequently, a substrate (124) for the package is designed with vias (206) at the locations of void formation. During molding, air pockets at the locations of void formation escape through the vias (206) and vents (116) in the lower cavity bar (110), as mold compound flows between the die (and the substrate (124) and forces the air out. In addition, the lower cavity bar (110) has a down set central location (114), which allows air to pass from the vias (206) to the vents (116). In addition, as the diameter of a via (206) is between 20–30 microns, more area on the lower surface of the substrate (124) is available for terminals arranged in an array.

FIG. 2 accompanies this abstract.