METHODS OF FORMING LEAD FREE SOLDER BUMPS AND RELATED STRUCTURES

RELATED APPLICTION

[0001] The present application claims the benefit of priority as a Continuation-In-Part application from U.S. Patent Application Serial No. 10/601,938 filed on June 23, 2003, which claims the benefit of priority from U.S. Provisional Patent Application No. 60/391,511 filed on June 25, 2002. The disclosures of U.S. Patent Application No. 10/601,938 and U.S. Provisional Patent Application No. 60/391,511 are hereby incorporated herein in their entirety by reference. The present application also claims the benefit of priority from U.S. Provisional Application No. 60/584,016 filed on June 30, 2004, the disclosure of which is hereby incorporated herein in its entirety by reference.

BACKGROUND

[0002] For relatively high pin-counts and/or relatively high performance SoCs (System-On-Chips), solder bumping on 300mm-wafers is moving from a development phase to a high-volume production phase. At the same time, laws are being enacted to prohibit solders including lead (Pb). To meet the demand for mass-production using lead-free solder, eutectic tin-silver (Sn-Ag) solder alloys have been proposed. In addition, tin-silver-copper (Sn-Ag-Cu) ternary alloys have been proposed to potentially provide improved thermal fatigue properties.

[0003] In the reference by Hirokazu Ezawa *et al.* entitled "*Pb-Free Bumpling By Alloying Electroplated Metal Stacks*" (IEEE, 2003 Electronic Components And Technology Conference, pages 664-667), a eutectic Sn-Ag solder bumping process is discussed using two step electroplating of Ag/Sn metal stacks. In the Ezawa reference, alloying behavior of Ag/Sn and Ag/Sn/Cu electroplated metal stacks is investigated using differential scanning calorimetry (DSC) analysis. In particular, a 2μm Ag/ 50μm Sn electroplated metal stack may provide the Sn-Ag solder alloy with a composition of Sn-3.5wt.%Ag, with a

melting temperature of 227 °C, determined using a single peak of DSC analysis. For a 2μm Ag/Cu/50μm Sn electroplated stack, as the Cu thickness increases from 0μm to 0.8μm, the single peak temperature may decrease to 222 °C. According to the Ezawa reference, metal stacks formed by multi-step electroplating can be successfully transformed to solder alloys by reflow annealing. The disclosure of the Esawa reference is hereby incorporated herein in its entirety by reference.

SUMMARY

[0004] According to some embodiments of the present invention, a method of forming an electronic device may include forming an under bump seed metallurgy layer on an electronic substrate. A nickel layer may be formed on the under bump seed metallurgy layer so that the under bump seed metallurgy layer is between the nickel layer and the electronic substrate, and portions of the under bump seed metallurgy layer may be free of the nickel layer. After forming the nickel layer, a lead free solder layer may be formed on the nickel layer so that the nickel layer is between the solder layer and the under bump seed metallurgy layer. In addition, a copper layer may be formed on the under bump seed metallurgy layer before forming the nickel layer so that the under bump seed metallurgy layer is between the copper layer and the electronic substrate, and so that the copper layer is between the nickel layer and the under bump seed metallurgy layer. In addition, portions of the under bump seed metallurgy layer may be free of the copper layer.

[0005] In addition, a plating mask may be formed on the under bump seed metallurgy layer before forming the copper layer, and portions of the under bump seed metallurgy layer may be exposed through the plating mask. Accordingly, the copper layer may be formed by plating the copper layer on the portions of the under bump seed metallurgy layer exposed through the plating mask, the nickel layer may be formed by plating the nickel layer on the copper layer, and the solder layer may be formed by plating the solder layer on the nickel layer. The plating mask may then be removed after forming the solder layer, and portions of the under bump seed metallurgy layer free of the copper and/or nickel layers may be removed after removing the plating mask.

[0006] The nickel layer may have a thickness in the range of about 1 μm (micrometer) to about 5 μm (micrometer), and more particularly, in the range of about 1.5 μm (micrometer) to about 5 μm (micrometer), and the copper layer may have a thickness greater than about 5 μm (micrometer). In addition, the solder layer may comprise a lead-free solder layer, for example, including tin and at least one of silver, bismuth, copper, indium, antimony, gold, and/or zinc, and a weight percent of tin in the solder may be greater than about 95 weight percent. More particularly, a weight percent of tin in the solder layer may be in the range of about 97 weight percent and about 99.5 weight percent.

[0007] Forming the solder layer may include forming a first layer of tin and forming a second layer of silver, bismuth, copper, indium, antimony, gold, and/or zinc, and the first layer may be between the second layer and the nickel layer. The first layer of tin may be greater than about 95 weight percent of the solder layer. More particularly, the first layer of tin may be in the range of about 97 weight percent and about 99.5 weight percent of the solder layer, and the first and second layers may be heated to provide an alloy thereof after forming the solder layer. More particularly, heating the first and second layers may include heating the first and second layers to a temperature that is less than a melting temperature of the first and/or second layers. In an alternative, heating the first and second layers may include heating the first and second layers to a temperature that is less than a melting temperature of one of the first or second layers and greater than a melting temperature of the other of the first or second layers. In another alternative, heating the first and second layers may include heating the first and second layers to a temperature that is less than a melting temperature of either of the first and second layers and above a melting temperature of the alloy thereof.

[0008] In addition, forming the under bump seed metallurgy layer may include forming an adhesion layer on the electronic substrate, and forming a conduction layer on the adhesion layer such that the adhesion layer is between the conduction layer and the electronic substrate. Moreover, the adhesion layer and the conduction layer may include different materials. The adhesion layer may include Ti (titanium), TiW (titanium-tungsten), TiN (titanium nitride), and/or Cr

(chromium), and the conduction layer may include Cu (copper), Ag (silver), and/or Au (gold).

[0009] In an alternative, forming the solder layer may include plating first and second portions of the solder layer using a same plating bath including first and second plating metals. The first portion of the solder layer may be plated in the plating bath using a first plating voltage and/or current so that the first portion of the solder layer has a first concentration of the first plating metal. The second portion of the solder layer may be plated in the plating bath using a second plating voltage and/or current so that the second portion of the solder layer has a second concentration of the first plating metal different than the first concentration.

[0010] According to some additional embodiments of the present invention, a method of forming an electronic device may include forming an under bump seed metallurgy layer on an electronic substrate. A first solder layer including a first metal may be formed on portions of the under bump seed metallurgy layer so that the under bump seed metallurgy layer is between the first solder layer and the electronic substrate. A second solder layer including a second metal may be formed on the first solder layer so that the first solder layer is between the second solder layer and the under bump seed metallurgy layer. The first and second solder layers may then be heated to a temperature that is less than a melting temperature of the first and/or second metals to provide an alloy of the first and second metals.

[0011] The first metal may include one of silver or tin, and the second metal may include the other of silver or tin. More particularly, the first solder layer may be a layer of tin, and the second solder layer may be a layer of silver. Moreover, heating the first and second solder layers may include heating the first and second solder layers to a temperature that is less than a melting temperature of either of the first and second metals and that is greater than a melting temperature of the alloy of the first and second metals. Forming the first solder layer may include forming a layer of the first metal, and forming the second solder layer may include forming a layer of the second metal.

[0012] In an alternative, the first and second solder layers may be formed using a same plating bath including the first and second metals.

Accordingly, forming the first solder layer may include plating the first solder layer using the plating bath and using a first plating voltage and/or plating current so that the first solder layer has a first concentration of the first metal. Similarly, forming the second solder layer may include plating the second solder layer using the plating bath and using a second plating voltage and/or plating current so that the second solder layer has a second concentration of the first metal different than the first concentration of the first metal.

[0013] In addition, a plating mask may be formed on the under bump seed metallurgy layer before forming the first and second solder layers, and portions of the under bump seed metallurgy layer may be exposed through the plating mask. Accordingly, forming the first solder layer may include plating the first solder layer on the portions of the under bump seed metallurgy layer exposed through the plating mask, and forming the second solder layer may include plating the second solder layer on the first solder layer. In addition, a copper layer may be plated on the portions of the under bump seed metallurgy layer exposed through the plating mask before forming the first and second solder layers. Moreover, a nickel layer may be formed on the copper layer before forming the first and second solder layers. Accordingly, the copper layer may be between the nickel layer and the under bump seed metallurgy layer, the nickel layer may be between the first solder layer and the copper layer, and the first solder layer may be between the second solder layer and the nickel layer.

[0014] Moreover, the alloy of the first and second metals may be lead free. For example, the first metal may include tin and the second metal may include silver, bismuth, copper, indium, antimony, gold, and/or zinc, and a weight percent of tin in the solder may be greater than about 95 weight percent. More particularly, a weight percent of tin in the alloy of the first and second metals may be in the range of about 97 weight percent to about 99.5 weight percent.

[0015] In addition, forming the under bump seed metallurgy layer may include forming an adhesion layer on the electronic substrate, and forming a conduction layer on the adhesion layer. The adhesion layer may be between the conduction layer and the electronic substrate, and the adhesion layer and the conduction layer may include different materials. More particularly, the adhesion

layer may include Ti (titanium), TiW (titanium-tungsten), TiN (titanium nitride), and/or Cr (chromium), and the conduction layer may include Cu (copper), Ag (silver), and/or Au (gold).

[0016] According to some more embodiments of the present invention, a method of forming an electronic device may include forming an under bump seed metallurgy layer on an electronic substrate, and first and second solder layers may be plated using a same plating bath including first and second plating metals. More particularly, the first solder layer may be plated on portions of the under bump seed metallurgy layer using the plating bath and using a first plating voltage and/or plating current so that the first solder layer has a first concentration of the first plating metal. The second solder layer may be plated on the first solder layer using the plating bath and using a second plating voltage and/or plating current so that the second solder layer has a second concentration of the first plating metal different than the first concentration of the first plating metal.

[0017] After plating the first and second solder layers, the first and second solder layers may be heated to a temperature that is less than a melting temperature of the first and/or second metals to provide at least partial mixing of the first and second solder layers. For example, the first metal may be tin, and a weight percent of tin in the mixture of the first and second solder layers may be greater than about 95 weight percent. More particularly, a weight percent of tin in the mixture of the first and second solder layers may be in the range of about 97 weight percent to about 99.5 weight percent. Moreover, the first metal may include tin, and the second metal may include silver, bismuth, copper, indium, antimony, gold, and/or zinc.

[0018] The first solder layer may have a third concentration of the second metal, the second solder layer may have a fourth concentration of the second metal, and the third and fourth concentrations may be different. More particularly, the first concentration may be greater than the second concentration, and the fourth concentration may be greater than the third concentration.

[0019] In addition, a plating mask may be formed on the under bump seed metallurgy layer before plating the first and second solder layers such that portions of the under bump seed metallurgy layer are exposed through the plating

mask. Accordingly, plating the first solder layer may include plating the first solder layer on portions of the under bump seed metallurgy layer exposed through the plating mask, plating the second solder layer may include plating the second solder layer on the first solder layer, and the first solder layer may be between the second solder layer and the under bump seed metallurgy layer. Before plating the first and second solder layers, a copper layer may be plated on portions of the under bump seed metallurgy layer exposed through the plating mask, and a nickel layer may be plated on the copper layer. Accordingly, the copper layer may be between the nickel layer and the under bump seed metallurgy layer, and the nickel layer may be between the first solder layer and the copper layer. In addition, the first and second solder layers may be lead free.

[0020] According to yet more embodiments of the present invention, an electronic device may include an electronic substrate and an under bump seed metallurgy layer on the electronic substrate. A nickel layer may be provided on the under bump seed metallurgy layer so that the under bump seed metallurgy layer is between the nickel layer and the electronic substrate, and portions of the under bump seed metallurgy layer may be free of the nickel layer. In addition, a lead free solder layer may be provided on the nickel layer so that the nickel layer is between the solder layer and the under bump seed metallurgy layer. In addition, a copper layer may be on the under bump seed metallurgy layer before forming the nickel layer so that the under bump seed metallurgy layer is between the copper layer and the electronic substrate, and so that the copper layer is between the nickel layer and the under bump seed metallurgy layer. Moreover, portions of the under bump seed metallurgy layer may be free of the copper layer.

[0021] The nickel layer may have a thickness in the range of about 1 μm (micrometer) to about 5 μm (micrometer), and more particularly, in the range of about 1.5 μm (micrometer) to about 5 μm (micrometer). The copper layer may have a thickness greater than about 5 μm (micrometer). Moreover, the solder layer may be a lead-free solder layer, for example, including tin and at least one of silver, bismuth, copper, indium, antimony, gold, and/or zinc, and a weight percent of tin in the solder may be greater than about 95 weight percent. A weight percent

of tin in the solder layer may be in the range of about 97 weight percent and about 99.5 weight percent.

[0022] In an alternative, the solder layer may include a first layer of tin and a second layer of silver, bismuth, copper, indium, antimony, gold, and/or zinc, and the first layer of tin may be between the second layer and the nickel layer. The first layer of tin may be greater than about 95 weight percent of the solder layer. More particularly, the first layer of tin may be in the range of about 97 weight percent and about 99.5 weight percent of the solder layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Figures 1-4 are cross-sectional views illustrating steps of forming solder bumps according to embodiments of the present invention.

[0024] Figures 5-8 are cross-sectional views illustrating steps of forming solder bumps according to additional embodiments of the present invention.

DETAILED DESCRIPTION

[0025] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[0026] In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when an element such as a layer, region or substrate is referred to as being on another element, it can be directly on the other element or intervening elements may also be present. In contrast, if an element such as a layer, region or substrate is referred to as being directly on another element, then no other intervening elements are present. Similarly, when an element such as a layer, region or substrate is referred to as being coupled or connected to/with another element, it can be directly coupled or

connected to/with the other element or intervening elements may also be present. In contrast, if an element such as a layer, region or substrate is referred to as being directly coupled or connected to/with another element, then no other intervening elements are present. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. The symbol "/" is also used as a shorthand notation for "and/or".

[0027] Furthermore, relative terms, such as beneath, upper, lower, top, and/or bottom may be used herein to describe one element's relationship to another element as illustrated in the figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the figures. For example, if the device in one of the figures is turned over, elements described as below other elements would then be oriented above the other elements. The exemplary term below, can therefore, encompasses both an orientation of above and below.

[0028] It will be understood that although the terms first and second are used herein to describe various regions, layers and/or sections, these regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one region, layer or section from another region, layer or section. Thus, a first region, layer or section discussed below could be termed a second region, layer or section, and similarly, a second region, layer or section could be termed a first region, layer or section without departing from the teachings of the present invention. Like numbers refer to like elements throughout.

[0029] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes", and/or "including," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0030] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0031] A potential difficulty faced by binary lead free structures is the ability to control the process in a manufacturing environment while allowing for a process window large enough for assembly. When plating a tin-silver solder, for example, tin may plate significantly more easily than silver due to differences in electrochemical potentials, and a desired concentration of tin in the resulting binary solder may be significantly greater than that of silver. A concentration of silver in the plating solution, however, may be much greater than that of tin in the plating solution to provide the desired concentrations in the plated solder. Because the concentration of tin in the plating solution is relatively low but the concentration of tin in the resulting plated solder is relatively high, the tin may be depleted from the solder relatively quickly, and a process control may be difficult to maintain.

[0032] According to embodiments of the present invention illustrated in Figures 1-4, an integrated circuit substrate **101** may include a semiconductor substrate having electronic circuits (such as one or more resistors, transistors, diodes, capacitors, inductors, etc.) therein, and a conductive input/output pad **103** (such as an aluminum and/or copper pad) on the substrate **101** may provide electrical connection with one or more circuits of the substrate **101**. In addition, an insulating passivation layer **105** may be provided on the substrate **101** and input/output pad **103**, and a via hole in the passivation layer **105** may expose at least portions of the input/output pad **103**. As used herein, the term substrate may also be defined to include the input/output pad and the passivation layer. The term substrate may also include interconnection wiring therein.

[0033] As shown in Figure 1, an under bump seed metallurgy layer **107** may be deposited on the passivation layer **105** and on exposed portions of the input/output pad **103**, and the under bump seed metallurgy layer **107** may include

an adhesion layer **107a**, such as a layer including titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN), and/or chromium (Cr), and a conduction layer **107b**, such as a layer including copper (Cu), silver (Ag), and/or gold (Au). A plating stencil **108** of an organic and/or an inorganic material can then be formed on the under bump seed metallurgy layer **107**. The plating stencil **108**, for example, may be formed by spinning or laminating a photosensitive material on the under bump seed metallurgy layer **107**, baking the photosensitive material, selectively exposing the photosensitive material to light, and developing the photosensitive material to form a via hole exposing at least portions of the input/output pad **103**.

[0034] An under bump barrier metallurgy layer **109** may then be plated on portions of the under bump seed metallurgy layer **107** exposed through the plating stencil **108**, and the under bump barrier metallurgy layer **109** may include nickel (Ni) and/or copper (Cu). The under bump barrier metallurgy layer **109** may be a layer of nickel having a thickness in the range of about 1 μm (micrometers) to about 5 μm (micrometers), and more particularly, in the range of about 1.5 μm (micrometers) to about 5 μm (micrometers). Seed layers and nickel barrier layers are discussed, for example, in U.S. Patent Publication No. 20040053483 entitled "*Methods Of Forming Electronic Structures Including Conductive Shunt Layers And Related Structures*," the disclosure of which is hereby incorporated herein in its entirety by reference. In an alternative, the under bump barrier metallurgy layer **109** may be a layer of copper having a thickness greater than about 5 μm (micrometers). According to some embodiments of the present invention, the under bump barrier metallurgy layer **109** may include a copper layer (for example, having a thickness greater than about 5 μm) and a nickel layer (for example, having a thickness in the range of about 1 μm to about 5 μm) such that the copper layer is between the nickel layer and the under bump seed metallurgy layer **107**. In some embodiments of the present invention, under bump barrier metallurgy layer **109** may include a nickel layer plated directly on the under bump seed metallurgy layer **107** without an intervening layer of plated copper.

[0035] After plating the under bump barrier metallurgy layer **109**, a lead free solder bump **111** may be plated on the under bump barrier metallurgy layer **109**, and the lead free solder bump **111** may be a binary lead free alloy solder

bump such as a tin-silver (SnAg) alloy solder bump, a tin-silver-copper alloy solder bump, and/or a tin-copper alloy solder bump. Moreover, the lead free solder bump **111** may be plated as separate layers of tin and silver (or separate layers of tin, silver, and copper; separate layers of tin and copper; etc.), and a subsequent reflow (in some embodiments after removing the plating stencil) can be used to form the alloy thereof. In an alternative, the tin and silver may be plated together. In either case, the tin and silver may be provided such that a concentration of silver in the resulting solder alloy is sufficiently low to suppress formation of SnAg platelets, precipitates, and/or needles that may otherwise occur as a result of temperature excursions. A concentration of tin in the resulting solder alloy may be greater than about 95 weight percent. More particularly, a concentration of silver in the resulting solder alloy may be in the range of about 1 weight percent to about 3 weight percent, and/or a concentration of tin in the resulting solder alloy may be in the range of about 97 weight percent to about 99 weight percent. In other alternatives, the lead free solder bump **111** may include tin and at least one of bismuth, copper, indium, antimony, gold, zinc, and/or silver. For example, the lead-free solder bump **111** may include a tin-silver-copper solder. In another alternative, the lead free solder bump may include a tin-copper solder having a concentration of tin of about 99.5 weight percent.

[0036] For example, a first layer of tin can be plated followed by a second layer of silver, or a first layer of silver can be plated followed by a second layer of tin, and thicknesses of the layers of tin and silver can be determined to provide an average concentration of silver in the resulting SnAg solder alloy (after reflow) in the range of about 1 weight percent to about 3 weight percent, and/or to provide an average concentration of tin in the range of about 97 weight percent to about 99 weight percent. The thicker layer of tin may be plated before plating the thinner layer of silver, for example, because the thicker layer of tin may be easier to plate on the under bump barrier metallurgy layer **109** within the hole defined by the plating stencil **108**. Stated in other words, the thinner layer of silver may be plated with better uniformity and/or control after plating the thicker tin layer. After plating the layers of the different metals (and in some embodiments after removing the plating stencil and/or after removing portions of the under bump seed

metallurgy layer), the layers of tin and silver may be heated to a temperature that is less than a melting temperature of at least one of the metals to provide an alloy of the two metals (*e.g.*, tin and silver). More particularly, the layers of the two metals may be heated to a temperature that is less than a melting temperature of either of the two metals (*e.g.*, less than about 232 degrees C for tin and less than about 962 degrees C for silver), but that is greater than a melting temperature of the alloy of the two metals (*e.g.*, greater than about 220 degrees C for tin-silver). In another alternative, the layers of the two metals may be heated to a temperature that is greater than the melting temperature of one of the metals (*e.g.*, greater than about 232 degrees C for tin) but less than a melting temperature of the other metal (*e.g.*, less than about 962 degrees C for silver).

[0037] In an alternative for forming the solder layer **111**, tin and silver can be plated together (simultaneously) to provide a plated alloy having an average concentration of silver in the range of about 1 weight percent to about 3 weight percent, and/or to provide an average concentration of tin in the range of about 97 weight percent to about 99 weight percent. A composition of the plated alloy may be controlled by adjusting an electroplating current density while plating the tin and silver using a plating solution including both tin and silver.

[0038] In another alternative for forming the solder layer **111**, a first relatively tin rich layer may be plated, and then a second relatively silver rich layer may be plated using a same plating bath including both tin and silver. More particularly, the first relatively tin rich layer may be plated using the plating bath and using a first plating voltage and/or plating current, and the second relatively silver rich layer may be plated using the same plating bath and a second plating voltage and/or plating current (different than the first plating voltage and/or plating current) so that a concentration of tin in the first relatively tin rich layer is greater than a concentration of tin in the second relatively silver rich layer and so that a concentration of silver in the first relatively tin rich layer is less than a concentration of silver in the second relatively silver rich layer. For example, the first plating voltage and the first plating current may be less than the second plating voltage and the second plating current. At the higher plating voltage and higher plating current, the plating bath may be relatively depleted of tin in the vicinity of

plating so that a plating rate of tin is reduced while plating the second relatively silver rich layer. As used herein, silver rich means that the concentration of silver is greater in the second layer than in the first layer, but does not necessarily mean that the concentration of silver in the second layer is greater than the concentration of tin in the second layer. After plating the first relatively tin rich layer and the second relatively silver rich layer (and in some embodiments after removing the plating stencil and/or after removing portions of the under bump seed metallurgy layer), the layers may be heated to provide at least partial mixing of the layers. More particularly, the layers may be heated to a temperature that is less than a melting temperature of at least one of silver and/or tin.

[0039] As shown in Figure 1, portions of the under bump metallurgy seed layer **107** may be free of one or more layers making up the under bump barrier metallurgy layer **109**. For example, portions of the under bump metallurgy seed layer **107** may be free of plated copper and nickel layers making up the under bump barrier metallurgy layer **109**. Similarly, portions of the under bump metallurgy seed layer **107** may be free of one or more layers making up the solder bump **111**. For example, portions of the under bump metallurgy seed layer **107** may be free of plated tin and silver layers making up the solder bump **111**.

[0040] As shown in Figure 2, the plating stencil **108** may be removed thereby exposing portions of the under bump seed metallurgy layer **107** surrounding the plated layers (i.e. solder bump **111** and/or under bump barrier metallurgy layer **109**). As shown in Figure 3, exposed portions of the under bump seed metallurgy layer **107** may be etched using the under bump barrier metallurgy layer **109** and/or the solder bump **111** as an etch mask. More particularly, a wet etchant may be selected that selectively etches the under bump seed metallurgy layer **107** with respect to the under bump barrier metallurgy layer **109**. Accordingly, the under bump seed metallurgy layer **107** may be undercut with respect to the under bump barrier metallurgy layer **109**, as shown in Figure 3. While not shown in Figure 3, the etchant used to etch the under bump seed metallurgy layer **107** may etch the solder bump **111** (or portions thereof) selectively with respect to the under bump barrier metallurgy layer **109** so that the solder bump **111** of Figure 3 (or portions thereof) may be set back relative to the

under bump barrier metallurgy layer **109**. Stated in other words, the under bump barrier metallurgy layer **109** of Figure 3 may include a lip portion extending laterally beyond the under bump seed metallurgy layer **107** and the solder bump **111** (or portions thereof). In an alternative, the etchant used to remove exposed portions of the under bump seed metallurgy layer **107** may be selective with respect to the solder bump or portions thereof.

[0041] After removing exposed portions of the under bump seed metallurgy layer **107** to provide the structure illustrated in Figure 3, the solder bump **111** can be subjected to a reflow operation to provide the structure illustrated in Figure 4. If the solder bump **111** is plated as separate layers of different metals, the reflow operation may serve to at least partially mix the separate layers into a solder alloy. For example, if the solder bump **111** is plated as separate layers of tin and silver, a reflow operation may serve to at least partially mix the tin and silver into a tin-silver solder alloy having an average concentration of silver in the range of about 1 weight percent to about 3 weight percent, and/or having an average concentration of tin in the range of about 97 weight percent to about 99 weight percent. The reflow operation may be performed by heating the solder bump **111** to at least a liquidus temperature of a metal of the solder bump having the highest liquidus temperature. According to particular embodiments, the solder bump may be heated to a temperature not exceeding the liquidus temperature of the metal having the highest liquidus temperature. In other alternatives, a reflow operation may be omitted, solid state diffusion at a temperature below the melting temperature of either metal may be used to at least partially mix metals of different layers, and/or the metals may be heated to a temperature greater than a melting temperature of the alloy and less than a melting temperature of either of the metals.

[0042] If different metals of the solder bump **111** are plated simultaneously using a same plating solution, a reflow operation may be performed to provide the rounded shape of Figure 4, and/or to more evenly distribute metals of the solder alloy. If the solder bump **111** is plated as a mixture of tin and silver, a reflow operation may serve to more evenly distribute the tin and silver in the tin-silver solder alloy so that an average concentration of silver is in the range of about 1 weight percent to about 3 weight percent, and/or an average concentration of tin

is in the range of about 97 weight percent to about 99 weight percent. The reflow operation may be performed by heating the solder bump **111** to at least a liquidus temperature of the solder alloy. According to particular embodiments, the solder bump may be heated to a temperature not exceeding the liquidus temperature of the solder alloy. In other alternatives, a reflow operation may be omitted, solid state diffusion at a temperature below the melting temperature of either metal may be used to at least partially mix metals of the solder bump, and/or the metals may be heated to a temperature greater than a melting temperature of the alloy and less than a melting temperature of either of the metals.

[0043] In an alternative, a solder reflow operation may be performed before removing exposed portions of the under bump seed metallurgy layer **107** and/or before removing the plating stencil **108**. If the solder reflow operation is performed before removing exposed portions of the under bump seed metallurgy layer **107**, an additional solder non-wettable layer (such as a layer of chromium) may be provided on portions of the under bump seed metallurgy layer **107** surrounding the plated layers (i.e. under bump barrier metallurgy layer **109** and solder bump **111**). In addition or in an alternative, an oxide layer may be maintained on the solder to prevent spreading across the under bump seed metallurgy layer during reflow.

[0044] According to embodiments of the present invention illustrated in Figures 5-8, redistribution of a solder bump from an input/output pad may be provided, and/or an increased solder bump size may be provided. As shown in Figure 5, an integrated circuit substrate **201** may include a semiconductor substrate having electronic circuits (such as one or more resistors, transistors, diodes, capacitors, inductors, etc.) therein, and a conductive input/output pad **203** (such as an aluminum and/or copper pad) on the substrate **201** may provide electrical connection with one or more circuits of the substrate **201**. In addition, an insulating passivation layer **205** may be provided on the substrate **201** and input/output pad **203**, and a via hole in the passivation layer **205** may expose at least portions of the input/output pad **203**. As used herein, the term substrate may also be defined to include the input/output pad and the passivation layer. The term substrate may also include interconnection wiring therein.

[0045] As shown in Figure 5, an under bump seed metallurgy layer **207** may be deposited on the passivation layer **205** and on exposed portions of the input/output pad **203**, and the under bump seed metallurgy layer **207** may include an adhesion layer **207a**, such as a layer including titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN), and/or chromium (Cr), and a conduction layer **207b**, such as a layer including copper (Cu), silver (Ag), and/or gold (Au). A plating stencil **208** of an organic and/or an inorganic material can then be formed on the under bump seed metallurgy layer **207**. The plating stencil **208**, for example, may be formed by spinning or laminating a photosensitive material on the under bump seed metallurgy layer **207**, baking the photosensitive material, selectively exposing the photosensitive material to light, and developing the photosensitive material to form the via hole exposing at least portions of the input/output pad **203**.

[0046] In embodiments illustrated in Figures 5-8, the plating stencil may expose an elongate portion of the under bump seed metallurgy layer **207** extending away from the input/output pad **203** having a relatively narrow width and an enlarged width portion of the under bump seed metallurgy layer **207** laterally spaced from the input/output pad **203**. In subsequent plating and reflow steps, a relatively wide solder structure may result to provide a relatively thick solder bump laterally spaced apart from the input/output pad **207**, and a relatively narrow solder structure may result to provide a relatively thin solder redistribution line between the solder bump and the input/output pad **207**. Redistribution routing conductors are discussed, for example, in U.S. Patent No. 6,392,163 entitled Controlled-Shaped Solder Reservoirs For Increasing The Volume Of Solder Bumps; U.S. Patent No. 6,389,691 entitled Methods For Forming Integrated Redistribution Routing Conductors And Solder Bumps; U.S. Patent No. 6,388,203 entitled Controlled-Shaped Solder Reservoirs For Increasing The Volume Of Solder Bumps, And Structures Formed Thereby; U.S. Patent No. 6,329,608 entitled Key-Shaped Solder Bumps And Under Bump Metallurgy. The disclosures of these patents are hereby incorporated herein in their entirety by reference.

[0047] An under bump barrier metallurgy layer **209** may then be plated on portions of the under bump seed metallurgy layer **207** exposed through the plating stencil **208**, and the under bump barrier metallurgy layer **209** may include

nickel (Ni) and/or copper (Cu). The under bump barrier metallurgy layer **209** may be a layer of nickel having a thickness in the range of about 1 μm (micrometers) to 5 μm (micrometers), and more particularly, in the range of about 1.5 μm (micrometers) to about 5 μm (micrometers). In an alternative, the under bump barrier metallurgy layer **209** may be a layer of copper having a thickness greater than about 5 μm (micrometers). According to some embodiments of the present invention, the under bump barrier metallurgy layer **209** may include a copper layer (for example, having a thickness greater than about 5 μm) and a nickel layer (for example, having a thickness in the range of about 1 μm to about 5 μm) such that the copper layer is between the nickel layer and the under bump seed metallurgy layer **207**. Because the under bump barrier metallurgy layer **209** is plated using the plating stencil **208**, the under bump barrier metallurgy layer **209** may include an enlarged width portion laterally spaced apart from the input/output pad **203** and a elongate portion between the enlarged width portion and the input/output pad **203**. In some embodiments of the present invention, the under bump barrier metallurgy layer **209** may include a nickel layer plated directly on the under bump seed metallurgy layer **207** without an intervening layer of plated copper.

[0048] After plating the under bump barrier metallurgy layer **209**, a lead free solder structure **211** may be plated on the under bump barrier metallurgy layer **209**, and the lead free solder structure **211** may be a binary lead free alloy solder structure such as a tin-silver (SnAg) alloy solder structure, a tin-silver-copper alloy solder structure, and/or a tin-copper alloy solder structure. Moreover, the lead free solder structure **211** may be plated as separate layers of tin and silver (or separate layers of tin, silver, and copper; separate layers of tin and copper; etc.), and a subsequent reflow (and in some embodiments after removing the plating stencil) can be used to form the alloy thereof. In an alternative, the tin and silver may be plated together. In either case, the tin and silver may be provided such that a concentration of silver in the resulting solder alloy is sufficiently low to suppress formation of SnAg platelets, precipitates, and/or needles that may otherwise occur as a result of temperature excursions. For example, a concentration of tin in the resulting solder alloy may be greater than about 95 weight percent. More particularly, a concentration of silver in the resulting solder alloy may be in the

range of about 1 weight percent to about 3 weight percent, and/or a concentration of tin in the resulting solder alloy may be in the range of about 97 weight percent to about 99 weight percent. In other alternatives, the lead free solder structure **211** may include tin and at least one of bismuth, copper, indium, antimony, gold, zinc, and/or silver. For example, the lead-free solder structure **211** may include a tin-silver-copper solder. In another alternative, the lead-free solder structure may include a tin-copper solder having a concentration of tin of about 99.5 weight percent.

[0049] Because the solder structure **211** is plated using the plating stencil **208**, the solder structure **211** may include an enlarged width portion **211a** laterally spaced apart from the input/output pad **203** and a elongate portion **211b** between the enlarged width portion and the input/output pad **203**. As shown, a plated thickness of the solder structure **211** may be relatively uniform. Differences in widths of the solder structure and underlying under bump barrier metallurgy layer **209** may provide differences in internal solder pressures due to surface tension during a subsequent reflow operation so that solder flows from elongate portion **211b** to enlarged width portion **211a** thereby increasing a size of a resulting solder bump.

[0050] More particularly, a first layer of tin can be plated followed by a second layer of silver, or a first layer of silver can be plated followed by a second layer of tin, and thicknesses of the layers of tin and silver can be determined to provide an average concentration of silver in the resulting SnAg solder alloy (after reflow) in the range of about 1 weight percent to about 3 weight percent, and/or to provide an average concentration of tin in the range of about 97 weight percent to about 99 weight percent. The thicker layer of tin may be plated before plating the thinner layer of silver, for example, because the thicker layer of tin may be easier to plate on the under bump barrier metallurgy layer **209** within the hole defined by the plating stencil **208**. Stated in other words, the thinner layer of silver may be plated with better uniformity and/or control after plating the thicker tin layer. After plating the layers of the different metals (and in some embodiments after removing the plating stencil and/or after removing portions of the under bump seed metallurgy layer), the layers of tin and silver may be heated to a temperature that is

less than a melting temperature of at least one of the metals to provide an alloy of the two metals (*e.g.*, tin and silver). More particularly, the layers of the two metals may be heated to a temperature that is less than a melting temperature of either of the two metals (*e.g.*, less than about 232 degrees C for tin and less than about 962 degrees C for silver), but that is greater than a melting temperature of the alloy of the two metals (*e.g.*, greater than about 220 degrees C for tin-silver). In another alternative, the layers of the two metals may be heated to a temperature that is greater than the melting temperature of one of the metals (*e.g.*, greater than about 232 degrees C for tin) but less than a melting temperature of the other metal (*e.g.*, less than about 962 degrees C for silver).

[0051] In an alternative, tin and silver can be plated together (simultaneously) to provide a plated alloy having an average concentration of silver in the range of about 1 weight percent to about 3 weight percent, and/or having an average concentration of tin in the range of about 97 weight percent to about 99 weight percent. A composition of the plated alloy may be controlled by adjusting an electroplating current density while plating the tin and silver using a plating solution including both tin and silver.

[0052] In another alternative for forming the solder structure **211**, a first relatively tin rich layer may be plated, and then a second relatively silver rich layer may be plated using a same plating bath including both tin and silver. More particularly, the first relatively tin rich layer may be plated using the plating bath and using a first plating voltage and/or plating current, and the second relatively silver rich layer may be plated using the same plating bath and a second plating voltage and/or plating current (different than the first plating voltage and/or plating current) so that a concentration of tin in the first relatively tin rich layer is greater than a concentration of tin in the second relatively silver rich layer and so that a concentration of silver in the first relatively tin rich layer is less than a concentration of silver in the second relatively silver rich layer. For example, the first plating voltage and the first plating current may be less than the second plating voltage and the second plating current. At the higher plating voltage and higher plating current, the plating bath may be relatively depleted of tin in the vicinity of plating so that a plating rate of tin is reduced while plating the second relatively

silver rich layer. As used herein, silver rich means that the concentration of silver is greater in the second layer than in the first layer, but does not necessarily mean that the concentration of silver in the second layer is greater than the concentration of tin in the second layer. After plating the first relatively tin rich layer and the second relatively silver rich layer (and in some embodiments after removing the plating stencil and/or after removing portions of the under bump seed metallurgy layer), the layers may be heated to provide at least partial mixing of the layers. More particularly, the layers may be heated to a temperature that is less than a melting temperature of at least one of silver and/or tin.

[0053] As shown in Figure 5, portions of the under bump metallurgy seed layer **207** may be free of one or more layers making up the under bump barrier metallurgy layer **209**. For example, portions of the under bump metallurgy seed layer **207** may be free of plated copper and nickel layers making up the under bump barrier metallurgy layer **209**. Similarly, portions of the under bump metallurgy seed layer **207** may be free of one or more layers making up the solder structure **211**. For example, portions of the under bump metallurgy seed layer **207** may be free of plated tin and silver layers making up the solder structure **211**.

[0054] As shown in Figure 6, the plating stencil **208** may be removed thereby exposing portions of the under bump seed metallurgy layer **207** surrounding the plated layers (i.e. solder structure **211** and/or under bump barrier metallurgy layer **209**). As shown in Figure 7, exposed portions of the under bump seed metallurgy layer **207** may be etched using the under bump barrier metallurgy layer **209** and/or the solder structure **211** as an etch mask. More particularly, a wet etchant may be selected that selectively etches the under bump seed metallurgy layer **207** with respect to the under bump barrier metallurgy layer **209**. Accordingly, the under bump seed metallurgy layer **207** may be undercut with respect to the under bump barrier metallurgy layer **209**, as shown in Figure 7. While not shown in Figure 7, the etchant used to etch the under bump seed metallurgy layer **207** may etch the solder structure **211** (or portions thereof) selectively with respect to the under bump barrier metallurgy layer **209** so that the solder structure **211** of Figure 7 (or portions thereof) may be set back relative to the under bump barrier metallurgy layer **209**. Stated in other words, the under bump

barrier metallurgy layer **209** of Figure 7 may include a lip portion extending laterally beyond the under bump seed metallurgy layer **207** and the solder structure **211** (or portions thereof). In an alternative, the etchant used to remove exposed portions of the under bump seed metallurgy layer **207** may be selective with respect to the solder structure or portions thereof.

[0055] After removing exposed portions of the under bump seed metallurgy layer **207** to provide the structure illustrated in Figure 7, the solder structure **211** can be subjected to a reflow operation to provide the structure illustrated in Figure 8. By providing elongate and enlarged width portions of the solder structure **211** and the under bump barrier metallurgy layer **209**, differences in internal pressures of the solder due to surface tension may result in a flow of solder from the elongate portion **211b** of the solder structure **211** to the enlarged width portion **211a** of the solder structure **211** so that a thickness and a volume of the resulting solder bump can be increased. Moreover, a thickness of the elongate portion **211b** of the solder structure **211** can be reduced over a conductive redistribution structure.

[0056] If the solder structure **211** is plated as separate layers of different metals, the reflow operation may serve to at least partially mix the separate layers into a solder alloy. For example, if the solder structure **211** is plated as separate layers of tin and silver, a reflow operation may serve to at least partially mix the tin and silver into a tin-silver solder alloy having an average concentration of silver in the range of about 1 weight percent to about 3 weight percent, and/or having an average concentration of tin in the range of about 97 weight percent to about 99 weight percent. The reflow operation may be performed by heating the solder structure **211** to at least a liquidus temperature of a metal of the solder bump having the highest liquidus temperature. According to particular embodiments, the solder bump may be heated to a temperature not exceeding the liquidus temperature of the metal having the highest liquidus temperature. In other alternatives, a reflow operation may be omitted, solid state diffusion at a temperature below the melting temperature of either metal may be used to at least partially mix metals of different layers, and/or the metals may be heated to a

temperature greater than a melting temperature of the alloy and less than a melting temperature of either of the metals.

[0057] If different metals of the solder structure **211** are plated simultaneously using a same plating solution, a reflow operation may be performed to provide the relatively thick raised solder bump **211a** and the relatively thin redistribution solder layer **211b** of Figure 8, and/or to more evenly distribute metals of the solder alloy. If the solder structure **211** is plated as a mixture of tin and silver, a reflow operation may serve to more evenly distribute the tin and silver in the tin-silver solder alloy so that an average concentration of silver is in the range of about 1 weight percent to about 3 weight percent, and/or an average concentration of tin is in the range of about 97 weight percent to about 99 weight percent. The reflow operation may be performed by heating the solder structure **211** to at least a liquidus temperature of the solder alloy. According to particular embodiments, the solder bump may be heated to a temperature not exceeding the liquidus temperature of the solder alloy. In other alternatives, a reflow operation may be omitted, solid state diffusion at a temperature below the melting temperature of either metal may be used to at least partially mix metals of the solder bump, and/or the metals may be heated to a temperature greater than a melting temperature of the alloy and less than a melting temperature of either of the metals.

[0058] In an alternative, a solder reflow operation may be performed before removing exposed portions of the under bump seed metallurgy layer **207**. If the solder reflow operation is performed before removing exposed portions of the under bump seed metallurgy layer **207**, an additional solder non-wettable layer (such as a layer of chromium) may be provided on portions of the under bump seed metallurgy layer **207** surrounding the plated layers (i.e. under bump barrier metallurgy layer **209** and solder structure **211**). In addition or in an alternative, an oxide layer may be maintained on the solder to prevent spreading across the under bump seed metallurgy layer during reflow.

[0059] While particular binary solders (such as tin-silver solder) are discussed herein by way of example, embodiments of the present invention may be provided using other types of solders. Other types of solders, such as ternary

solders, may be used according to some embodiments of the present invention. For example, a ternary solder (such as a tin-silver-copper solder) may be used according to some embodiments of the present invention. Moreover, other binary solders such as tin-copper solders may be used with a concentration of tin in the tin-copper solder of about 99.5 weight percent.

[0060] While the present invention has been particularly shown and described with reference to embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims and their equivalents.

That Which Is Claimed Is:

1. A method of forming an electronic device, the method comprising:

forming an under bump seed metallurgy layer on an electronic substrate;

forming a nickel layer on the under bump seed metallurgy layer so that the under bump seed metallurgy layer is between the nickel layer and the electronic substrate, wherein portions of the under bump seed metallurgy layer are free of the nickel layer; and

forming a lead free solder layer on the nickel layer so that the nickel layer is between the solder layer and under bump seed metallurgy layer.

2. A method according to Claim 1 further comprising:

before forming the nickel layer, forming a plating mask on the under bump seed metallurgy layer wherein portions of the under bump seed metallurgy layer are exposed through the plating mask, wherein forming the nickel layer comprises plating the nickel layer on the portions of the under bump seed metallurgy layer exposed through the plating mask, and wherein forming the solder layer comprises plating the solder layer on the nickel layer.

3. A method according to Claim 2 further comprising:

before forming the nickel layer, plating a copper layer on the portions of the under bump seed metallurgy layer exposed through the plating mask so that the copper layer is between the nickel layer and the under bump seed metallurgy layer..

4. A method according to Claim 2 further comprising:

after forming the solder layer, removing the plating mask; and

after removing the plating mask, removing portions of the under bump seed metallurgy layer free of the nickel layer.

5. A method according to Claim 1 wherein the nickel layer has a thickness in the range of about 1.5 μm (micrometer) to about 5 μm (micrometer)

6. A method according to Claim 1 wherein the nickel layer has a thickness in the range of about 1 μm (micrometer) to about 5 μm (micrometer).

7. A method according to Claim 1 further comprising:

before forming the nickel layer, forming a copper layer on the under bump seed metallurgy layer so that the under bump seed metallurgy layer is between the copper layer and the electronic substrate, wherein portions of the under bump seed metallurgy layer are free of the copper layer, and wherein the copper layer is between the nickel layer and the under bump seed metallurgy layer.

8. A method according to Claim 7 wherein the copper layer has a thickness greater than about 5 μm (micrometer).

9. A method according to Claim 7 wherein the nickel layer has a thickness in the range of about 1 μm (micrometer) to about 5 μm (micrometer).

10. A method according to Claim 1 wherein the solder layer comprises a lead-free solder.

11. A method according to Claim 1 wherein the solder layer comprises tin and at least one of silver, bismuth, copper, indium, antimony, gold, and/or zinc.

12. A method according to Claim 11 wherein a weight percent of tin in the solder layer is greater than about 95 weight percent.

13. A method according to Claim 1 wherein forming the solder layer comprises forming a first layer of tin and forming a second layer of silver, bismuth, copper, indium, antimony, gold, and/or zinc.

14. A method according to Claim 13 wherein the first layer is between the second layer and the nickel layer.

15. A method according to Claim 13 wherein the first layer of tin is greater than about 95 weight percent of the solder layer.

16. A method according to Claim 13 further comprising:

after forming the solder layer, heating the first and second layers to provide an alloy thereof.

17. A method according to Claim 16 wherein heating the first and second layers comprises heating the first and second layers to a temperature that is less than a melting temperature of at least one of the first and/or second layers.

18. A method according to Claim 16 wherein heating the first and second layers comprises heating the first and second layers to a temperature that is less than a melting temperature of one of the first and second layers and greater than a melting temperature of the other of the first and second layers.

19. A method according to Claim 16 wherein heating the first and second layers comprises heating the first and second layers to a temperature that is less than a melting temperature of either of the first and second layers.

20. A method according to Claim 19 wherein heating the first and second layers comprises heating the first and second layers to a temperature above a melting temperature of the alloy thereof.

21. A method according to Claim 1 wherein forming the under bump seed metallurgy layer comprises:

forming an adhesion layer on the electronic substrate; and

forming a conduction layer on the adhesion layer, wherein the adhesion layer is between the conduction layer and the electronic substrate, and wherein the adhesion layer and the conduction layer comprise different materials.

22. A method according to Claim 21 wherein the adhesion layer comprises Ti (titanium), TiW (titanium-tungsten), TiN (titanium nitride), and/or Cr (chromium).

23. A method according to Claim 21 wherein the conduction layer comprises Cu (copper), Ag (silver), and/or Au (gold).

24. A method according to Claim 1 wherein forming the solder layer comprises:

plating a first portion of the solder layer in a plating bath including first and second plating metals using a first plating voltage and/or current so that the first portion of the solder layer has a first concentration of the first plating metal; and

plating a second portion of the solder layer in the plating bath including the first and second plating metals using a second plating voltage and/or current so that the second portion of the solder layer has a second concentration of the first plating metal different than the first concentration.

25. A method of forming an electronic device, the method comprising:

forming an under bump seed metallurgy layer on an electronic substrate;

forming a first solder layer on portions of the under bump seed metallurgy layer so that the under bump seed metallurgy layer is between the first solder layer and the electronic substrate wherein the first solder layer comprises a first metal;

forming a second solder layer on the first solder layer so that the first solder layer is between the second solder layer and the under bump seed metallurgy layer wherein the second solder layer comprises a second metal; and

heating the first and second solder layers to a temperature that is less than a melting temperature of at least one of the first and second metals to provide an alloy of the first and second metals wherein the alloy is lead free.

26. A method according to Claim 25 wherein the first metal comprises one of silver or tin and wherein the second metal comprises the other of silver or tin.

27. A method according to Claim 25 wherein heating the first and second solder layers comprises heating the first and second solder layers to a temperature that is less than a melting temperature of either of the first and second metals.

28. A method according to Claim 27 wherein heating the first and second solder layers comprises heating the first and second solder layers to a temperature that is greater than a melting temperature of the alloy of the first and second metals.

29. A method according to Claim 25 wherein forming the first solder layer comprises forming a layer of the first metal and wherein forming the second solder layer comprises forming a layer of the second metal.

30. A method according to Claim 25:

wherein forming the first solder layer comprises plating the first solder layer using a plating bath including the first and second metals and using a first plating voltage and/or plating current so that the first solder layer has a first concentration of the first metal; and

wherein forming the second solder layer comprises plating the second solder layer using the plating bath including the first and second metals and using a second plating voltage and/or plating current so that the second solder layer has a second concentration of the first metal different than the first concentration of the first metal.

31. A method according to Claim 25 further comprising:

before forming the first and second solder layers, forming a plating mask on the under bump seed metallurgy layer wherein portions of the under bump seed metallurgy layer are exposed through the plating mask, wherein forming the first solder layer comprises plating the first solder layer on the portions of the under bump seed metallurgy layer exposed through the plating mask, and wherein forming the second solder layer comprises plating the second solder layer on the first solder layer.

32. A method according to Claim 31 further comprising:

before forming the first and second solder layers, plating a copper layer on the portions of the under bump seed metallurgy layer exposed through the plating mask, and plating a nickel layer on the copper layer so that the copper layer is between the nickel layer and the under bump seed metallurgy layer, so that the nickel layer is between the first solder layer and the copper layer, and so that the first solder layer is between the second solder layer and the nickel layer.

33. A method according to Claim 25 wherein the first metal comprises tin and the second metal comprises silver, bismuth, copper, indium, antimony, gold, and/or zinc.

34. A method according to Claim 33 wherein the weight percent of tin in the alloy of the first and second metals is greater than about 95 weight percent.

35. A method according to Claim 25 wherein forming the under bump seed metallurgy layer comprises:

forming an adhesion layer on the electronic substrate; and

forming a conduction layer on the adhesion layer, wherein the adhesion layer is between the conduction layer and the electronic substrate, and wherein the adhesion layer and the conduction layer comprise different materials.

36. A method according to Claim 35 wherein the adhesion layer comprises Ti (titanium), TiW (titanium-tungsten), TiN (titanium nitride), and/or Cr (chromium).

37. A method according to Claim 35 wherein the conduction layer comprises Cu (copper), Ag (silver), and/or Au (gold).

38. A method of forming an electronic device, the method comprising:

forming an under bump seed metallurgy layer on an electronic substrate;

plating a first solder layer on portions of the under bump seed metallurgy layer using a plating bath including first and second plating metals and using a first plating voltage and/or plating current so that the first solder layer has a first concentration of the first plating metal; and

plating a second solder layer on the first solder layer using the plating bath including the first and second plating metals and using a second plating voltage and/or plating current so that the second solder layer has a second concentration of the first plating metal different than the first concentration of the first plating metal.

39. A method according to Claim 38 further comprising:

after plating the first and second solder layers, heating the first and second solder layers to a temperature that is less than a melting temperature of at least one of the first and second metals to provide at least partial mixing of the first and second solder layers.

40. A method according to Claim 39 wherein the first metal comprises tin, and wherein a weight percent of tin in the mixture of the first and second solder layers is greater than about 95 weight percent.

41. A method according to Claim 38 wherein the first metal comprises tin and wherein the second metal comprises silver, bismuth, copper, indium, antimony, gold, and/or zinc.

42. A method according to Claim 38 wherein the first solder layer has a third concentration of the second metal and the second solder layer has a fourth concentration of the second metal, and wherein the third and fourth concentrations are different.

43. A method according to Claim 42 wherein the first concentration is greater than the second concentration, and wherein the fourth concentration is greater than the third concentration.

44. A method according to Claim 38 further comprising:

before plating the first and second solder layers, forming a plating mask on the under bump seed metallurgy layer wherein portions of the under bump seed metallurgy layer are exposed through the plating mask, wherein plating the first solder layer comprises plating the first solder layer on portions of the under bump seed metallurgy layer exposed through the plating mask, and wherein plating the second solder layer comprises plating the second solder layer on the first solder layer so that the first solder layer is between the second solder layer and the under bump seed metallurgy layer.

45. A method according to Claim 44 further comprising:

before plating the first and second solder layers, plating a copper layer on portions of the under bump seed metallurgy layer exposed through the plating mask, and plating a nickel layer on the copper layer so that the copper layer is between the nickel layer and the under bump seed metallurgy layer and so that the nickel layer is between the first solder layer and the copper layer.

46. A method according to Claim 38 wherein the first and second solder layers are lead free.

47. An electronic device comprising:

an electronic substrate;

an under bump seed metallurgy layer on the electronic substrate;

a nickel layer on the under bump seed metallurgy layer so that the under bump seed metallurgy layer is between the nickel layer and the electronic substrate, wherein portions of the under bump seed metallurgy layer are free of the nickel layer; and

a lead free solder layer on the nickel layer so that the nickel layer is between the solder layer and and the under bump seed metallurgy layer.

48. An electronic device according to Claim 47 wherein the nickel layer has a thickness in the range of about 1 μm (micrometer) to about 5 μm (micrometer).

49. An electronic device according to Claim 48 wherein the nickel layer has a thickness in the range of about 1.5 μm (micrometer) to about 5 μm (micrometer)

50. An electronic device according to Claim 47 further comprising:

a copper layer on the under bump seed metallurgy layer so that the under bump seed metallurgy layer is between the copper layer and the electronic substrate, wherein portions of the under bump seed metallurgy layer are free of the copper layer, and wherein the copper layer is between the under bump seed metallurgy layer and the nickel layer.

51. An electronic device according to Claim 50 wherein the copper layer has a thickness greater than about 5 μm (micrometer).

52. An electronic device according to Claim 51 wherein the nickel layer has a thickness in the range of about 1.5 μm (micrometer) to about 5 μm (micrometer).

53. An electronic device according to Claim 47 wherein the solder layer comprises a lead-free solder.

54. An electronic device according to Claim 47 wherein the solder layer comprises tin and at least one of silver, bismuth, copper, indium, antimony, gold, and/or zinc.

55. An electronic device according to Claim 54 wherein a weight percent of tin in the solder layer is greater than about 95 weight percent.

56. An electronic device according to Claim 47 wherein the solder layer comprises a first layer of tin and a second layer of silver, bismuth, copper, indium, antimony, gold, and/or zinc.

57. An electronic device according to Claim 56 wherein the first layer is between the second layer and the nickel layer.

58. An electronic device according to Claim 56 wherein the first layer of tin is greater than about 95 weight percent of the solder layer.