WHAT IS CLAIMED IS:

1. A storage device capable of communicating with a host, the storage device comprising:

a reconfigurable logic circuit configured to:

operate as a first accelerator implemented to perform a first function corresponding to a first application executed by the host;

change~~able~~ from ~~a~~ the first accelerator to a second accelerator, different from the first accelerator, during an operation of the storage device; and

operate as the second accelerator implemented to perform a second function corresponding to a second application executed by the host, wherein the first application that uses the first accelerator to execute calculations is different from the second application that uses the second accelerator to execute calculations;

a control logic circuit configured to receive, from the host, a host command including information about ~~a~~ the second function required by the host, and to dynamically reconfigure the reconfigurable logic circuit such that the reconfigurable logic circuit performs the second function according to the received host command; and

non-volatile memory connected to the control logic circuit,

wherein the control logic circuit comprises a command decoder configured to detect the second function from the host command as a detected function, and to determine whether a design file for implementing the detected function into the reconfigurable logic circuit has been stored in the non-volatile memory.

2. The storage device of claim 1, wherein the control logic circuit comprises a configuration controller configured to dynamically reconfigure the reconfigurable logic circuit, by programming, in the reconfigurable logic circuit, ~~a~~ the design file for implementing the second function into the reconfigurable logic circuit.

3. The storage device of claim 2, wherein the configuration controller is further configured to receive the design file from the host as a received design file and program the received design file into the reconfigurable logic circuit.

4. The storage device of claim 2, wherein

the non-volatile memory is further configured to store the design file, and

the configuration controller is further configured to receive the design file from the non-volatile memory as a received design file and program the received design file into the reconfigurable logic circuit.

5. The storage device of any of claims 2 to 4, wherein the control logic circuit further comprises a memory controller configured to control a read operation for reading the design file from the non-volatile memory as a read design file and provide the read design file to the configuration controller.

6. The storage device of claim 2, further comprising:

volatile memory that stores the design file, and

wherein the configuration controller is further configured to receive the design file from the volatile memory as a received design file and program the received design file into the reconfigurable logic circuit.

7. The storage device of claim 1, further comprising volatile memory,

wherein the ~~control logic circuit comprises a~~ command decoder is configured ~~to detect the function from the host command as a detected function, and~~ to determine whether ~~a~~ the design file for implementing the detected function into the reconfigurable logic circuit has been stored in the non-volatile memory or the volatile memory.

8. The storage device of any one of claims 1 to 7, wherein a first chip including the control logic circuit and a second chip including the reconfigurable logic circuit are mounted on a single board.

9. The storage device of any one of claims 1 to 7, wherein a first chip including the control logic circuit and a second chip including the reconfigurable logic circuit are implemented as a package-on-package (POP).

10. The storage device of any one of claims 1 to 7, wherein the control logic circuit and the reconfigurable logic circuit are implemented in a single chip.

11. The storage device of any one of claims 1 to 10, wherein the reconfigurable logic circuit includes a field programmable gate array (FPGA).

12. A storage system, comprising:

a storage device comprising a reconfigurable logic circuit; and

a host capable of executing a plurality of applications and configured to decide reconfiguration of the reconfigurable logic circuit such that the reconfigurable logic circuit operates as a first accelerator corresponding to a first application from among the plurality of applications and to transmit a first host command including information about the first application to the storage device,

wherein the reconfigurable logic circuit is reconfigured to the first accelerator according to the first host command,

wherein during an operation of the storage system and after transmitting the first host command, the host is further configured to decide reconfiguration of the reconfigurable logic circuit such that the reconfigurable logic circuit operates as a second accelerator corresponding to a second application from among the plurality of applications and to transmit a second host command including information about the second application to the storage device, and

wherein the storage device further comprises:

memory; and

a command decoder configured to detect information about the first application from the first host command and determine whether a first design file for implementing the reconfigurable logic circuit into the first accelerator has been stored in the memory.

13. The storage system of claim 12, wherein the host is further configured to transmit, to the storage device, ~~a~~ the first design file for programming the reconfigurable logic circuit into the first accelerator.

~~14. The storage system of claim 12 or claim 13, wherein during an operation of the storage system and after transmitting the first host command, the host is further configured to decide reconfiguration of the reconfigurable logic circuit such that the reconfigurable logic circuit operates as a second accelerator corresponding to a second application from among the plurality of applications and to transmit a second host command including information about the second application to the storage device.~~

1~~5~~4. The storage system of claim ~~14~~12, wherein the host is further configured to transmit, to the storage device, a second design file for programming the reconfigurable logic circuit into the second accelerator.

~~16~~15. The storage system of claim 12, wherein the storage device further comprises a configuration controller configured to dynamically reconfigure the reconfigurable logic circuit, by programming, in the reconfigurable logic circuit, ~~a~~ the

first design file for implementing the reconfigurable logic circuit into the first accelerator according to the first host command.

~~17. The storage system of claim 16, wherein the storage device further comprises:~~

~~memory; and~~

~~a command decoder configured to detect information about the first application from the first host command and determine whether a design file for implementing the reconfigurable logic circuit into the first application has been stored in the memory.~~

~~18~~16. A method of operating a storage device including a reconfigurable logic circuit, memory and a command decoder, the method comprising:

receiving, from a host, a host command including information about a function required by the host, wherein the receiving is performed by the storage device; ~~and~~

dynamically reconfiguring the reconfigurable logic circuit to correspond to the function, by downloading, into the reconfigurable logic circuit, a design file for implementing the function into the reconfigurable logic circuit, according to the host command, wherein the dynamically reconfiguring is performed by the storage device; and

performing, by the reconfigurable logic circuit, a convolutional neural network (CNN) operation or a recurrent neural network (RNN) operation as the neural network operation according to the design file,

wherein the method further comprises:

before the dynamically reconfiguring, detecting the function from the host command as a detected function, and determining whether the design file for implementing the detected function has been stored in the memory, wherein the detecting and the determining are performed by the command decoder.

~~19~~17. The method of claim ~~18~~16, further comprising, before the dynamically reconfiguring, ~~detecting the function from the host command as a detected function, and~~ determining whether the detected function has been implemented in the reconfigurable logic circuit, wherein ~~the detecting and~~ the determining is performed by the command decoder~~storage device~~.

~~20~~18. The method of claim ~~18~~ 16 or claim ~~19~~17, wherein

the ~~storage device further comprises~~ memory ~~that~~ stores the design file, and

the method further comprises, before the dynamically reconfiguring, reading by the storage device the design file from the memory.