CLAIMS

1. A memory, comprising:

an anti-fuse array, comprising a plurality of anti-fuse structures, wherein the plurality of anti-fuse structures are arranged in a first direction and a second direction, the first direction is perpendicular to or has an acute angle with the second direction, and each of the plurality of anti-fuse structures comprises:

a first unit comprising a first selection transistor, a first anti-fuse cell and a second anti-fuse cell, and

a second unit comprising a second selection transistor, a third anti-fuse cell and a fourth anti-fuse cell,

wherein the first unit and the second unit share an active region; and

a plurality of programming lines arranged in the first direction and extending in the second direction;

wherein the active region is provided with a first extension part and a second extension part which are independent of each other at a first side, and the active region is provided with a third extension part and a fourth extension part which are independent of each other at a second side, the first side being opposite to the second side in the first direction, wherein the first anti-fuse cell is arranged at the first extension part, the second anti-fuse cell is arranged at the second extension part, the third anti-fuse cell is arranged at the third extension part, and the fourth anti-fuse cell is arranged at the fourth extension part;

a row of anti-fuse structures arranged in the second direction corresponds to four programming lines, the four programming lines being respectively connected to first anti-fuse cells, second anti-fuse cells, third anti-fuse cells and fourth anti-fuse cells of the anti-fuse structures; and

in the second direction, adjacent anti-fuse cells of adjacent anti-fuse structures share a same gate structure which is connected to one of the four programming lines;

wherein each of the plurality of anti-fuse structures further comprises:

a first gate structure arranged on a surface of the active region and not overlapping with either the first extension part or the second extension part;

a second gate structure arranged on the surface of the active region, not overlapping with either the third extension part or the fourth extension part, and spaced from the first gate structure;

a third gate structure arranged on a surface of the first extension part;

a fourth gate structure arranged on a surface of the second extension part;

a fifth gate structure arranged on a surface of the third extension part;

a sixth gate structure arranged on a surface of the fourth extension part;

a first doped region arranged in the active region between the first gate structure and the second gate structure;

a second doped region arranged in the active region on a side, away from the second gate structure, of the first gate structure and in the first extension part and the second extension part; and

a third doped region arranged in the active region on a side, away from the first gate structure, of the second gate structure and in the third extension part and the fourth extension part,

wherein the first gate structure, the first doped region and the second doped region form the first selection transistor; the third gate structure and the second doped region in the first extension part form the first anti-fuse cell; the fourth gate structure and the second doped region in the second extension part form the second anti-fuse cell; the second gate structure, the first doped region and the third doped region form the second selection transistor; the fifth gate structure and the third doped region in the third extension part form the third anti-fuse cell; and the sixth gate structure and the third doped region in the fourth extension part form the fourth anti-fuse cell.

2. The memory of claim 1, wherein the first gate structure and the second gate structure are arranged in the first direction, the third gate structure and the fourth gate structure are arranged in the second direction, and the fifth gate structure and the sixth gate structure are arranged in the second direction.

3. The memory of claim 1, wherein each of the plurality of anti-fuse structures further comprises:

a bit line connection structure connected to the first doped region between the first gate structure and the second gate structure, wherein the first doped region is configured to be connected to a bit line through the bit line connection structure.

4. The memory of claim 1, wherein each of the plurality of anti-fuse structures further comprises:

a first connection structure connected to the third gate structure, wherein the third gate structure is configured to be connected to a programming line through the first connection structure, the first connection structure being arranged on a side, away from the second extension part, of the first extension part; and

a second connection structure connected to the fourth gate structure, wherein the fourth gate structure is configured to be connected to another programming line through the second connection structure, the second connection structure being arranged on a side, away from the first extension part, of the second extension part.

5. The memory of claim 4, wherein the third gate structure comprises a third main region corresponding to the first extension part and a third sub-region protruding away from the second extension part, and the first connection structure is connected to the third sub-region, and wherein the fourth gate structure comprises a fourth main region corresponding to the second extension part and a fourth sub-region protruding away from the first extension part, and the second connection structure is connected to the fourth sub-region.

6. The memory of claim 1, wherein each of the plurality of anti-fuse structures further comprises:

a third connection structure connected to the fifth gate structure, wherein the fifth gate structure is configured to be connected to a programming line through the third connection structure, the third connection structure being arranged on a side, away from the fourth extension part, of the third extension part; and

a fourth connection structure connected to the sixth gate structure, wherein the sixth gate structure is configured to be connected to another programming line through the fourth connection structure, the fourth connection structure being arranged on a side, away from the third extension part, of the fourth extension part.

7. The memory of claim 6, wherein the fifth gate structure comprises a fifth main region corresponding to the third extension part and a fifth sub-region protruding in a direction away from the fourth extension part, and the third connection structure is connected to the fifth sub-region, and wherein the sixth gate structure comprises a sixth main region corresponding to the fourth extension part and a sixth sub-region protruding in a direction away from the third extension part, and the fourth connection structure is connected to the sixth sub-region.

8. The memory of claim 1, wherein the first selection transistor and the second selection transistor are symmetrically arranged with a first axis as a symmetry axis, the first anti-fuse cell and the third anti-fuse cell are symmetrically arranged with the first axis as the symmetry axis, and the second anti-fuse cell and the fourth anti-fuse cell are symmetrically arranged with the first axis as the symmetry axis.

9. The memory of claim 1, wherein first selection transistors of the anti-fuse structures arranged in the second direction share the same gate structure, and the second selection transistors of the anti-fuse structures arranged in the second direction share the same gate structure.

10. The memory of claim 1, further comprising a plurality of bit lines arranged in the second direction and extending in the first direction, wherein a column of anti-fuse structures arranged in the first direction share the same bit line.