# SEMICONDUCTOR DEVICE AND METHOD OF DEPOSITING ENCAPSULANT ALONG SIDES AND SURFACE EDGE OF SEMICONDUCTOR DIE IN EMBEDDED WLCSP

## Field of the Invention

The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device and method of depositing an encapsulant over the sides and an exposed portion of an active surface of a semiconductor die in a fan-out wafer level chip scale packages (Fo-WLCSP).

## Background of the Invention

Semiconductor devices are commonly found in modern electronic products. Semiconductor devices vary in the number and density of electrical components. Discrete semiconductor devices generally contain one type of electrical component, e.g., light emitting diode (LED), small signal transistor, resistor, capacitor, inductor, and power metal oxide semiconductor field effect transistor (MOSFET). Integrated semiconductor devices typically contain hundreds to millions of electrical components. Examples of integrated semiconductor devices include microcontrollers, microprocessors, charged-coupled devices (CCDs), solar cells, and digital micro-mirror devices (DMDs).

Semiconductor devices perform a wide range of functions such as signal processing, high-speed calculations, transmitting and receiving electromagnetic signals, controlling electronic devices, transforming sunlight to electricity, and creating visual projections for television displays. Semiconductor devices are found in the fields of entertainment, communications, power conversion, networks, computers, and consumer products. Semiconductor devices are also found in military applications, aviation, automotive, industrial controllers, and office equipment.

Semiconductor devices exploit the electrical properties of semiconductor materials. The structure of semiconductor material allows its electrical conductivity to be manipulated by the application of an electric field or base current or through the process of doping. Doping introduces impurities into the semiconductor material to manipulate and control the conductivity of the semiconductor device.

A semiconductor device contains active and passive electrical structures. Active structures, including bipolar and field effect transistors, control the flow of electrical current. By varying levels of doping and application of an electric field or base current, the transistor either promotes or restricts the flow of electrical current. Passive structures, including resistors, capacitors, and inductors, create a relationship between voltage and current necessary to perform a variety of electrical functions. The passive and active structures are electrically connected to form circuits, which enable the semiconductor device to perform high-speed operations and other useful functions.

Semiconductor devices are generally manufactured using two complex manufacturing processes, i.e., front-end

manufacturing, and back-end manufacturing, each involving potentially hundreds of steps. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each semiconductor die is typically identical and contains circuits formed by electrically connecting active and passive components. Back-end manufacturing involves singulating individual semiconductor die from the finished wafer and packaging the die to provide structural support and environmental isolation. The term "semiconductor die" as used herein refers to both the singular and plural form of the words, and accordingly, can refer to both a single semiconductor device and multiple semiconductor devices.

One goal of semiconductor manufacturing is to produce smaller semiconductor devices. Smaller devices typically consume less power, have higher performance, and can be produced more efficiently. In addition, smaller semiconductor devices have a smaller footprint, which is desirable for smaller end products. A smaller semiconductor die size can be achieved by improvements in the front-end process resulting in semiconductor die with smaller, higher density active and passive components. Back-end processes may result in semiconductor device packages with a smaller footprint by improvements in electrical interconnection and packaging materials.

Semiconductor die are typically enclosed within a semiconductor package for electrical interconnect, structural support, and environmental protection of the die. The semiconductor can be subject to damage or degradation if a portion of the semiconductor die is exposed to external elements, particularly when surface mounting the die. For example, the semiconductor die can be damaged or degraded during

handling and exposure to light.

## Summary of the Invention

A need exists to protect the semiconductor die within a semiconductor package. Accordingly, in one embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a semiconductor wafer including a plurality of semiconductor die, forming an insulating layer over the semiconductor wafer, removing a portion of the insulating layer to expose a portion of an active surface of the semiconductor die, singulating the semiconductor wafer to separate the semiconductor die, and depositing an encapsulant over the semiconductor die to cover a side of the semiconductor die and the exposed portion of the active surface of the semiconductor die.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a semiconductor die, forming an insulating layer over the semiconductor die, removing a portion of the insulating layer to expose a portion of a surface of the semiconductor die, and depositing an encapsulant over the semiconductor die to cover a side of the semiconductor die and the exposed portion of the active surface of the semiconductor die.

In another embodiment, the present invention is a semiconductor device comprising a semiconductor die and insulating layer formed over the semiconductor die with a portion of a surface of the semiconductor die devoid of the insulating layer. An encapsulant is deposited over the semiconductor die to cover a side of the semiconductor die and the portion of the surface of the semiconductor die devoid of

the insulating layer.

In another embodiment, the present invention is a semiconductor device comprising a semiconductor die and insulating layer formed over the semiconductor die with a portion of a surface of the semiconductor die devoid of the insulating layer. An encapsulant is deposited over the semiconductor die to cover the portion of the surface of the semiconductor die devoid of the insulating layer.

In another embodiment, the present invention is a method of making a semiconductor device comprising the steps of providing a substrate, mounting a semiconductor die to the substrate, depositing a mold underfill material over a side surface of the semiconductor die and an exposed surface of the semiconductor die, and depositing an encapsulant over the mold underfill material.

## Brief Description of the Drawings

FIG. 1 illustrates a printed circuit board (PCB) with different types of packages mounted to its surface;

FIGs. 2a-2c illustrate further detail of the representative semiconductor packages mounted to the PCB;

FIGs. 3a-3d illustrate a semiconductor wafer with a plurality of semiconductor die separated by a saw street;

FIGs. 4a-4e illustrate a process of depositing an encapsulant over the sides and an exposed portion of an active surface of a semiconductor die in a WLCSP;

FIG. 5 illustrates the WLCSP with the sides and the exposed portion of the active surface of the semiconductor die covered with the encapsulant;

FIGs. 6a-6c illustrate a semiconductor wafer with a

plurality of semiconductor die separated by a saw street;

FIGs. 7a-7e illustrate another process of depositing an encapsulant over the sides and an exposed portion of an active surface of a semiconductor die in a WLCSP;

FIG. 8 illustrates the WLCSP with the sides and the exposed portion of the active surface of the semiconductor die covered with the encapsulant;

FIGs. 9a-9h illustrate a process of depositing a MUF material with the sides and a portion of an active surface of a semiconductor die in a WLCSP;

FIG. 10 illustrates the WLCSP with the sides and the portion of the active surface of the semiconductor die covered with the MUF material;

FIG. 11 illustrates the MUF material disposed between the semiconductor die and substrate; and

FIG. 12 illustrates another WLCSP with the sides and the portion of the active surface of the semiconductor die covered with the MUF material.

## Detailed Description of the Drawings

The present invention is described in one or more embodiments in the following description with reference to the figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

Semiconductor devices are generally manufactured using two complex manufacturing processes: front-end manufacturing and back-end manufacturing. Front-end manufacturing involves the formation of a plurality of die on the surface of a semiconductor wafer. Each die on the wafer contains active and passive electrical components, which are electrically connected to form functional electrical circuits. Active electrical components, such as transistors and diodes, have the ability to control the flow of electrical current. Passive electrical components, such as capacitors, inductors, and resistors, create a relationship between voltage and current necessary to perform electrical circuit functions.

Passive and active components are formed over the surface of the semiconductor wafer by a series of process steps including doping, deposition, photolithography, etching, and planarization. Doping introduces impurities into the semiconductor material by techniques such as ion implantation or thermal diffusion. The doping process modifies the electrical conductivity of semiconductor material in active devices by dynamically changing the semiconductor material conductivity in response to an electric field or base current. Transistors contain regions of varying types and degrees of doping arranged as necessary to enable the transistor to promote or restrict the flow of electrical current upon the application of the electric field or base current.

Active and passive components are formed by layers of materials with different electrical properties. The layers can be formed by a variety of deposition techniques determined in part by the type of material being deposited. For example, thin film deposition can involve chemical vapor deposition (CVD), physical vapor deposition (PVD), electrolytic plating, and

electroless plating processes. Each layer is generally patterned to form portions of active components, passive components, or electrical connections between components.

Back-end manufacturing refers to cutting or singulating the finished wafer into the individual semiconductor die and then packaging the semiconductor die for structural support and environmental isolation. To singulate the semiconductor die, the wafer is scored and broken along non-functional regions of the wafer called saw streets or scribes. The wafer is singulated using a laser cutting tool or saw blade. After singulation, the individual semiconductor die are mounted to a package substrate that includes pins or contact pads for interconnection with other system components. Contact pads formed over the semiconductor die are then connected to contact pads within the package. The electrical connections can be made with solder bumps, stud bumps, conductive paste, or wirebonds. An encapsulant or other molding material is deposited over the package to provide physical support and electrical isolation. The finished package is then inserted into an electrical system and the functionality of the semiconductor device is made available to the other system components.

FIG. 1 illustrates electronic device 50 having a chip carrier substrate or printed circuit board (PCB) 52 with a plurality of semiconductor packages mounted on its surface. Electronic device 50 can have one type of semiconductor package, or multiple types of semiconductor packages, depending on the application. The different types of semiconductor packages are shown in FIG. 1 for purposes of illustration.

Electronic device 50 can be a stand-alone system that uses the semiconductor packages to perform one or more electrical functions. Alternatively, electronic device 50 can

be a subcomponent of a larger system. For example, electronic device 50 can be part of a cellular phone, personal digital assistant (PDA), digital video camera (DVC), or other electronic communication device. Alternatively, electronic device 50 can be a graphics card, network interface card, or other signal processing card that can be inserted into a computer. The semiconductor package can include microprocessors, memories, application specific integrated circuits (ASIC), logic circuits, analog circuits, RF circuits, discrete devices, or other semiconductor die or electrical components. Miniaturization and weight reduction are essential for the products to be accepted by the market. The distance between semiconductor devices must be decreased to achieve higher density.

In FIG. 1, PCB 52 provides a general substrate for structural support and electrical interconnect of the semiconductor packages mounted on the PCB. Conductive signal traces 54 are formed over a surface or within layers of PCB 52 using evaporation, electrolytic plating, electroless plating, screen printing, or other suitable metal deposition process. Signal traces 54 provide for electrical communication between each of the semiconductor packages, mounted components, and other external system components. Traces 54 also provide power and ground connections to each of the semiconductor packages.

In some embodiments, a semiconductor device has two packaging levels. First level packaging is a technique for mechanically and electrically attaching the semiconductor die to an intermediate carrier. Second level packaging involves mechanically and electrically attaching the intermediate carrier to the PCB. In other embodiments, a semiconductor device may only have the first level packaging where the die is mechanically and electrically mounted directly to the PCB.

For the purpose of illustration, several types of first level packaging, including bond wire package 56 and flipchip 58, are shown on PCB 52. Additionally, several types of second level packaging, including ball grid array (BGA) 60, bump chip carrier (BCC) 62, dual in-line package (DIP) 64, land grid array (LGA) 66, multi-chip module (MCM) 68, quad flat non-leaded package (QFN) 70, and quad flat package 72, are shown mounted on PCB 52. Depending upon the system requirements, any combination of semiconductor packages, configured with any combination of first and second level packaging styles, as well as other electronic components, can be connected to PCB 52. In some embodiments, electronic device 50 includes a single attached semiconductor package, while other embodiments call for multiple interconnected packages. By combining one or more semiconductor packages over a single substrate, manufacturers can incorporate pre-made components into electronic devices and systems. Because the semiconductor packages include sophisticated functionality, electronic devices can be manufactured using less expensive components and a streamlined manufacturing process. The resulting devices are less likely to fail and less expensive to manufacture resulting in a lower cost for consumers.

FIGs. 2a-2c show exemplary semiconductor packages. FIG. 2a illustrates further detail of DIP 64 mounted on PCB 52. Semiconductor die 74 includes an active region containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and are electrically interconnected according to the electrical design of the die. For example, the circuit can include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements formed within the active

region of semiconductor die 74. Contact pads 76 are one or more layers of conductive material, such as aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), or silver (Ag), and are electrically connected to the circuit elements formed within semiconductor die 74. During assembly of DIP 64, semiconductor die 74 is mounted to an intermediate carrier 78 using a gold-silicon eutectic layer or adhesive material such as thermal epoxy or epoxy resin. The package body includes an insulative packaging material such as polymer or ceramic. Conductor leads 80 and bond wires 82 provide electrical interconnect between semiconductor die 74 and PCB 52. Encapsulant 84 is deposited over the package for environmental protection by preventing moisture and particles from entering the package and contaminating semiconductor die 74 or bond wires 82.

FIG. 2b illustrates further detail of BCC 62 mounted on PCB 52. Semiconductor die 88 is mounted over carrier 90 using an underfill or epoxy-resin adhesive material 92. Bond wires 94 provide first level packaging interconnect between contact pads 96 and 98. Molding compound or encapsulant 100 is deposited over semiconductor die 88 and bond wires 94 to provide physical support and electrical isolation for the device. Contact pads 102 are formed over a surface of PCB 52 using a suitable metal deposition process such as electrolytic plating or electroless plating to prevent oxidation. Contact pads 102 are electrically connected to one or more conductive signal traces 54 in PCB 52. Bumps 104 are formed between contact pads 98 of BCC 62 and contact pads 102 of PCB 52.

In FIG. 2c, semiconductor die 58 is mounted face down to intermediate carrier 106 with a flipchip style first level packaging. Active region 108 of semiconductor die 58 contains analog or digital circuits implemented as active devices,

passive devices, conductive layers, and dielectric layers formed according to the electrical design of the die. For example, the circuit can include one or more transistors, diodes, inductors, capacitors, resistors, and other circuit elements within active region 108. Semiconductor die 58 is electrically and mechanically connected to carrier 106 through bumps 110.

BGA 60 is electrically and mechanically connected to PCB 52 with a BGA style second level packaging using bumps 112. Semiconductor die 58 is electrically connected to conductive signal traces 54 in PCB 52 through bumps 110, signal lines 114, and bumps 112. A molding compound or encapsulant 116 is deposited over semiconductor die 58 and carrier 106 to provide physical support and electrical isolation for the device. The flipchip semiconductor device provides a short electrical conduction path from the active devices on semiconductor die 58 to conduction tracks on PCB 52 in order to reduce signal propagation distance, lower capacitance, and improve overall circuit performance. In another embodiment, the semiconductor die 58 can be mechanically and electrically connected directly to PCB 52 using flipchip style first level packaging without intermediate carrier 106.

FIG. 3a shows a semiconductor wafer 120 with a base substrate material 122, such as silicon, germanium, gallium arsenide, indium phosphide, or silicon carbide, for structural support. A plurality of semiconductor die or components 124 is formed on wafer 120 separated by a non-active, inter-die wafer area or saw street 126 as described above. Saw street 126 provides cutting areas to singulate semiconductor wafer 120 into individual semiconductor die 124. In one embodiment, semiconductor wafer 120 is 200-300 millimeters (mm) in diameter.

FIG. 3b shows a cross-sectional view of a portion of

semiconductor wafer 120. Each semiconductor die 124 has a back surface 128 and active surface 130 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface 130 to implement analog circuits or digital circuits, such as digital signal processor (DSP), ASIC, memory, or other signal processing circuit. Semiconductor die 124 may also contain integrated passive devices (IPDs), such as inductors, capacitors, and resistors, for RF signal processing.

An electrically conductive layer 132 is formed over active surface 130 using PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 132 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 132 operates as contact pads electrically connected to the circuits on active surface 130. Conductive layer 132 can be formed as contact pads disposed side-by-side a first distance from the edge of semiconductor die 124, as shown in FIG. 3b. Alternatively, conductive layer 132 can be formed as contact pads that are offset in multiple rows such that a first row of contact pads is disposed a first distance from the edge of the die, and a second row of contact pads alternating with the first row is disposed a second distance from the edge of the die.

A first insulating or passivation layer 134 is formed over semiconductor die 124 and conductive layer 132 using PVD, CVD, printing, spin coating, spray coating, sintering or thermal

oxidation. The insulating layer 134 contains one or more layers of silicon dioxide (SiO2), silicon nitride (Si3N4), silicon oxynitride (SiON), tantalum pentoxide (Ta2O5), aluminum oxide (Al2O3), hafnium oxide (HfO2), benzocyclobutene (BCB), polyimide (PI), polybenzoxazoles (PBO), polymer, or other dielectric material having similar structural and insulating properties.

An electrically conductive layer or redistribution layer (RDL) 136 is formed over the first insulating layer 134 using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating. Conductive layer 136 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. One portion of conductive layer 136 is electrically connected to conductive layer 132 of semiconductor die 124. Other portions of conductive layer 136 can be electrically common or electrically isolated depending on the design and function of semiconductor die 124.

A second insulating or passivation layer 134 is formed over conductive layer 136 and the first insulating layer 134. Multiple insulating layers 134 and conductive layers 136 can be formed over active surface 130 of semiconductor die 124. A surface inspection can be performed to detect passivation or RDL defects.

A portion of insulating layer 134 is removed by laser direct ablation (LDA) using laser 138 to expose conductive layer 132 and portion 140 of active surface 130 along a surface edge of semiconductor die 124. That is, portion 140 of active surface 130 along a surface edge of semiconductor die 124 is devoid of insulating layer 134. Alternatively, a portion of insulating layer 134 is removed by an etching process through a patterned photoresist layer to expose conductive layer 132 and

portion 140 of active surface 130 along the surface edge of semiconductor die 124.

In FIG. 3c, an electrically conductive layer 142 is formed over the exposed portion of conductive layer 132 and insulating layer 134 after final repassivation using PVD, CVD, evaporation, electrolytic plating, electroless plating, or other suitable metal deposition process. Conductive layer 142 can be Al, Cu, Sn, Ni, Au, Ag, tungsten (W), or other suitable electrically conductive material. Conductive layer 142 is a UBM electrically connected to conductive layer 132. UBMs 142 can be a multi-metal stack with adhesion layer, barrier layer, and seed or wetting layer. The adhesion layer is formed over conductive layer 132 and can be titanium (Ti), titanium nitride (TiN), titanium tungsten (TiW), Al, or chromium (Cr). The barrier layer is formed over the adhesion layer and can be Ni, NiV, platinum (Pt), palladium (Pd), TiW, or chromium copper (CrCu). The barrier layer inhibits the diffusion of Cu into the active area of the die. The seed layer is formed over the barrier layer and can be Cu, Ni, NiV, Au, or Al. UBMs 142 provide a low resistive interconnect to conductive layer 132, as well as a barrier to solder diffusion and seed layer for solder wettability.

In FIG. 3d, semiconductor wafer 120 is singulated through saw street 126 using a saw blade or laser cutting tool 144 into individual semiconductor die 124.

FIGs. 4a-4e illustrate, in relation to FIGs. 1 and 2a-2c, a process of depositing an encapsulant over the sides and an exposed portion of an active surface of a semiconductor die in a WLCSP. FIG. 4a shows a cross-sectional view of a portion of a carrier or temporary substrate 150 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or

other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 152 is formed over carrier 150 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. Carrier 150 can be a large round or rectangular panel (greater than 300 mm) with capacity for multiple semiconductor die 124.

Semiconductor die 124 from FIG. 3d are mounted to carrier 150 and interface layer 152 using, for example, a pick and place operation with insulating layer 134 oriented toward the carrier. FIG. 4b shows semiconductor die 124 mounted to interface layer 152 of carrier 150 as reconstituted wafer 153. Active surface 130 of semiconductor die 124 is held off or offset from interface layer 152 by nature of insulating layer 134 and/or conductive layer 142 contacting the interface layer, i.e., there is a gap between portion 140 of active surface 130 and interface layer 152.

In FIG. 4c, an encapsulant or molding compound 154 is deposited over semiconductor die 124 and carrier 150 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 154 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 154 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. In particular, encapsulant 154 is disposed along the sides of semiconductor die 124 and in the gap between active surface 130 and interface layer 152 and thus covers the sides of semiconductor die 124 and exposed portion 140 of active surface 130 along the surface edge of the semiconductor die up to insulating layer 134. Accordingly, encapsulant 154 covers or contacts at least five

surfaces of semiconductor die 124, i.e., four side surfaces and portion 140 of active surface 130 of the semiconductor die.

In FIG. 4d, carrier 150 and interface layer 152 are removed by chemical etching, mechanical peeling, chemical mechanical planarization (CMP), mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping to expose insulating layer 134 and conductive layer 142. A portion of encapsulant 154 is removed by LDA using laser 156. Alternatively, a portion of encapsulant 154 is removed by an etching process through a patterned photoresist layer. Portion 140 of active surface 130 along the surface edge of semiconductor die 124, as well as the sides of the semiconductor die, remain covered by encapsulant 154 as a protective panel to increase yield, particularly when surface mounting the semiconductor die. Encapsulant 154 also protects semiconductor die 124 from degradation due to exposure to light. Semiconductor die 124 is prepared for electrical testing by cleaning insulating layer 134 and conductive layer 142 with one or more steps of plasma, wet solvent, copper oxide, or dry cleaning.

In FIG. 4e, an electrically conductive bump material is deposited over conductive layer 142 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. In one embodiment, the bump material is deposited with a ball drop stencil, i.e., no mask required. The bump material can be Al, Sn, Ni, Au, Ag, lead (Pb), Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 142 using a suitable attachment or bonding process. In one embodiment, the bump material is

reflowed by heating the material above its melting point to form balls or bumps 160. In some applications, bumps 160 are reflowed a second time to improve electrical contact to conductive layer 142. Bumps 160 can also be compression bonded or thermocompression bonded to conductive layer 142. Bumps 160 represent one type of interconnect structure that can be formed over conductive layer 142. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Laser marking can be performed before or after bump formation, or after removal of carrier 150.

Semiconductor die 124 are singulated through encapsulant 154 with saw blade or laser cutting tool 162 into individual embedded wafer level ball grid array (eWLB) or wafer-level chip scale package (WLCSP) 164. FIG. 5 shows WLCSP 164 after singulation. In one embodiment, WLCSP 164 has dimensions of 3.0 x 2.6 x 0.7 millimeters mm with 0.4 mm pitch. Semiconductor die 124 is electrically connected to bumps 160 for external interconnect. Encapsulant 154 covers the sides of semiconductor die 124 and portion 140 of active surface 130 to protect the sides and surface edge of the semiconductor die and increase manufacturing yield, particularly when surface mounting the semiconductor die. Encapsulant 154 also protects semiconductor die 124 from degradation due to exposure to light. WLCSP 164 undergoes electrical testing before or after singulation.

FIGs. 6a-6c illustrate another embodiment of semiconductor wafer 170 with a base substrate material 172, such as silicon, germanium, gallium arsenide, indium phosphide, or silicon carbide, for structural support, similar to FIG. 3a. A plurality of semiconductor die or components 174 is formed on wafer 170 separated by a non-active, inter-die wafer area or saw

street 176 as described above. Saw street 176 provides cutting areas to singulate semiconductor wafer 170 into individual semiconductor die 174. In one embodiment, semiconductor wafer 170 is 200-300 millimeters (mm) in diameter.

FIG. 6a shows a cross-sectional view of a portion of semiconductor wafer 170. Each semiconductor die 174 has a back surface 178 and active surface 180 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface 180 to implement analog circuits or digital circuits, such as DSP, ASIC, memory, or other signal processing circuit. Semiconductor die 174 may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing.

An electrically conductive layer 182 is formed over active surface 180 using PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 182 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 182 operates as contact pads electrically connected to the circuits on active surface 180. Conductive layer 182 can be formed as contact pads disposed side-by-side a first distance from the edge of semiconductor die 174, as shown in FIG. 6a. Alternatively, conductive layer 182 can be formed as contact pads that are offset in multiple rows such that a first row of contact pads is disposed a first distance from the edge of the die, and a second row of contact pads alternating with the first row is disposed a second

distance from the edge of the die.

An electrically conductive layer 184 is formed over conductive layer 182 using PVD, CVD, evaporation, electrolytic plating, electroless plating, or other suitable metal deposition process. Conductive layer 184 can be Al, Cu, Sn, Ni, Au, Ag, W, or other suitable electrically conductive material. Conductive layer 184 is a UBM electrically connected to conductive layer 182. UBMs 184 can be a multi-metal stack with adhesion layer, barrier layer, and seed or wetting layer. The adhesion layer is formed over conductive layer 182 and can be Ti, TiN, TiW, Al, or Cr. The barrier layer is formed over the adhesion layer and can be Ni, NiV, Pt, Pd, TiW, or CrCu. The barrier layer inhibits the diffusion of Cu into the active area of the die. The seed layer is formed over the barrier layer and can be Cu, Ni, NiV, Au, or Al. UBMs 184 provide a low resistive interconnect to conductive layer 182, as well as a barrier to solder diffusion and seed layer for solder wettability.

In FIG. 6b, a first insulating or passivation layer 186 is formed over semiconductor die 174 and conductive layer 184 using PVD, CVD, printing, spin coating, spray coating, sintering or thermal oxidation, i.e., passivation occurs after formation of UBM 184. The insulating layer 186 contains one or more layers of SiO2, Si3N4, SiON, Ta2O5, Al2O3, HfO2, BCB, PI, PBO, polymer, or other dielectric material having similar structural and insulating properties.

An electrically conductive layer or RDL 188 is formed over the first insulating layer 186 using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating. Conductive layer 188 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. One portion of conductive layer 188 is

electrically connected to conductive layer 182 of semiconductor die 174. Other portions of conductive layer 188 can be electrically common or electrically isolated depending on the design and function of semiconductor die 174.

A second insulating or passivation layer 186 is formed over conductive layer 188 and the first insulating layer 186. Multiple insulating layers 186 and conductive layers 188 can be formed over active surface 180 of semiconductor die 174. A surface inspection can be performed to detect passivation or RDL defects.

A portion of insulating layer 186 is removed by LDA using laser 190 to expose conductive layer 184 and portion 192 of active surface 180 along a surface edge of semiconductor die 174. That is, portion 192 of active surface 180 along a surface edge of semiconductor die 174 is devoid of insulating layer 186. Alternatively, a portion of insulating layer 186 is removed by an etching process through a patterned photoresist layer to expose conductive layer 182 and portion 192 of active surface 180 along the surface edge of semiconductor die 174.

In FIG. 6c, semiconductor wafer 170 is singulated through saw street 176 using a saw blade or laser cutting tool 194 into individual semiconductor die 174.

FIGs. 7a-7e illustrate, in relation to FIGs. 1 and 2a-2c, another process of depositing an encapsulant over the sides and an exposed portion of an active surface of a semiconductor die in a WLCSP. FIG. 7a shows a cross-sectional view of a portion of a carrier or temporary substrate 200 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 202 is formed over carrier 200 as a temporary adhesive bonding film,

etch-stop layer, or thermal release layer. Carrier 200 can be a large round or rectangular panel (greater than 300 mm) with capacity for multiple semiconductor die 174.

Semiconductor die 174 from FIG. 6c are mounted to carrier 200 and interface layer 202 using, for example, a pick and place operation with insulating layer 186 oriented toward the carrier. FIG. 7b shows semiconductor die 174 mounted to interface layer 202 of carrier 200 as reconstituted wafer 203. Active surface 180 of semiconductor die 174 is held off or offset from interface layer 202 by nature of insulating layer 186 contacting the interface layer, i.e., there is a gap between portion 192 of active surface 180 and interface layer 202.

In FIG. 7c, an encapsulant or molding compound 204 is deposited over semiconductor die 174 and carrier 200 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 204 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 204 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. In particular, encapsulant 204 is disposed along the sides of semiconductor die 174 and in the gap between active surface 180 and interface layer 202 and thus covers the sides of semiconductor die 174 and exposed portion 192 of active surface 180 along the surface edge of the semiconductor die up to insulating layer 186. Accordingly, encapsulant 204 covers or contacts at least five surfaces of semiconductor die 174, i.e., four side surfaces and portion 192 of active surface 180 of the semiconductor die.

In FIG. 7d, carrier 200 and interface layer 202 are removed by chemical etching, mechanical peeling, CMP, mechanical

grinding, thermal bake, UV light, laser scanning, or wet stripping to expose insulating layer 186 and conductive layer 184. A portion of encapsulant 204 is removed by LDA using laser 206. Alternatively, a portion of encapsulant 204 is removed by an etching process through a patterned photoresist layer. Portion 192 of active surface 180 along the surface edge of semiconductor die 124, as well as the sides of the semiconductor die, remain covered by encapsulant 204 as a protective panel to increase yield, particularly when surface mounting the semiconductor die. Encapsulant 204 also protects semiconductor die 174 from degradation due to exposure to light. Semiconductor die 174 is prepared for electrical testing by cleaning insulating layer 186 and conductive layer 184 with one or more steps of plasma, wet solvent, copper oxide, or dry cleaning.

In FIG. 7e, an electrically conductive bump material is deposited over conductive layer 184 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. In one embodiment, the bump material is deposited with a ball drop stencil, i.e., no mask required. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 184 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form balls or bumps 210. In some applications, bumps 210 are reflowed a second time to improve electrical contact to conductive layer 184. Bumps 210 can also be compression bonded or thermocompression bonded to conductive layer 184. Bumps 210

represent one type of interconnect structure that can be formed over conductive layer 184. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect. Laser marking can be performed before or after bump formation, or after removal of carrier 200.

Semiconductor die 174 are singulated through encapsulant 204 with saw blade or laser cutting tool 212 into individual eWLB or WLCSP 214. FIG. 8 shows WLCSP 214 after singulation. In one embodiment, WLCSP 214 has dimensions of 3.0 x 2.6 x 0.7 millimeters mm with 0.4 mm pitch. Semiconductor die 174 is electrically connected to bumps 210 for external interconnect. Encapsulant 204 covers the sides of semiconductor die 174 and portion 192 of active surface 180 to protect the sides and surface edge of semiconductor die 174 and increase manufacturing yield, particularly when surface mounting the semiconductor die. Encapsulant 204 also protects semiconductor die 174 from degradation due to exposure to light. WLCSP 214 undergoes electrical testing before or after singulation.

FIGs. 9a-9h illustrate, in relation to FIGs. 1 and 2a-2c, a process of depositing MUF material over the sides and an exposed portion of an active surface of a semiconductor die in a WLCSP. FIG. 9a shows a semiconductor die 220, from a semiconductor wafer similar to FIG. 3a, having a back surface 222 and active surface 224 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface 224 to implement analog circuits or digital circuits, such as DSP, ASIC, memory, or other signal

processing circuit. Semiconductor die 220 may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing. In one embodiment, semiconductor die 220 is a flipchip type semiconductor die.

An electrically conductive layer 226 is formed over active surface 224 using PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 226 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 226 operates as contact pads electrically connected to the circuits on active surface 224.

An electrically conductive layer 228 is formed over conductive layer 226 using a patterning and metal deposition process such as sputtering, electrolytic plating, and electroless plating. Conductive layer 228 can be Al, Cu, Sn, Ni, Au, Ag, W, or other suitable electrically conductive material. Conductive layer 228 is a UBM electrically connected to conductive layer 226. UBMs 228 can be a multi-metal stack with adhesion layer, barrier layer, and seed or wetting layer. The adhesion layer is formed over conductive layer 226 and can be Ti, TiN, TiW, Al, or Cr. The barrier layer is formed over the adhesion layer and can be Ni, NiV, Pt, Pd, TiW, or CrCu. The barrier layer inhibits the diffusion of Cu into the active area of the die. The seed layer is formed over the barrier layer and can be Cu, Ni, NiV, Au, or Al. UBMs 228 provide a low resistive interconnect to conductive layer 226, as well as a barrier to solder diffusion and seed layer for solder wettability.

An electrically conductive bump material is deposited over conductive layer 228 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing

process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 228 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form balls or bumps 230. In some applications, bumps 230 are reflowed a second time to improve electrical contact to conductive layer 228. Bumps 230 can also be compression bonded or thermocompression bonded to conductive layer 228. Bumps 230 represent one type of interconnect structure that can be formed over conductive layer 228. The interconnect structure can also use stud bump, micro bump, or other electrical interconnect.

Semiconductor die 220 are mounted to substrate 232 using, for example, a pick and place operation with bumps 230 oriented toward the substrate. Substrate 232 includes conductive traces 234 for vertical and lateral interconnect through the substrate. FIG. 9b shows semiconductor die 220 mounted to substrate 232, as reconstituted wafer 236, with bumps 230 metallurgically and electrically bonded to conductive traces 234. Active surface 224 of semiconductor die 220 is held off or offset from substrate 232 by nature of bumps 230, i.e., there is a gap between portion 238 of active surface 224 and substrate 232. Substrate 232 can be a large round or rectangular panel (greater than 300 mm) with capacity for multiple semiconductor die 220.

In FIG. 9c, a mold underfill (MUF) material 240 is deposited over semiconductor die 220 and substrate 232 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, mold

underfill, or other suitable application process. MUF material 240 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. MUF material 240 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. In particular, MUF material 240 is disposed along the sides of semiconductor die 220 and in the gap between active surface 224 and substrate 232 and thus covers the sides of semiconductor die 220 and exposed portion 238 of active surface 224 along the surface edge of the semiconductor die.

In FIG. 9d, semiconductor die 220 are singulated through MUF material 240 and substrate 232 with saw blade or laser cutting tool 239 to separate the semiconductor die and substrate units.

FIG. 9e shows a cross-sectional view of a portion of a carrier or temporary substrate 242 containing sacrificial base material such as silicon, polymer, beryllium oxide, glass, or other suitable low-cost, rigid material for structural support. An interface layer or double-sided tape 243 is formed over carrier 150 as a temporary adhesive bonding film, etch-stop layer, or thermal release layer. Carrier 242 can be a large round or rectangular panel (greater than 300 mm) with capacity for multiple semiconductor die 220 and substrate 232 units.

Semiconductor die 220 and substrate 232 units are mounted to carrier 242 and interface layer 243 using, for example, a pick and place operation with the substrate oriented toward the carrier. FIG. 9f shows semiconductor die 220 and substrate 232 units mounted to interface layer 243 of carrier 242.

An encapsulant or molding compound 244 is deposited over MUF material 240, substrate 232, and carrier 242 using a

paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator. Encapsulant 244 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 244 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants.

In FIG. 9g, carrier 242 and interface layer 243 are removed by chemical etching, mechanical peeling, CMP, mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping to expose substrate 232 and encapsulant 244. A portion of encapsulant 244 is removed by LDA using laser 245. Alternatively, a portion of encapsulant 244 is removed by an etching process through a patterned photoresist layer.

In FIG. 9h, an electrically conductive bump material is deposited over conductive layer 234 of substrate 232 opposite semiconductor die 220 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 234 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form balls or bumps 246. In some applications, bumps 246 are reflowed a second time to improve electrical contact to conductive layer 234. Bumps 246 can also be compression bonded or thermocompression bonded to conductive layer 234. Bumps 246 represent one type of interconnect structure that can be formed over conductive layer 234. The interconnect structure can also

use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

Laser marking can be performed before or after bump formation, or after removal of carrier 242. The assembly undergoes plasma cleaning and flux printing.

Semiconductor die 220 are singulated through encapsulant 244 with saw blade or laser cutting tool 248 into individual eWLB or WLCSP 250. FIG. 10 shows WLCSP 250 after singulation. In one embodiment, WLCSP 250 has dimensions of 3.0 x 2.6 x 0.7 millimeters mm with 0.4 mm pitch. Semiconductor die 220 is electrically connected to substrate 232 and bumps 246 for external interconnect. MUF material 240 covers the sides of semiconductor die 220 and portion 238 of active surface 224 to protect the sides and surface edge of the semiconductor die and increase manufacturing yield, particularly when surface mounting the semiconductor die. MUF material 240 also protects semiconductor die 220 from degradation due to exposure to light. WLCSP 250 undergoes electrical testing before or after singulation.

FIG. 11 illustrates an embodiment of WLCSP 254, similar to FIG. 10, with MUF material 240 disposed under semiconductor die 220 and encapsulant 244 covering the side surfaces of the semiconductor die.

FIG. 12 illustrates another embodiment including semiconductor die 260, from a semiconductor wafer similar to FIG. 3a, having a back surface 262 and active surface 264 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors,

diodes, and other circuit elements formed within active surface 264 to implement analog circuits or digital circuits, such as DSP, ASIC, memory, or other signal processing circuit. Semiconductor die 260 may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing. In one embodiment, semiconductor die 260 is a wire bond type semiconductor die.

An electrically conductive layer 266 is formed over active surface 264 using PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process. Conductive layer 266 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. Conductive layer 266 operates as contact pads electrically connected to the circuits on active surface 264.

Semiconductor die 260 is mounted to substrate 268 with die attach adhesive 270, such as epoxy resin, similar to FIGs. 9a-9b. Substrate 268 includes conductive traces 272 for vertical and lateral interconnect through the substrate. Bond wires 274 are formed between conductive layer 266 of semiconductor die 260 and conductive traces 272 on substrate 268. Substrate 268 can be a large round or rectangular panel (greater than 300 mm) with capacity for multiple semiconductor die 260.

An encapsulant or molding compound 276 is deposited over semiconductor die 260 and substrate 268 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator, similar to FIG. 9c. Encapsulant 276 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 276 is non-conductive and environmentally protects

the semiconductor device from external elements and contaminants.

Semiconductor die 260 are singulated through encapsulant 276 and substrate 268, similar to FIG. 9d. The singulated semiconductor die 260 and substrate 268 are mounted to a carrier, similar to FIG. 9e. An encapsulant or molding compound 278 is deposited over encapsulant 276 and substrate 268 using a paste printing, compressive molding, transfer molding, liquid encapsulant molding, vacuum lamination, spin coating, or other suitable applicator, similar to FIG. 9f. Encapsulant 278 can be polymer composite material, such as epoxy resin with filler, epoxy acrylate with filler, or polymer with proper filler. Encapsulant 278 is non-conductive and environmentally protects the semiconductor device from external elements and contaminants. The carrier is removed.

An electrically conductive bump material is deposited over conductive layer 272 of substrate 268 opposite semiconductor die 260 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and combinations thereof, with an optional flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. The bump material is bonded to conductive layer 272 using a suitable attachment or bonding process. In one embodiment, the bump material is reflowed by heating the material above its melting point to form balls or bumps 280. In some applications, bumps 280 are reflowed a second time to improve electrical contact to conductive layer 272. Bumps 280 can also be compression bonded or thermocompression bonded to conductive layer 272. Bumps 280 represent one type of interconnect structure that can be formed

over conductive layer 272. The interconnect structure can also use bond wires, conductive paste, stud bump, micro bump, or other electrical interconnect.

Laser marking can be performed before or after bump formation, or after removal of the carrier. The assembly undergoes plasma cleaning and flux printing.

Semiconductor die 260 are singulated through encapsulant 244 into individual eWLB or WLCSP 282 having dimensions of 3.0 x 2.6 x 0.7 millimeters mm with 0.4 mm pitch. Semiconductor die 260 is electrically connected to substrate 268 and bumps 280 for external interconnect. Encapsulant 276 covers the side surfaces of semiconductor die 260 to protect the surface edge of the semiconductor die and increase manufacturing yield, particularly when surface mounting the semiconductor die.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

## Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a semiconductor wafer including a plurality of semiconductor die;

forming an insulating layer over the semiconductor wafer;

removing a portion of the insulating layer along a surface edge of the semiconductor die;

forming a conductive layer over the semiconductor wafer;

singulating the semiconductor wafer into the plurality of semiconductor die;

depositing an encapsulant over the semiconductor die to cover a side of the semiconductor die and the surface edge of the semiconductor die after singulating the semiconductor wafer; and

forming a conductive bump on the conductive layer after depositing the encapsulant.

2. The method of claim 1, further including:

providing a carrier;

disposing the semiconductor die over the carrier with the surface edge of the semiconductor die offset from the carrier;

depositing the encapsulant over the semiconductor die and carrier to cover the side of the semiconductor die and the surface edge of the semiconductor die; and

removing the carrier.

3. The method of claim 1, further including depositing the encapsulant after forming the insulating layer.

4. The method of claim 1, further including removing the portion of the insulating layer by laser direct ablation.

5. A method of making a semiconductor device, comprising:
providing a semiconductor die;
forming an insulating layer over the semiconductor die;
removing a portion of the insulating layer along a surface edge of the semiconductor die; and
depositing an encapsulant over the semiconductor die to cover a side of the semiconductor die and the surface edge of the semiconductor die.

6. The method of claim 5, further including:
providing a carrier;
disposing the semiconductor die over the carrier with the surface of the semiconductor die offset from the carrier;
depositing the encapsulant over the semiconductor die and carrier to cover the side and surface edge of the semiconductor die; and
removing the carrier.

7. The method of claim 5, further including forming the insulating layer over the semiconductor die at a wafer level.

8. The method of claim 5, further including forming a conductive layer over the semiconductor die.

9. The method of claim 8, further including forming an interconnect structure over the conductive layer.

10. The method of claim 8, further including depositing the encapsulant over the semiconductor die after forming the conductive layer.

11. The method of claim 5, further including removing the portion of the insulating layer by laser direct ablation.

12. A method of making a semiconductor device, comprising:
providing a substrate;
disposing a semiconductor die over the substrate;
depositing a mold underfill material between the semiconductor die and substrate; and
depositing an encapsulant over a side surface of the semiconductor die and a side surface of the substrate.

13. The method of claim 12, wherein the substrate includes conductive traces for vertical and lateral interconnect.

14. The method of claim 12, further including disposing a conductive bump over the substrate after depositing the encapsulant.

15. The method of claim 12, further including removing a portion of the encapsulant by laser direct ablation (LDA).

16. A method of making a semiconductor device, comprising:
providing a semiconductor die;

forming an insulating layer over the semiconductor die;

forming a conductive layer over the semiconductor die;

depositing an encapsulant over the semiconductor die to cover a side of the semiconductor die after forming the conductive layer; and

disposing a conductive bump directly on the conductive layer after depositing the encapsulant.

17. The method of claim 16, further including:

providing a carrier;

disposing the semiconductor die over the carrier with a surface of the semiconductor die offset from the carrier;

depositing the encapsulant over the semiconductor die and carrier to cover the side of the semiconductor die and a portion of the surface of the semiconductor die; and

removing the carrier.

18. The method of claim 16, further including forming the insulating layer over the semiconductor die at a wafer level.

19. The method of claim 16, further including removing a portion of the insulating layer along a surface edge of the semiconductor die.

20. The method of claim 19, further including removing the portion of the insulating layer prior to depositing the encapsulant.

21. A method of making a semiconductor device, comprising:

providing a semiconductor die;

forming an under bump metallization (UBM) over the semiconductor die;

depositing an encapsulant over a side of the semiconductor die after forming the UBM; and

forming a conductive bump over the UBM after depositing the encapsulant.

22. The method of claim 21, further including:

providing a carrier;

disposing the semiconductor die over the carrier with a surface of the semiconductor die offset from the carrier;

depositing the encapsulant over the semiconductor die and carrier; and

removing the carrier.

23. The method of claim 21, further including forming:

an insulating layer over the semiconductor die; and

removing a portion of the insulating layer along a surface edge of the semiconductor die.