Image Processing Apparatus

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The present invention relates to an image processing apparatus, and more particularly to the encryption of image data.

Fig. 1 shows a block diagram of a configuration of a prior art image encoding apparatus having an encryption function.

Fig. 2 shows a block diagram of an image decoding apparatus for decoding the image data encoded by the apparatus of Fig. 1.

In the encoding apparatus shown in Fig. 1, numeral 110 denotes a high resolution analog video signal (hereinafter referred to as an HD signal), which, in the present example, has the number of scan lines of 1,050 and a frame frequency of 30 Hz. Relative to the HD signal, a video signal of an ordinary resolution having the number of scan lines of 525, a frame frequency of 30 Hz and the number of pixels of 858 is referred to as an SD signal.

An HD A/D conversion circuit 112 samples the video signal 110 at a sampling frequency of 54.054 MHz to convert it to a digital signal. By virtue of the sampling frequency, the number of pixels per line of

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the digital HD signal is 1,716. A high resolution (HD)/ordinary resolution (SD) conversion circuit 114 reduces the number of pixels to one half in both vertical direction and horizontal direction to output a video signal of the ordinary resolution having the number of scan lines of 525, the frame frequency of 30 Hz and the number of pixels per line of 858.

An encoding circuit 116 efficiently encodes the digital SD signal outputted from the conversion circuit 114 by an encoding scheme which is a combination of motion compensated adaptive prediction and DCT. A decoding circuit 118 decodes the encoded signal outputted from the decoded circuit 116 to reproduce an SD signal. An SD/HD conversion signal 120 interpolates pixels to the output video data from the decoding circuit 118 by a factor of two in both vertical direction and horizontal direction to convert it to an HD signal. Namely, the SD/HD conversion circuit 120 outputs a signal corresponding to the high resolution video signal having the number of scan lines of 1,050, the number of pixels per line of 1,716 and the frame frequency of 30 Hz.

A subtractor 122 subtracts the output of the SD/HD conversion circuit 120 from the output of the A/D conversion circuit 112 for each pixel. The output of the subtractor 122 is referred to as an auxiliary video signal. An encoding circuit 124 encodes the

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output of the subtractor 122 in the same encoding scheme as that for the encoding circuit 116.

A multiplexing circuit 126 multiplexes the encoded data (the encoded SD signal) outputted from the encoding circuit 116 and the encoded data (the encoded auxiliary video signal) outputted from the encoding circuit 124 and outputs it to an encryption circuit 128. The encryption circuit 128 encrypts the output of the multiplexing circuit 126 in accordance with an encryption key signal of an encryption key output circuit 130, and an output unit 132 outputs the encrypted data outputted from the encryption circuit 128 to a transmission line. As described above, the transmission line may be a communication line or a recording medium.

The encryption is briefly explained with reference to Figs. 3 and 4. Following encryption techniques are available.

Fig. 3 shows a flow chart of the encryption by the US Data Encryption Standard (DES) published in the FIPS Publication 46 dated January 15, 1977, and Fig. 4 shows a function of the encryption of Fig. 3. The data encryption algorithm of the DES has been published as the "Data Encryption Standard" as described above. Referring to Figs. 3 and 4, the DES will be explained.

The DES handles block encryption to binary data comprising 0's and 1's. In the DES, the binary data is grouped into 64-bit blocks and the transposition and

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the replacement are repeated for each block to encrypt it. An encryption key is a 64-bit signal, of which 8 bits are check bits for detecting an error. Thus, a 56-bit encryption key is actually effective. The replacement of the digit is controlled by the encryption key in each cycle. Fig. 3 shows an encryption process of the DES. Fig. 4 shows a function fK(R) which is a heart of the encryption.

As shown in Fig. 3, a 64-bit plain text is first transpositioned. This is a fixed transposition independent from the encryption key. Then, the 64 bits are divided into a left half L_0 and a right half R_0. Then, the following operations are repeated over the 16 stages:

$$L_n = R_{n-1} \qquad (1)$$

$$R_n = L_{n-1} + fK_n(R_{n-1})$$

where + represents a sum of mode 2 for each bit, L_n and R_n represent the left half 32 bits and the right half 32 bit, respectively, at the end of the operation for the n-th stage, and K_n is generated from the encryption key as shown in the right side of Fig. 3. In Fig. 12, $s_1 \ldots s_{16}$ are 1 or 2.

Condensed transposition is defined as the transposition excluding some of the input. In Fig. 3, 8 bits out of the 56 input bits are excluded so that an output comprises 48 bits. The condensed transposition is irrevocable conversion so that the input cannot be

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perfectly reproduced from the output. This serves to make the estimation of the encryption key difficult.

Referring to Fig. 4, the function fK(R) in Fig. 3 is specifically explained. In Fig. 4, to generate the function fK(R), augmented transposition is made to R. The augmented transposition is defined as the overlapped transposition of some inputs. In the illustrated example, 16 bits out of the 32 input bits appear in overlap at the output. K composed by the key is mode 2 added to the output. The resulting 48 bits are divided into eight 6-bit blocks and the respective 6 bits are converted to 4 bits by S_1, S_2, ..., S_8, respectively. Assuming that the 6 bits constitute one character, it may be considered as a kind of replacement. However, since the output is compressed to 4 bits, the conversion is irrevocable. Accordingly, the fK(R) is generally an irrevocable function. This, however, does not mean that the conversion of the formula (1) is irrevocable. The formula (1) may be converted as follows:

$$\begin{aligned} R_{n-1} &= L_n \\ L_{n-1} &= R_n + fK_n(R_{n-1}) \\ &= R_n + fK(L_n) \end{aligned} \qquad (2)$$

It is thus seen that L_{n-1} and R_{n-1} can be calculated from L_n and R_n.

The calculation of the formula (1) is repeated 16 times and when L_{16} and R_{16} are determined, they are

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finally transpositioned again and the encryption is terminated.

In a decoding apparatus shown in Fig. 2, a transmission data input unit 140 receives the data from the transmission line and supplies it to a decryption circuit 142. The decryption circuit 142 decrypts it by utilizing the encryption key signal outputted from the encryption key output circuit 144. In order for the decryption to be correctly done, the exactly same encryption key as that outputted from the encryption key output circuit 130 used in the encoding apparatus (see Fig. 1) should be used.

The decryption is substantially a reverse operation to the encryption. Briefly, the process proceeds from the bottom to the top in Fig. 3. First, a reverse transposition to the last transposition in the encryption is made, and R_{n-1} and L_{n-1} are determined from the formula (2), and when R_0 and L_0 are determined, a reverse transposition to the first transposition in the encryption is made. In this manner, the original 64 bits are reproduced. In order to decrypt the DES encrypted text, there has been no known method other than examining the keys one by one. Assuming that one microsecond is needed to examine if one key is correct one or not, 2,283 years will be needed to examine all of 2^{56} keys.

The transmission data decrypted by the decryption

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circuit 142 is separated by a separation circuit 146 to encoded data of the SD signal and encoded data of the auxiliary video signal, which are supplied to decoding circuits 148 and 150, respectively. The decoding circuit 148 outputs the reproduced SD signal and the decoding circuit 150 output the reproduced auxiliary video signal.

An SD A/D conversion circuit 152 converts the digital SD signal outputted from the decoding circuit 148 to an analog signal. The output of the SD A/D conversion circuit 152 is an analog video signal having the number of scan lines of 525 and the frame frequency of 30 Hz. This video signal is applied to a monitor device of an ordinary resolution to display the image.

An SD/HD conversion circuit 154 converts the digital SD signal outputted from the decoding circuit 148 to a digital HD signal in the same process as that of the SD/HD conversion circuit 120. An adder 156 adds the output of the decoding circuit 150 and the output of the SD/HD conversion circuit 154. The output of the adder 156 is a video signal corresponding to the high resolution video signal. An HD D/A conversion circuit 158 converts the digital output of the adder 156 to an analog signal. The output of the HD D/A converter 158 is a video signal having the number of scan lines of 1,050 and the frame frequency of 30 Hz. The video signal is applied to a high resolution monitor

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to display the image.

The above prior art video signal encoding and decoding apparatus has a problem in that the video signal cannot be reproduced for those who do not have the encryption key, for both the low resolution video signal and the high resolution video signal.

There is a demand that charges to users are discriminated between the low resolution display device having the number of scan lines of 525 and the high resolution display device having the number of scan lines of 1,050, for the same content, but the prior art apparatus does not meet the requirement.

In a first aspect the present invention provides an image processing apparatus which permits the reproduction as usual for an image having a lower resolution than a predetermined level and permits the reproduction of an image having a higher resolution by conducting a predetermined process.

In one embodiment, the image processing apparatus comprises separation means for separating input image data into low resolution image data and one or more auxiliary image data for interpolating the low resolution image data, and encryption means for encrypting at least one auxiliary data.

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In another preferred embodiment, the image processing apparatus for separating the input image data into the low resolution image data and the one or more auxiliary image data for interpolating the low resolution image data and decoding the image data having at least one auxiliary image data encrypted comprises decryption means for decrypting the encrypted auxiliary image data, and synthesization means for synthesizing the low resolution image data and the auxiliary image data.

Other aspects features and advantages of the invention will become apparent from the following detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a block diagram of a prior art image encoding apparatus,

Fig. 2 shows a block diagram of a prior art image decoding apparatus,

Fig. 3 shows a flow of prior art encryption,

Fig. 4 shows a flow of prior art decryption,

Fig. 5 shows a block diagram of a configuration of one embodiment of an image encoding apparatus of the present invention,

Fig. 6 shows a block diagram of a configuration of an embodiment of an image decoding apparatus of

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the present invention,

Fig. 7 shows a block diagram of a modified portion of a configuration of a modified embodiment of Fig. 6,

Fig. 8 shows a block diagram of a modified portion of a modified embodiment of Fig. 6,

Fig. 9 shows a block diagram of a configuration of a second embodiment of the image encoding apparatus of the present invention,

Fig. 10 shows a block diagram of a configuration of a second embodiment of the image decoding apparatus of the present invention,

Fig. 11 illustrates band division of a space frequency,

Fig. 12 shows a block diagram of a configuration of a modified portion of a modified embodiment of Fig. 10,

Fig. 13 shows a block diagram of a configuration of a modified portion of a modified embodiment of Fig. 10,

Fig. 14 shows a block diagram of a specific encoding circuit of the embodiment, and

Fig. 15 shows a block diagram of a specific decoding circuit of the embodiment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Fig. 5 shows a block diagram of a configuration

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of one embodiment of the encoding apparatus of the present invention, and Fig. 6 shows a block diagram of a configuration of the decoding apparatus.

The encoding apparatus shown in Fig. 5 is first explained. Numeral 10 denotes a high resolution video signal having the number of scan lines of 1,050 and the frame frequency of 30 Hz as the HD signal 110 does. Numeral 12 denotes an HD A/D conversion circuit for converting the video signal 10 to a digital signal, numeral 14 denotes a high resolution (HD)/ordinary resolution (SD) conversion circuit for converting the digital HD signal outputted from the HD A/D conversion circuit 12 to a video signal of the ordinary resolution, numeral 16 denotes an encoding circuit for efficiently encoding the output of the conversion circuit 14, numeral 18 denotes a decoding circuit for decoding the output of the encoding circuit 16, numeral 20 denotes an SD/HD conversion circuit for interpolating the SD signal output of the decoding circuit 18 to convert it to an HD signal, numeral 22 denotes a subtractor for subtracting the output of the SD/HD conversion circuit 20 from the output of the HD A/D conversion circuit 12 for each pixel, and numeral 24 denotes an encoding circuit for encoding the output of the subtactor 22. The circuits 12 - 24 have the same functions as those of the circuits 112 - 124 of Fig. 1 and operate in the same manner.

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Numeral 26 denotes an encryption circuit for encrypting the output of the encoding circuit 24 in accordance with an encryption signal outputted from an encryption key output circuit 28. As the encryption technique, the one which complies with the DES standard is used.

Numeral 30 denotes a multiplexing circuit for multiplexing the output of the encoding circuit 16 and the encryption circuit 26, and numeral 32 denotes an output unit for outputting transmission data multiplexed by the multiplexing circuit 30 to a transmission line such as a communication line or a recording medium.

The encoding apparatus shown in Fig. 5 is explained. The operations of the circuits 12 - 24 are same as those of the prior art apparatus. Namely, the encoding circuit 16 outputs the encoded data of the video signal derived by converting the HD signal 10 to the ordinary resolution, and the encoding circuit 24 outputs the encoded data of the auxiliary video signal to reproduce the high resolution video signal from the transmission video data of the ordinary resolution. In the present embodiment, prior to the multiplexing of the both encoded data, the output encoded data of the encoding circuit 24 is encrypted by the encryption circuit 26 by using the encryption key signal outputted from the encryption key output circuit 28 and it is applied to the multiplexing circuit 30.

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applied to the encoded data of the auxiliary video signal by using the same encryption key signal outputted from the encryption key output circuit 46 as the encryption key signal outputted from the encryption key output circuit 28 of the encoding circuit (Fig. 1). The encoded data of the auxiliary video signal decrypted by the decryption circuit 44 is applied to the decoding circuit 50 and decoded thereby.

Thus, the decoding circuit 48 outputs the reproduced digital SD signal and the decoding circuit 50 outputs the reproduced digital auxiliary video signal.

The SD D/A conversion circuit 52 converts the digital SD signal outputted from the decoding circuit 48 to an analog signal. The SD D/A conversion circuit 52 may be an analog signal having the number of scan lines of 525 and the frame frequency of 30 Hz and the video signal is applied to a monitor device of the ordinary resolution to display the image.

The SD/HD conversion circuit 54 converts the digital SD signal outputted from the decoding circuit 48 to a digital signal in the same process as that of the SD/HD conversion circuit 120. The adder 56 adds the output of the decoding circuit 50 to the output of the SD/HD conversion circuit 54 for each pixel. The output of the adder 56 is a video signal corresponding to the high resolution video signal. The HD D/A conversion circuit 58 converts the digital output of

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the adder 56 to an analog signal. The output of the HD D/A conversion circuit 58 is a high resolution video signal having the number of scan lines of 1,050 and the frame frequency of 30 Hz and it may be applied to a high resolution monitor to display the image.

In the decoding apparatus shown in Fig. 6, without the encryption key or if the encryption key is not correct (hereinafter collectively referred to as without key or no key state), the decryption circuit 44 outputs quite an unstable data pattern so that the output of the HD D/A conversion circuit 58 is also unstable and an unstable pattern such as a noise image is displayed on the screen of the display device such as a CRT.

Alternatively, a fixed image may be displayed on the high resolution monitor screen in the no key state. Figs. 7 and 8 show portions of block diagrams of such modified encoding apparatus. The like elements in Figs. 7 and 8 are designated by like numerals.

In Fig. 7, a switch 60 is provided between the decoding circuit 50 and the adder 56, and when the no key state (no input of the encryption key signal) is detected by the decryption circuit 44, the switch 60 is set to '0' by the detection output so that '0' is applied to the adder 56. When the correct encryption key is inputted to the decryption circuit 44', the decryption circuit 44' connects the switch 60 to the

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output of the decoding circuit 50.

In Fig. 8, a switch 62 is provided between the adder 56 and the HD D/A conversion circuit 58 so that in the no key state a predetermined level is inputted to the HD D/A conversion circuit 58. The switch 62 normally selects the output of the adder 56, and when the decryption circuit 44' the no key state (no input of the encryption key signal), the switch is set to the predetermined level input. In this manner, when the correct input is present, the high resolution video signal is outputted but in the no key state, the predetermined level signal is outputted and an image corresponding to the predetermined level is displayed on the monitor screen.

In Figs. 7 and 8, the switches 60 and 62 are illustrated to facilitate the understanding although it is apparent that the function of such switches 60 and 62 may be incorporated in the decoding circuit 50 and/or HD A/D conversion circuit 58. Alternatively, the output of the decoding circuit 50 or the HD D/A conversion circuit may be forced to a predetermined level (for example, zero output) in response to the detection of the no key state by the decryption circuit 44.

In Figs. 7 and 8, the no key state is detected by the decryption circuit 44 although it may be detected by error code detection or error correction process.

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A second embodiment of the present invention which is applied to a system in which the image information is transmitted by the band division by the space frequency is now explained. Fig. 9 shows a block diagram of a configuration of an encoding apparatus thereof, and Fig. 10 shows a block diagram of a configuration of a decoding apparatus. Fig. 11 illustrates the band division of the space frequency.

Numeral 210 denotes an analog HD signal to be encoded. In the present embodiment, it is a video signal having the number of scan lines of 1,050 and the frame frequency of 30 Hz. An HD A/D conversion circuit 212 samples the analog HD signal at a sampling frequency of 54.054 MHz to convert it to a digital signal. The number of pixels per line of the sampled HD signal is 1,716.

The output of the HD A/D conversion circuit 212 is applied to band division filters 214 and 216 and divided by the filters 214 and 216 to a low frequency component and a high frequency component at a horizontal frequency and the number of pixels is reduced to one half, respectively.

The output of the band division filter 214 is a low resolution component of the horizontal frequency, which is further separated into a low frequency component and a high frequency component at a vertical frequency by band division filters 218 and 220 to reduce

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the number of pixels to one half. Similarly, the band division filters 222 and 224 separates the output of the band division filter 216 (the high resolution component at the horizontal frequency) into a low frequency component and a high frequency component at the vertical frequency to reduce the number of pixels to one half.

In this manner, the high resolution video signal having 1,716 pixels in the horizontal direction and 1,024 pixels in the vertical direction is separated into an LL signal (the output of the band division filter 218), an LH signal (the output of the band division filter 220), an HL signal (the output of the band division filter 222) and an HH signal (the output of the band division filter 224) having one half of the total number of pixels in the horizontal direction and the vertical direction, as shown in Fig. 11. Since only the LL signal has the low-pass data in both the horizontal direction and the vertical direction, it is the video information which can be reproduced for display as the image and corresponds to the video signal of the ordinary resolution having the number of scan lines of 525, the frame frequency of 30 Hz and the number of pixels per line of 858. On the other hand, since the LH signal, the HL signal and the HH signal are high-pass data, they cannot be displayed as the image as they are and they are the auxiliary video signals which

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form the high resolution video signal in cooperation with the LL signal.

The encoding circuit 226 efficiently encodes the output of the band division filter 218 (LL signal) by an encoding scheme which is a combination of the motion compensated adaptive prediction known as the CCIR Recommendation 723 and the DCT. Encoding circuit 228, 230 and 232 efficiently encode the outputs of the band division filters 220, 222 and 224 (LH signal, HL signal and HH signal), respectively, by a combination of the DPCM and a zero run length encoded and variable length code. The outputs of the encoding circuits 228 - 232 are multiplexed by a multiplexing circuit 234. An encryption circuit 236 encrypts the output of the multiplexing circuit 234 by using the encryption key outputted from the encryption key output circuit 238 in accordance with the encryption technique of the DES standard described above.

The multiplexing circuit 240 multiplexes the output of the encoding circuit 226 and the output of the encryption circuit 236 and the output thereof is outputted to the transmission line by the output unit 242.

In the decoding apparatus shown in Fig. 10, the transmission data input unit 250 receives the transmission data from the transmission line and applies it to the separation circuit 252. The separation

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circuit 252 separates it into a portion related to the encoded data of the LL signal and a portion related to the other LH, HL and HH signals, and applies the former to the decoding circuit 254 and the latter to the decryption circuit 256. The decryption circuit 256 decrypts the encoded data of the LH, HL and HH signals by using the encryption key signal outputted from the encryption key output circuit 258. In order to correctly decrypt it, the encryption key should be same as that used for encoding the encryption key signal.

The separation circuit 260 separates the output of the decryption circuit 256 to the encoded data of the LH signal, the encoded data of the HL signal and the encoded data of the HH signal, which are applied to the decoding circuits 262, 264 and 266, respectively.

The decoding circuits 254, 262, 264 and 266 decode the encoded data inputted thereto, respectively. The output of the decoding circuit 254 is the LL signal. The SD D/A conversion circuit 268 converts the output of the decoding circuit 254 to an analog signal. The output of the SD D/A conversion circuit 268 is an analog video signal having the number of scan lines of 525 and the frame frequency of 30 Hz and it can be displayed as an image by an image display device of the ordinary resolution.

The reproduced LL signal and LH signal are combined at the vertical frequency by the band

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synthesization filters 270 and 272 and the number of pixels in the vertical direction is interpolated to two times. Similarly, the reproduced HL signal and HH signal are synthesized at the vertical frequency by the band synthesization filters 274 and 276 and the number of pixels in the vertical direction is interpolated to two times. The synthesized signals are combined at the horizontal frequency by the band synthesization filters 278 and 280 and the number of pixels in the horizontal direction is interpolated to two times.

By those synthesization processes, the digital high resolution video signal having the number of scan lines of 1,050 and the frame frequency of 30 Hz is reproduced. The HD D/A conversion circuit 282 converts the reproduced digital HD signal to an analog signal.

In the decoding apparatus shown in Fig. 10, in the no key state, the decryption circuit 256 outputs a quite unstable data pattern so that the output of the HD D/A conversion circuit 282 is also unstable and an unstable pattern such as a noise image is displayed on the screen of the display device such as CRT.

Alternatively, the image of the low resolution or a still image may be displayed on the high resolution monitor screen in the no key state. Figs. 12 and 13 show portions of block diagrams of such modified decoding apparatus. The like elements to those of Fig. 10 are

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designated by the like numerals.

In Fig. 12, an SD/HD conversion circuit 284 for converting the output of the decoding circuit 254 to the HD signal and a selection switch for selecting the output of the SD/HD conversion circuit 284 or the synthesized output by the band synthesization filters 278 and 280 and supplying it to the HD D/A conversion circuit 282 are provided. The SD/HD conversion circuit 284 is identical to the SD/HD conversion circuit 54 of Fig. 6. The switch 286 is normally connected to synthezied output of the band synthesization filters 278 and 280, and when no key state is detected by the decryption circuit, it is switched to the output of the SD/HD conversion circuit 284 by the detection output. Thus, in the no key state, the image can be displayed by the high resolution monitor although the quality of the image is not sufficient for the high resolution monitor.

When the encryption key signal may not be inputted to the decryption circuit 256', it may be possible that the output of the encryption key output circuit 258 is forcibly stopped or the encryption key output circuit 258 itself is not present.

For the configuration shown in Fig. 12, the high frequency data of the band synthesization filters 270 - 280 may be reset by the detection output of the decryption circuit 256' to attain the same effect.

In Fig. 13, a switch 282 is provided between

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synthesized output by the band synthesization filters 278 and 280 and the HD D/A conversion circuit 282 so that in the no key state, a predetermined level is inputted to the HD D/A conversion circuit 282. The switch 288 normally selects the synthesized output by the band synthesization filters 278 and 280, and when the no key state is detected by the decryption circuit 256, it is switched to the predetermined level input by the detection output. In this manner, when the correct encryption key is present, the high resolution video signal is outputted, but in the no key state, the predetermined level signal is outputted and the image corresponding to the predetermined level is displayed on the monitor screen.

When the encryption key signal is not inputted to the decryption circuit 256', it may be possible that the output of the encryption key output circuit is forcibly stopped or the encryption key output circuit 258 itself is not present.

For the configuration shown in Fig. 13, the switch 288 may not be provided and the output of the HD D/A conversion circuit 282 may be forced to a constant level (for example, zero output) in accordance with the detection output of the no key state by the decryption circuit 44.

In Figs. 12 and 13, the no key state is detected by the decryption circuit 256 although it may be detected by

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an error detection code or error correction process.

Embodiments of the encoding circuit and the decoding circuit used in the respective embodiments are now explained.

Fig. 14 shows a block diagram of a specific embodiment of the encoding circuit.

The encoding circuit shown in Fig. 14 comprises a blocking circuit 301, ADCT circuit 302, a quantization circuit 303, a variable length encoding circuit (VLC) 304, a motion compensation circuit 305, a motion vector detection circuit 306, a rate control circuit 307, a local decoding circuit 308 and a buffer memory 309.

In Fig. 14, image data to be encoded is grouped into 8 x 8 pixel blocks by the block forming circuit 301 and they are supplied to the DCT (discrete cosine transform) circuit 302 through the switch 310.

The switch 310 is periodically (for example, for each frame or every several fields) switched to a terminal a to prevent erroneous propagation.

Namely, when it is connected to the terminal a, an intra-frame or intra-field encoding (intra mode) is conducted.

In the intra mode, it is DCT-transformed by the DCT circuit 302 and the resulting DCT coefficient is quantized by the quantization circuit 303 and further encoded by the variable length encoding circuit 304 and temporarily stored in the buffer 309.

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On the other hand, in other than the intra mode, the switch 310 is connected to a terminal b to conduct the motion compensated prediction encoding.

Numerals 311 and 312 denote a de-quantization circuit and a de-DCT circuit which constitute the local decoding circuit 308. The data quantized by the quantization circuit 303 is restored to the original image data by the local decoding circuit 308.

Numeral 313 denotes an adder, numeral 314 denotes a switch which is closed in other than the intra mode, and numeral 316 denotes a subtractor.

The locally decoded image data refers the motion vector detected by the motion vector detection circuit 306 to output the corresponding block of the predetermined frame (preceding frame, succeeding frame or interpolated frame).

The output of the motion compensation circuit 305 is subtracted by the input image data by the subtractor 316 to produce a difference.

The difference is encoded by the DCT circuit 302, the quantization circuit 303 and the variable length encoding circuit 304 and it is stored in the buffer 309.

The motion vector detection circuit 306 compares the frame data to be encoded with the predetermined reference frame data to produce the motion vector, and the output of the motion vector

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detection circuit 306 is supplied to the motion compensation circuit 305 to specify the block to be outputted by the motion compensation circuit 305.

The rate control circuit 307 controls the quantity of encoding by switching the quantization step of the quantization circuit 303 in accordance with an occupation rate of the encoded data in the buffer 309.

Finally, the motion vector data detected by the motion vector detection circuit 306, an encoding identification code for identifying the intra mode and quantization step data indicating the quantization step are added by an adding circuit 315 and it is outputted as the encoded data.

Fig. 15 shows a specific block diagram of the decoding circuit.

The decoding circuit basically operates in the reverse manner to the encoding circuit shown in Fig. 14.

The decoding circuit shown in Fig. 15 comprises an input buffef memory 401, a variable length decoding circuit 402, a de-quantization circuit 403, a de-DCT circuit 404, a motion compensation circuit 405 and an output buffer memory 406.

The encoded data sequentially read from the input buffer memory 401 is processed by the variable length decoding circuit 402, the de-quantization circuit 403 and the de-DCT circuit 404 and converted to the space area data.

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The quantization step of the de-quantization circuit 403 is determined by the quantization step data which is transmitted along with the encoded data.

Numeral 407 denotes an adder for adding the output of the de-DCT circuit 404 to the difference outputted from the motion compensation circuit 405, and numeral 408 denotes a switch for selecting the output of the de-DCT circuit 404 or the output of the adder 407.

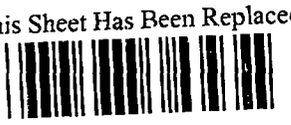
The switch 408 is connected to the terminal a in the intra mode by the encoding identification code detected by the data detection circuit, not shown, and connected to the terminal b in other mode.

The decoded data is temporarily stored in the output buffer memory 406 and restored to the original space arrangement and outputted as one-frame or one-field image data.

As will be readily understood from the above description, in accordance with the present embodiment, the high resolution video signal is not reproduced for those who do not have the encryption key and the reproduction of only the low resolution video signal is permitted. The charges to the users may be discriminated between the display device of the low resolution and the display device of the high resolution of the same content.

The present invention may be implemented in other various forms without departing from the spirits and

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the principal features.

For example, while the image signal is divided into four frequency bands in the second embodiment, the present invention is not limited thereto.

In other words, the foregoing description of the embodiments has been given for illustrative purpose only and not to be construed as imposing limitation in every respect.

The scope of the invention is, therefore, to be determined solely by the following claims and not limited by the text of the specification and alterations made within the scope equivalent to the scope of the claims fall within the true spirit and scope of the invention.

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WHAT IS CLAIMED IS:

1. An image processing apparatus comprising:

a) input means for inputting an image signal;

b) division means for dividing the image signal inputted from said input means to a plurality of frequency band signal groups; and

c) encryption means for encrypting at least one of the signal groups divided by said division means.

2. An image processing apparatus according to Claim 1, further comprising:

encoding means for encoding the signal groups divided by said division means.

3. An image processing apparatus according to Claim 2, wherein said encoding means conducts block encoding by using orthogonal transform.

4. An image processing apparatus according to Claim 2, further comprising:

multiplexing means for multiplexing the encoded signal groups.

5. An image processing apparatus comprising:

a) input means for inputting an image signal;

b) conversion means for converting the image signal inputted from said input means to a plurality of

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image signals of different resolutions; and

c) encryption means for encrypting at least one of the image signals converted by said conversion means.

6. An image processing apparatus according to Claim 5, further comprising:

encoding means for encoding the image signals converted by said conversion means.

7. An image processing apparatus according to Claim 6, wherein said encoding means conducts block encoding by using orthogonal transform.

8. An image processing apparatus according to Claim 6, further comprising:

multiplexing means for multiplexing the encoded image signals.

9. An image processing apparatus for dividing an image signal into a plurality of frequency band signal groups and decoding the divided signal groups with at least one of the signal groups being encrypted, comprising:

a) decryption means for decrypting the encrypted signal group and

b) synthesization means for synthesizing the

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signal group decrypted by said decryption means with other signal groups.

10. An image processing apparatus according to Claim 9, wherein said signal groups are encoded and said image processing apparatus further comprises decoding means for decoding the encoded signal groups.

11. An image processing apparatus according to Claim 9, wherein the output of the encrypted signal group is inhibited when said decryption means cannot decrypt the encrypted signal group.

12. An image processing apparatus according to Claim 9, wherein a predetermined signal is produced in lieu of the encrypted signal group when said decryption means cannot decrypt the encrypted signal group.

13. An image processing apparatus for dividing an input image signal into a plurality of image signals of different resolutions and decoding the divided image signals with at least one of the image signals being encrypted, comprising:

a) decryption means for decrypting the encrypted image signal; and

b) synthesization means for synthesizing the image signal decrypted by said decryption means with

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other image signals.

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14. An image processing apparatus according to Claim 13, wherein said image signals are encoded and said image processing apparatus further comprises decoding means for decoding the encoded image signals.

15. An image processing apparatus according to Claim 13, wherein the output of the encrypted image signal is inhibited when said decryption means cannot decrypt the encrypted image signal.

16. An image processing apparatus according to Claim 13, wherein a predetermined signal is produced in lieu of the encrypted image signal when said decryption means cannot decrypt the encrypted image signal.

17. An image processing apparatus comprising:

a) separation means for separating input image data into low resolution image data and one or more auxiliary image data for interpolating said low resolution image data; and

b) encryption means for encrypting at least one of the auxiliary image data.

18. An image processing apparatus according to Claim 17, further comprising:

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encoding means for encoding the image data separated by said separation means.

19. An image processing apparatus according to Claim 17, further comprising:

synthesization means for synthesizing the image data encoded by said encoding means.

20. An image processing apparatus for separating input image data into low resolution image data and one or more auxiliary image data for interpolating said low resolution image data and decoding the image data with at least one of the auxiliary image data being encrypted, comprising:

a) decryption means for decrypting the encrypted auxiliary image data; and

b) synthesization means for synthesizing the low resolution image data with the auxiliary image data.

21. An image processing apparatus according to Claim 20, wherein said low resolution image data and said auxiliary image data are encoded, and said image processing apparatus further comprises decoding means for decoding the encoded low resolution image data and auxiliary image data.

22. An image processing apparatus according to

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Claim 20, wherein the output of the encrypted auxiliary image data is inhibited when said decryption means cannot decrypt the encrypted image data.

23. An image processing apparatus according to Claim 20, wherein a predetermined signal is outputted in lieu of the encrypted auxiliary image data when said decryption means cannot decrypt the encrypted image data.

24. An image processing apparatus comprising:

a) separation means for separating input image data into low resolution image data and one or more auxiliary image data for interpolating said low resolution image data; and

b) mask means for masking at least one of the auxiliary image data.

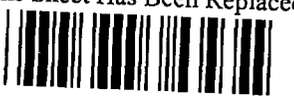
25. An image processing apparatus according to Claim 24, further comprising:

encoding means for encoding the image data separated by said separation means.

26. An image processing apparatus according to Claim 24, further comprising:

synthesization means for synthesizing the image data encoded by said encoding means.

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27. A video transmission system wherein one or more auxiliary video signals are transmitted with a basic video signal, so as to enable reproduction of basic quality images or higher quality images, wherein the or each auxiliary signal is subjected to encryption independently of the basic signal.

28. A record carrier or signal conveying video information, wherein images are encoded at a basic quality level and a higher quality level by means of basic and auxiliary signal components, and wherein at least one auxiliary signal component is encrypted independently of the basic signal component.