SURFACE ROUGHENING PROCESS

DESCRIPTION

TECHNICAL FIELD AND PRIOR ART

The invention relates to the field of microstructure manufacturing as well as the treatment of substrates in semiconductor materials.

In microelectronics, certain operations, such as bonding operations, require that the surfaces to be bonded are as smooth as possible. But the manufacturing of certain devices, particularly types implementing a membrane or mobile part, may necessitate having recourse to surfaces that face each other but that cannot adhere to each other, in order to be able to justly prevent ill-timed bondings of the membrane on the facing surface and to be able to maintain mobility of this membrane.

Therefore document FR 2 857 953 discloses such a process for manufacturing BSOI type structures in which a so-called structured zone is made, preventing bonding to another surface. This type of structure finds interest in the MEMS field, and more particularly in the case where the superficial silicon membrane must be released to manufacture sensors.

During the membrane release step, a step which comprises for example an underlying oxide attack, or during operation of the sensor, this membrane happens to bond to the substrate, thereby inducing dysfunction of the component.

As explained in the document above, a BSOI substrate that comprises a rough buried interface avoids this problem; the roughness of the buried interface prevents any bonding between the membrane and the support.

In document FR 2 857 953, roughening of the surface implements various techniques, for example mechanical and/or chemical thinning (mechanical-chemical polishing, grinding, TMAH or HF/HNO_3 etching). These techniques may create defects on the surface of the semiconductor substrate (and even in the depth of the substrate in the case of grinding) that may generate defects on the specific BSOI antisticking substrate during manufacturing (for example bonding defects or structural defects in the SOI layer). In the case where the roughened substrate is thinned to become the active layer, these defects may interfere with the fabrication of certain types of components.

Roughening may also be done by deposition of a non-monocrystalline material, which is therefore different from the monocrystalline substrate. The material deposited then has physical properties, for example thermal and/or electrical conductivity, that are different from those of the starting substrate and which also may interfere with certain applications.

Therefore the problem is posed of finding another process that allows a rough surface to be made on a substrate without increasing the density of defects on the initial substrate and without modifying its main physical characteristics.

DISCLOSURE OF THE INVENTION

The present invention allows a first monocrystalline semiconductor substrate with a roughened surface to be manufactured. This first roughened substrate is a homogeneous material presenting a very low density of defects, identical to that of the starting substrate (of monocrystalline Si for example).

This roughened substrate may then be used for making antisticking structures, that is, BSOI structures having a roughened buried interface.

The invention particularly relates to a process for forming a rough interface or topology in a semiconductor substrate comprising:

- the formation, on a surface of said substrate, of a zone of irregularities in a material that may be oxidized and/or does not shield thermal oxidation,
- the formation of a rough interface in the semiconductor substrate by thermal oxidation of, or through, this material and a part of the semiconductor substrate.

According to the present invention, a material having a topology or roughness of amplitude greater than the initial topology or roughness of said substrate surface is deposited or formed on a surface of the first substrate, then this material and at least a part of the substrate is oxidized, or a part of this substrate through this material is oxidized.

The oxidation step may be a dry or wet oxidation step at temperatures between 950° C and 1200° C.

The conditions of the oxidation step are adapted in such a way as to allow the material added on the first substrate to be oxidized at least entirely. The oxidation front also preferentially reaches the substrate.

According to an embodiment, a homogeneous or heterogeneous layer is formed on the first substrate, this layer being rough and having a thickness d for example of between 100 nm and 1 µm. This layer is not an oxidation barrier. The substrate is for example in a semiconductor material such

as silicon, and the layer is then, for example, in polycrystalline silicon.

The initial surface topology or roughness of the material or layer formed on the surface of the first substrate is transferred to the substrate by oxidation of this material or this layer, or by oxidation through this material (if it is an oxide, for example).

The total consumption by oxidation of the layer deposited will allow defects, particularly crystalline defects, to be eliminated from the p-Si layer deposited. The oxidation front then reaches the initial substrate. Therefore with a superficial oxide (for example from the consumption of poly-Si material and part of the substrate) and an initial Si substrate (preferably monocrystalline) the density of defects is identical or comparable to that of the starting substrate. The oxide/silicon interface is rough, the surface roughness of the material deposited having been transferred during the advance of the oxidation front.

The oxide may then possibly be withdrawn and a new oxide deposition or a new oxidation may be carried out on the rough surface of the substrate.

The initial oxide or new oxide may therefore undergo mechanical-chemical polishing in the perspective of bonding by molecular adhesion.

Assembly with another substrate having undergone treatment according to the invention or with an untreated bulk substrate may then be carried out. In both cases a part of the assembly, for example one of the two substrates assembled, may then be treated, for example by thinning.

The roughness or topology may be formed by the deposition of a silicon oxide layer or a layer of polysilicon or amorphous silicon.

According to yet another embodiment, roughness or topology may be induced by the deposition of particles on the surface of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

- Figures 1A-1C represent an embodiment of the invention.
- Figures 2A-2B and 3A-3B represent another embodiment of the invention.
- Figures 4A-4C illustrate two other embodiments of the invention.
- Figures 5A and 5B represent the assembly of a substrate according to the invention with another substrate.
- Figures 6A and 6B represent the assembly of two substrates according to the invention.
- Figure 7 represents a substrate according to the invention in which the oxide layer was eliminated and then replaced by another oxide layer.
- Figures 8 and 9 represent devices without roughness (Figure 8) and the corresponding bonding problems, and with roughness (Figure 9).

DETAILED DISCLOSURE OF PARTICULAR EMBODIMENTS

According to the invention, substrate 2 is selected in a first semiconductor and monocrystalline material, whose surface 4 presents a roughness equal to R1 (Figure 1A).

A second material 6 is then formed or deposited on the surface of this substrate. The surface of this material presents a roughness R2 relative to the type of layer

deposited and to the deposition technique utilized. This roughness R2 is greater than roughness R1 of substrate 2. The roughness comes from differences in altitude or levels (following an axis z perpendicular to the surface 4 of the substrate), between the high zones and low zones of the surface of the second material 6. The roughness presents an altitude profile wherein the maximum amplitude (this is for example a certain roughness) R2 is greater than roughness R1 of substrate 2, when the roughnesses are compared at the same frequency (high or low frequency).

Then thermal oxidation is performed. According to the nature of the second material 6, the oxidation front will oxidize it entirely, or cross it entirely (if it has already been oxidized), and at least partially transfer the topology and roughness profile in the initial bulk substrate 2.

At the end of this oxidation, the topology or roughness of the second material 6, transferred in the substrate 2, will either be maintained or reduced but will remain greater than the initial roughness R1 of surface 4.

This will have the consequence of generating a rough interface 12 between the thermal oxide 10 generated by thermal oxidation and the substrate 2 (Figure 1C).

If the layer is not initially an oxide, the layer 6, deposited on substrate 2 and possibly part of the substrate, will have been entirely transformed during oxidation. If layer 6 is an oxide (it is for example silicon oxide), oxidation will have transferred the roughness or topology of the surface in substrate 2, part of the latter being, in addition, oxidized.

According to an embodiment of the invention illustrated in Figures 1A-1C, a starting substrate 2, for example in

silicon, is selected. A deposition 6 is formed on the surface 4 of substrate 2. This deposition is for example in polysilicon or amorphous silicon. The roughness R2 of this deposition 6, on the order of several nm of AFM RMS, for example between 1 nm and 10 nm, for example even for 5 μm x 5 μm scan windows, is adapted for making "antisticking" structures.

The oxidation step is then done. In the case of the deposition of a layer 6 in polycrystalline or amorphous silicon, a thickness e of thermal oxide 10 is preferably formed (Figure 1C) that is greater than or equal to:
$E=d/0.44$

This thickness corresponds to the thermal oxide 10 thickness allowing all of layer 6 deposited on surface 4 to be oxidized.

At the end of this oxidation step, the oxidation front 12 or oxide–substrate interface is substantially at a depth of $d/0.44$ under surface 8, or in the substrate 2 itself (therefore at a depth, under surface 8, that is greater than $d/0.44$).

This front or interface has a final topology or surface roughness R3 equal to or substantially less than R2, but greater than R1. This roughness R3 is sufficient so that, if a membrane is positioned facing this roughness surface R3 and comes in contact with the surface, adhesion of the membrane on this surface, that would obstruct mobility of the membrane, cannot be achieved.

The roughness R3 of interface 12 may be adapted: the roughness of surface R2 of the deposited material 6 is all the higher given that the thickness deposited is large. In addition, generation of thermal oxide with higher thickness tends to reduce roughness before the oxidation front.

Therefore, by exploiting the 2 parameters that are the thickness d of deposition 6 and the oxidation thickness, it is possible to control the final roughness R3 of the buried interface 12, the oxide/silicon interface in the example given. These considerations remain valid if layer 6 is already an oxide layer.

The thickness d of layer 6 may vary by several or dozens of nm to several µm, for example from 5 nm to 3 µm.

One may give the example of the following experimental conditions:

- thickness of polycrystalline silicon d = 400 nm,
- e = 1.2 µm,
- temperature during oxidation: 1100° C,
- final roughness of the buried interface: 3 nm RMS, in a scan of 5x5 µm.

According to another embodiment of the invention, illustrated in Figures 2A, 2B, and 3A, 3B, a deposit of beads or particles (not necessarily of spherical form) 14, 14' in silica or silicon for example is made on the surface of substrate 2. These beads will form a topology in the sense already explained above on the surface of this substrate 2. The amplitude of this topology is defined by the diameter d, or the maximum dimension, of beads measured according to the axis z (perpendicular to the surface 4 of substrate 2), of the particles deposited. The particles from Figure 2A have a diameter d1; those of Figure 3A have a diameter d2 that is less than d1.

During the oxidation step, an irregular oxidation front will be generated, which will again have the consequence of forming a rough interface 22, 22'' or substantially reproducing the initial topology formed by beads or particles 14, 14'. This interface is the oxide/silicon type

in the example of substrate 2 in silicon and particles 14, 14' initially in silicon.

The roughness or amplitude of the topology of interface 22, 22' depends on the maximum dimension, measured following axis z of deposited particles 14, 14' (the dimensions of these particles may go from several dozen nm to several µm, for example from 10 nm or 20 nm to 1 µm or 10 µm) and the thickness of the thermal oxide 20, 20'. In fact, the thicker this oxide, the more the roughness or amplitude of the topology of the interface 22, 22' is reduced.

Therefore, roughnesses and/or topologies that are both high and/or low frequencies may be generated (these frequencies are spatial frequencies of the distribution of irregularities at the substrate surface) according to the density and size of the particles 14, 14' deposited. In the case of particles of Si, a thermal oxide thickness greater than or equal to:

$$E=d/0.44$$

allows almost all of the particles to be consumed. This time d corresponds to the diameter or to the maximum size of the largest particle.

This technique also allows inhomogeneities in the concentration and size of particles 14, 14' to be created on the wafer, thereby allowing different types of roughnesses and/or topologies to be formed on the same wafer: to do this particles 14, 14' with varied diameters are deposited, for example particles with a diameter d1 and particles with a diameter d2 that is less than d1.

Two other embodiments will be explained in connection with Figures 4A-4C.

According to one of these embodiments of the invention, a rough deposition 36 of oxide or nitride is made (by LPCVD or PECVD techniques) on substrate 2.

The roughness R2 of surface 38 of this deposition is greater than roughness R1 of the initial surface 4 of substrate 2 (Figure 4A).

During thermal oxidation, an irregular oxidation front 31 is produced (Figure 4B), as in the other cases explained above. The irregular character is due to the surface roughness of the layer 36 deposited. A buried rough interface 32 is also formed, having a roughness R3, close to R2, more particularly slightly less than R2.

The duration of the oxidation step is such that the oxidation front at least reaches the initial substrate 2 and possibly progresses in substrate 2, beyond its initial surface 4.

In the case of oxide layer 36, it is crossed by the oxidation front which, furthermore, will oxidize the substrate. The oxidation will allow the transfer of the roughness of surface 38 in the substrate.

According to yet another embodiment of the invention, it is possible to make a layer 36 in oxide (for example by PECVD or LPCVD or thermal oxidation) or in nitride (for example by PECVD or LPCVD), then to roughen the layer or to increase the roughness of this layer by HF attack (the concentration of this may vary from 1% to 49%) or with H_3PO_4 (orthophosphoric acid) for SiN. This attack is stopped before reaching substrate 2.

If, as has already been explained above, a second oxidation is carried out after the roughening step, the irregular oxidation front will be transferred in substrate 2. Here

also, the thermal oxide thickness 40 (Figure 4C) formed will be such that the oxidation front crosses interface 4 and penetrates in substrate 2. The roughness of interface 32 may be adapted by varying on the one hand the parameters (time, concentration) of the HF attack (this will exploit the initial roughness of surface 38) and on the other hand the thickness of oxide 40 resulting from the oxidation step.

A substrate obtained by a process according to the invention comprises a buried interface 12, 22, 22', 32 with a chosen roughness or having a topology similar to the topology created initially, and may be utilized for different applications.

In particular, it may be employed for the manufacture of antisticking BSOI substrates, in "superior" substrate and/or support. The material layer 10, 20, 20', 40 may be eliminated, therefore leaving the oxidation front 12, 22, 22', 32 exposed at the desired roughness R2. A new thermal oxidation step may be carried out to generate very high quality silicon oxide.

The oxidized substrate may be bonded to the rough interface. Preparing the surface is then recommended.

As illustrated in Figure 5A, a mechanical chemical polishing step may be performed in order to restore good surface roughness (that is, a roughness adapted to direct bonding) of the oxide layer 10 (Figure 5A, as in addition Figures 6A, 6B, represents the layer 10 by way of example, but other layers 20, 20', 40, 60 are also affected).

As illustrated in Figure 5B, bonding, for example direct bonding by molecular adhesion, may then be performed on a second substrate 52, for example bulk silicon. This second substrate 52 or the first substrate may then be thinned.

Any thinning technique may be implemented, for example a mechanical, chemical or mechanical chemical technique or the "Smart Cut ™" process.

Direct bonding may then be carried out on a second substrate 102, itself also having a rough buried interface 112 (Figure 6A). This substrate was preferably obtained according to one of the processes described above.

The assembled structure may then undergo thermal treatment to reinforce the bonding interface and one or more thinning steps until an SOI structure 105 is obtained, comprising one or two rough oxide/silicon interfaces. Figure 6B represents such a structure with two rough interfaces 12, 112 and one residual layer 110 of the second substrate.

During the production of integrated sensor membranes or mobile parts, part of the oxide 10 may then be locally removed by etching through openings 111, 113 made in the residual layer 110. Cavities may then be locally created under membranes. The rough interface 112 prevents ill-timed bonding or adherence of the membrane on the substrate 2.

Another utilization of a substrate according to the invention is illustrated in Figure 7: the oxide 10, 20, 20', 40 may be replaced with an oxide layer 60 if the first (for example, layer 10) was not homogeneous enough. To do this, one may carry out a desoxidation step with an HF (hydrofluoric acid) solution, followed by a thermal oxidation step of substrate 2, thereby generating the oxide layer 60. The interface 12' thereby generated has a roughness that is less than or equal to that of the rough interface 12, of roughness R3, obtained after the first oxidation.

One advantage of a manufacturing process according to the invention is the flexibility of obtaining a rough

oxide/silicon interface: the roughness frequency ranges that may be reached are large, while a substrate is kept in a crystalline material and free of defects.

Another advantage of the manufacturing processes described is that the layer 6, 14, 36 of irregularities utilized is totally oxidized during the oxide generation step that will transfer the roughness or topology. This allows BSOI structures to be made without insert material (only monocrystalline silicon and oxide).

The different embodiments disclosed may be used individually, successively or even combined.

The examples given above implement a silicon substrate or substrates. But the invention may be applied to all semiconductor substrates that can be oxidized, particularly: monocrystalline Si, polycrystalline Si, amorphous Si, SiC.

Constructing a rough buried interface according to the invention is especially interesting for manufacturing an "antisticking" BSOI type substrate, the application described for example in document FR 2857953.

In a process according to the invention, the roughness obtained may be inspected for example by measuring haze on TENCOR 6200 (surfscan) type equipment. This parameter provides information on the surface roughness on the totality of the substrate surface ("full wafer" mapping), as explained in the article by F. Hölsteyns et al., "Seeing through the haze, Process monitoring and qualification using comprehensive surface data," published in Yield Management Solutions, Spring 2004, pp. 50-54.

The roughness may also be inspected by AFM (atomic force microscope) measurement on scans typically ranging from 1 μm^2 to 10000 μm^2.

Figures 8 and 9 illustrate the differences in behavior between a device without a rough interface and a device with a rough interface.

In Figure 8, a membrane 110 was obtained by etching a cavity 111 in a layer 120 of oxide through an opening 113. The assembly remains on a support 2 in a semiconductor material (silicon for example). The zones 107 and 109 of the membrane 110 may adhere to the upper surface of the substrate 2 during etching of the underlying oxide, or later, during deformations of this membrane linked to the operation of the finished component.

Figure 9 again represents a device according to the invention, in which the upper face 12 of the substrate 2 comprises a roughness obtained by a process according to the invention, for example such as explained above in connection with Figure 6B.

These roughnesses will prevent zones 107 and 109 of membrane 110 from adhering to the upper surface 12 of substrate 2.

In a variation, this may be the lower face 112 of membrane 110 that comprises a roughness obtained by a process according to the invention, for example such as explained above in connection with Figure 6B. This roughness prevents zones 107 and 109 of membrane 110 from adhering to the upper surface 12 of substrate 2.

CLAIMS

1. A process of forming a rough interface (12, 22, 22', 32) in a semiconductor substrate (2) comprising:
   - the formation, on a surface (4) of said substrate, of a zone of irregularities (8, 38) in a material (6, 14, 14', 36) that may be oxidized, and/or does not shield oxidation,
   - the formation of a rough interface in the semiconductor substrate (2) by thermal oxidation of, or through, this material (6, 14, 14', 36), and a part of the semiconductor substrate.

2. The process according to claim 1, the zone of irregularities comprising an additional layer (6, 36) presenting a roughness (R2) that is greater than the initial roughness (R1) of the surface of said substrate.

3. The process according to claim 2, the additional layer having an initial thickness between 10 nm and 3 μm.

4. The process according to one of claims 2 or 3, the roughness of the additional layer being between 1 nm RMS and 10 nm RMS, in a 5 μm x 5 μm scan.

5. The process according to one of claims 2 to 4, the roughness (R2) of the additional layer (6, 36) being obtained by prior chemical attack of the additional layer (6, 36), this prior chemical attack not reaching the substrate (2).

6. The process according to one of claims 1 to 5, the zone of irregularities being formed on a layer of polysilicon or amorphous silicon.

7. The process according to one of claims 1 to 5, the zone of irregularities being formed on a layer of silicon oxide or silicon nitride.

8. The process according to claim 5, the additional layer (6, 36) being in thermal oxide or nitride, the roughness (R2) of this additional layer (6, 36) being obtained by prior attack of HF or H3PO4.

9. The process according to claim 1, the zone of irregularities comprising particles (14, 14') deposited on the surface (4) of said substrate.

10. The process according to claim 9, the particles having a maximum diameter or size, measured following an axis perpendicular to the substrate of between 10 nm and 10 µm.

11. The process according to claim 10, the particles having different diameters or different sizes, these sizes being measured following an axis perpendicular to the substrate.

12. The process according to one of claims 1 to 11, the oxidation step being a dry or wet thermal oxidation step at a temperature between 950° C and 1200° C.

13. The process according to one of claims 1 to 12, the oxidation step being followed by a step of eliminating oxide formed by oxidation, to refresh the rough surface, then a step of forming a new thermal oxide layer.

14. The process of forming a semiconductor component with a buried rough interface comprising:

- the formation of a rough interface (12, 22, 22', 32) in a first semiconductor substrate according to one of claims 1 to 13,
- the preparation of the surface of the oxide or the oxidized material (6, 14, 14', 36), in view of assembly with a second substrate (52, 102),
- the assembly of the surface of the oxide or oxidized material (6, 14, 14', 36) and the second substrate (52, 102).

15. The process according to claim 14, the second substrate being a raw or bulk substrate.

16. The process according to claim 15, the second substrate being a monocrystalline or polycrystalline or amorphous silicon substrate, or SiC.

17. The process according to claim 14, the second substrate being obtained by a process according to one of claims 1 to 13.

18. The process according to one of claims 14 to 17, one of the two substrates then being thinned.

19. The process according to one of claims 14 to 18, at least one portion of oxide or oxidized material being eliminated.

20. The process according to claim 19, the elimination of a portion of oxide being done by etching through at least one opening (111, 113) made in one of the two substrates.

21. The process according to one of claims 1 to 20, the first substrate being a monocrystalline or polycrystalline or amorphous silicon substrate, or SiC.