

ABSTRACT

A control system controls the execution of cache memory access instructions such that cache coherency related problems do not arise.

The computer system includes a plurality of processing units (102) each having at least one cache. Multi-processor cache coherency is maintained in the computer system. At least one of the processing units of the computer system includes a split-level cache arrangement that comprises a first level cache (108) coupled to a second level cache (112), wherein integer store instructions enable data to be stored in both the first level cache and the second level cache. The first level cache is byte writable and the second level cache is word writable. During execution of an integer store instruction, one or more bytes are read from the first level cache and written to the second level cache along with write data of the FA instruction, such that data of word length is written to the second level cache.

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