Abstract

A semiconductor memory device may include a cell substrate; a mold structure including a plurality of gate electrodes stacked on the cell substrate; a channel structure penetrating the mold structure; a string select line on the mold structure; a string select channel structure penetrating the string select line and contacting the channel structure; an anti-arcing contact penetrating the mold structure; an insulating pattern between the anti-arcing contact and the plurality of gate electrodes; and an anti-arcing insulating pattern penetrating the string select line to be in contact with the anti-arcing contact.

FIG. 4