

Description

The invention relates to a raster positioning circuit such as, for example, a centering circuit for a deflection system of a display.

Deflection systems utilized in television receivers or monitors frequently include circuitry which allows for the adjustment of, for example, the centering of the raster on the face of the kinescope tube. The need for this centering feature is increased as overscan of the kinescope tube is reduced, that is, as the raster width approaches the width of the kinescope tube face. Centering is usually accomplished by causing a direct current of selected polarity and amplitude to flow through the deflection windings.

In some prior art arrangements such as the arrangement disclosed in EP-A-0072595, the centering circuitry is placed in parallel with the deflection windings to produce an average, or DC current through the deflection winding during the trace interval. This centering circuitry includes a non-symmetrical conduction network including an adjustable resistor. An integrating inductor is coupled in series combination with the network for rectifying a portion of the current that flows in the integrating inductor and that provides centering. The nominal resistance of the adjustable resistor in this arrangement is, typically, relatively large as compared with the impedance of the deflection winding.

It may be desirable to control the rectified current in the integrating inductance in a more precise manner and within a narrow tolerance range to counteract effects of temperature variations and aging of components.

In accordance with an aspect of the invention, a deflection apparatus with a raster positioning arrangement includes a source of a first signal at a frequency that is related to a deflection frequency. A deflection winding conducts a deflection current that causes the electron beam to form raster lines on the face of a display. A deflection rate voltage is generated in accordance with the first signal. An inductance responsive to the deflection rate voltage generates an alternating current in the inductance that is coupled to the deflection winding. A variation in the average value of the current in the inductance produces a corresponding variation in the average value of the deflection current and a corresponding variation in the positioning of the raster lines on the face of the display. A controllable conduction network responsive to a control signal and coupled in the current path of the current in the inductance rectifies the current in the inductance such that the average value of the current in the inductance is determined in accordance with the control signal. A signal that is indicative of the amplitude of the current in the inductance is gen-

erated. A control circuit, responsive to the signal that is indicative of the amplitude of the current in the inductance, generates the control signal such that the control circuit and the conduction network form a negative feedback control loop that regulates the average value of the current in the inductance.

In some television deflection systems, a B+ energizing voltage is coupled through a choke to a trace capacitor of a deflection circuit output stage for supplying the energy that is required by the output stage. In such arrangement, a direct current flows from a terminal of the trace capacitor via the deflection winding and through a deflection switch. Such direct current may, disadvantageously, cause a shift in the positioning of the raster to one side. The level of such direct current may be dependent on the losses of the system.

In carrying out another aspect of the invention, a centering circuit embodying the invention is coupled to the deflection winding to compensate for, or completely eliminate, such shift.

In the Drawing:

FIGURE 1 illustrates a deflection system that includes a raster centering circuit embodying the invention;

FIGURES 2a-2d illustrate a first example of waveforms useful in explaining the operation of the circuit of FIGURE 1; and

FIGURES 3a-3d illustrate a second example of waveforms useful in explaining the operation of the circuit of FIGURE 1 for a centering current that is larger than in the first example.

FIGURE 1 illustrates a deflection system 122, embodying the invention, that includes an output stage 22 that generates a deflection current i_y in a deflection winding L_y . Deflection winding L_y forms a series arrangement with a linearity inductor L_{LIN} . The series arrangement is coupled between terminals W1a and W10a. A voltage V_{cs} that includes an average, or DC voltage B+ is developed at terminal W10a. Voltage V_{cs} includes a parabolic voltage that is developed in a trace capacitor C_s to provide S-correction of current i_y . Terminal W1a is coupled to a deflection switch arrangement 24 that includes a damper diode D1 that is conductive during the first half of trace and a cascode switch arrangement 23 that is conductive in the second half of trace. During retrace switch arrangement 24 is non-conductive.

An oscillator and driver unit 20 receives a synchronizing signal V_H at horizontal frequency f_H from an incoming video signal. Unit 20 supplies an output signal at the frequency f_H for controlling the operation of output stage 22. Such output signal is coupled to the gate of an FET switch Q1a of cascode switch arrangement 23 of output stage 22. The output signal causes switch Q1a to conduct

from a time that occurs shortly prior to the center of the horizontal trace interval until switch Q1a becomes non-conductive, for initiating the retrace interval, at approximately the end of the horizontal trace interval. A main current conducting electrode of FET switch Q1a is coupled to the emitter electrode of a transistor switch Q1b of cascode switch arrangement 23. The collector of transistor switch Q1b is coupled to end terminal W1a of primary winding W1 of transformer T1. A voltage V_{Q1b} , at the base electrode of transistor switch Q1b, is developed across a zener diode 54. During trace, positive voltage V_{Q1b} is coupled from a series arrangement of a forward biased diode 55 and a resistor 55a coupled to a secondary winding W11 of transformer T1. During retrace, voltage V_{Q1b} is zero because diode 55 is non-conductive. At the beginning of retrace, the charge stored in the collector-base junction of transistor Q1b forms a collector-base current that causes zener diode 54 to conduct. Thus, zener diode 54 prevents voltage V_{Q1b} from exceeding the breakdown voltage of zener diode 54.

One plate of a retrace capacitor C_R that develops retrace voltage V_R is coupled to terminal W1a of winding W1. The other plate of capacitor C_R is coupled to ground. Damper diode D1, is coupled across the plates of retrace capacitor C_R . Diode D1 clamps the voltage at terminal W1a to approximately the ground potential during the first half of the trace interval, whereas cascode switch arrangement 23 clamps the voltage at terminal W1a to approximately ground potential during the second half of the trace interval. The switching operation of arrangement 23 at the horizontal rate generates both deflection current i_Y in deflection winding L_Y and a current i_{L1} in inductance L1. As described later on, current i_{L1} provides raster centering.

S-shaping of the horizontal deflection current i_Y is provided by trace capacitor C_s having one plate that is coupled to terminal W10a and the other plate coupled to ground. Energy losses are replenished by the DC voltage B+ portion of voltage V_{cs} . The DC voltage B+ portion of voltage V_{cs} is coupled from a regulated supply 50. Voltage V_{cs} includes a parabolic voltage portion that provides S-shaping of current i_Y .

Regulated supply 50 comprises a series pass transistor switch 56 operating with a duty cycle that is controlled by a B+ switching regulator control circuit 57. A current conducting terminal 56a of switch 56 is coupled to a DC unregulated voltage V_{UR} . The other current conducting terminal 56b is coupled via a choke L2 to terminal W10a for providing the DC current that replenishes the energy losses of deflection system 122. A flywheel diode 58 is coupled from terminal 56b to ground. Regulator control circuit 57 produces at an output terminal

57d, a rectangular waveform signal V_{REG} that is illustratively at the frequency f_H . The duty cycle of signal V_{REG} controls the duty cycle of switch 56 so as to regulate the average or DC voltage B+ part of voltage V_{cs} that energizes output stage 22.

A centering circuit 70, embodying an aspect of the invention, is coupled between terminals W1a and W10a. Centering circuit 70 includes a winding W1 that provides an integrating inductance L1 to circuit 70. Winding W1, coupled between terminal W1a and terminal W1b, is the primary winding of transformer T1.

A non-symmetrical conduction network 48 is coupled in series with winding W1 between terminal W1b and terminal W10a. Network 48 includes a diode D2, poled to conduct the negative portion of current i_{L1} in inductance L1. Diode D2 is coupled between terminals W10a and W1b. A retrace voltage V_R at terminal W1a develops in inductance L1 current i_{L1} at the frequency f_H . The collector electrode of a transistor Q3 of network 48 that conducts a collector current i_{Q3} is coupled to terminal W1b. The emitter electrode of transistor Q3 is coupled to an arrangement of a current sensing resistor R1 that is coupled in parallel with a capacitor C1. Each of resistor R1 and capacitor C1 has a corresponding terminal that is coupled to terminal W10a.

A control circuit 49, embodying another aspect of the invention, utilizes feedback for sensing the average value $i_{Q3(AV)}$ of positive current i_{Q3} that is proportional to the DC voltage drop across resistor R1. As described in detail later on, control circuit 49 regulates the average value $i_{Q3(AV)}$ of positive current i_{Q3} by controlling, in accordance with a voltage V_{REF} , the base electrode current i_b of transistor Q3.

FIGURES 2a-2d and FIGURES 3a-3d illustrate waveforms that are useful for explaining the operation of centering circuit 70 of FIGURE 1. Similar numbers and symbols in FIGURES 1, 2a-2d and 3a-3d indicate similar items or functions. FIGURES 2a-2d and the corresponding FIGURES 3a-3d illustrate similar types of waveforms for first and second examples, respectively.

In, the first example, represented by FIGURES 2a-2d, the average value $i_{Q3(AV)}$ of current i_{Q3} shown in FIGURE 2c, is substantially smaller than that in the second example, represented by FIGURES 3a-3d. The positive portion of current i_{L1} flows in transistor Q3 as collector current i_{Q3} . The average value $i_{Q3(AV)}$ of current i_{Q3} is controlled by transistor Q3 and determines the average value of current i_{L1} , as described later on.

In the first example, shown in FIGURES 2a-2d, transistor Q3 of FIGURE 1 conducts current i_{Q3} in the interval t_1 - t_2 of FIGURE 2c. The positive portion of current i_{L1} of FIGURE 2b is equal to current i_{Q3} of FIGURE 2c in the interval t_1 - t_2 . In the

second example, shown in FIGURES 3a-3d, transistor Q3 of FIGURE 1 is in saturation and operates as a switch. The positive portion of current i_{L1} of FIGURE 3b is equal to current i_{Q3} of FIGURE 3c in the interval t_1 - t_2 .

Non-symmetrical conduction, or rectification, that is performed by network 48 of FIGURE 1, causes the average value $i_{L1(AV)}$ of current i_{L1} to become more negative in the first example of FIGURE 2b than in the second example of FIGURE 3b. The average value $i_{L1(AV)}$ of FIGURE 1 is controlled by transistor Q3 of network 48 that regulates the average value $i_{Q3(AV)}$ of current i_{Q3} . The duration of the positive portion of the waveform of current i_{L1} of, for example, FIGURE 2b is controlled by transistor Q3 of FIGURE 1 in such a way that current i_{Q3} of, for example, FIGURE 2c, that is equal in the interval t_1 '- t_2 ' to current i_{L1} of FIGURE 2b, provides the required average value $i_{Q3(AV)}$ of FIGURE 2c. The remaining portion of the waveform of current i_{L1} of FIGURE 2b is negative. Thus, in each deflection cycle, transistor Q3 of FIGURE 1 controls the ratio between the interval in which current i_{L1} is positive and that in which it is negative.

In order to replenish energy losses when deflection system 122 of FIGURE 1 produces a given peak-to-peak amplitude of deflection current i_y , supply 50 has to supply a corresponding average DC current that flows in both inductor L1 and deflection winding L_y and switch 23. As explained before, the average value of current i_{L1} is controlled by transistor Q3. An increase in the magnitude of the average, or DC, current that flows in inductance L1 causes a corresponding decrease in the magnitude of the average value of current i_y . Such increase in the magnitude of the average value of the current in inductance L1 replenishes losses that were incurred prior to such increase, by a corresponding portion of the DC current that flows in deflection winding L_y . Thus, transistor Q3, that controls the average value $i_{L1(AV)}$, controls the centering of the raster by also controlling the average value of deflection current i_y .

The magnitude of the average value $i_{L1(AV)}$ in the first example of FIGURE 2a, that is more negative, represents a larger positive DC current that flows from supply 50 via inductor L1 and into terminal W1a, than that flowing in the second example of FIGURE 3b. Therefore, the magnitude of the average value of current i_y in the first example is smaller than that in the second example. It follows that deflection current i_y produces less offset of the raster in the first example than in the second example.

In accordance with an aspect of the invention, control circuit 49 regulates the average value of current i_y that determines the centering of the raster by precisely controlling the average value of

current i_{L1} inductance L1. Control circuit 49 controls the average value of current i_{L1} when current i_{L1} is, illustratively, positive.

Control circuit 49 comprises a differential amplifier 71 having an inverting input terminal 71a that is coupled to resistor R1 for sensing the voltage across resistor R1. Because of the filtering action of capacitor C1, the voltage across resistor R1 is indicative of the average value $i_{Q3(AV)}$ of current i_{Q3} . A non-inverting input terminal 71b receives a voltage that is adjustable by adjusting a potentiometer P1, as described later on.

Control circuit 49, using negative feedback, controls the base current i_b of transistor Q3 by controlling the voltage at a terminal 71c of amplifier 71. The output voltage at terminal 71c is controlled in the feedback loop in such a way that, in steady state, the voltages at input terminals 71a and 71b of amplifier 71 are substantially the same.

A secondary winding W12 of transformer T1 has an end terminal that is conductively coupled to terminal W10a. The other end terminal of winding W12 of transformer T1 is coupled through a diode D4 to the cathode of a zener diode D3. The anode of zener diode D3 is conductively coupled to terminal W10a. A voltage V_{D3} across diode D3 provides the power required for operating differential amplifier 71 by coupling the anode of diode D3 to a terminal SUP+ and the cathode of diode D3 to a terminal SUP- of amplifier 71. Also, voltage V_{D3} is coupled to potentiometer P1 for generating a reference voltage V_{REF} that is coupled to noninverting input terminal 71b of amplifier 71. Thus, control circuit 49 has a floating common potential that is equal to voltage V_{GS} .

Voltage V_{REF} between the wiper of potentiometer P1 and the terminal of potentiometer P1 is at voltage V_{GS} . Voltage V_{REF} is a constant DC voltage that is adjustable by adjusting the position of the wiper of potentiometer P1. The negative feedback loop of control circuit 49 causes the voltage across resistor R1, that determines the average value $i_{Q3(AV)}$ of current i_{Q3} , to be equal to voltage V_{REF} . Thus, adjustable voltage V_{REF} also determines the average value $i_{L1(AV)}$ of current i_{L1} .

It should be understood that by coupling a predetermined time varying voltage to, for example, terminal 71b of amplifier 71, it is possible to correct other types of raster distortion. For example, a parabolic waveform at the vertical rate that is capacitively coupled to terminal 71b of amplifier 71 is capable of correcting a bow distortion. Similarly, a linear component voltage is capable of correcting tilt distortion.

A diode D2a, illustrated in broken lines in FIGURE 1, may be added in series with diode D2 for obtaining a coarse adjustment of the average value of current i_{L1} and that of current i_y . When both

diodes D2 and D2a are coupled in series with inductance L1, the increase in the forward resistance of the series coupled diodes D2 and D2a causes the average value $i_{L1(AV)}$ to become smaller in magnitude. A decrease in the magnitude of the average value $i_{L1(AV)}$ causes the average value of current i_Y to become larger in magnitude, as described before. Thus, the magnitude of the average value of current i_Y can be, for example, increased by adding diode D2a in series with diode D2.

Claims

1. A deflection apparatus with a raster positioning arrangement, comprising:
 - a source of a first signal (V_H) at a frequency that is related to a deflection frequency (f_H);
 - a deflection winding (L_Y) for conducting a deflection current that causes an electron beam to scan said raster on the face of a display;
 - switching means (24) coupled to said deflection winding (L_Y) and responsive to said first signal (V_H) for generating a deflection rate voltage (V_R);
 - an inductance (L1) responsive to said deflection rate voltage (V_R) for generating an alternating current (i_{L1}) in said inductance (L1) that is coupled to said deflection winding (L_Y), such that a variation in the average value of said current (i_{L1}) in said inductance (L1) produces a corresponding variation in the average value of said deflection current (i_Y) and a corresponding variation in the positioning of the raster on the face of the display; and
 - a controllable conduction network (48) responsive to a control signal (i_b) and coupled in the current path of said current (i_{L1}) in said inductance (L1) for rectifying said current in said inductance (L1) such that the average value of said current in said inductance (L1) is determined in accordance with said control signal (i_b); characterized by:
 - second means (R1) responsive to said current (i_{L1}) in said inductance (L1) for generating a signal that is indicative of the amplitude of said current in said inductance (L1); and
 - a control circuit (49), responsive to said signal that is indicative of the amplitude of said current in said inductance (L1), for generating said control signal (i_b) such that said control circuit (49) and said conduction network (48) form a negative feedback control loop that regulates the average value of said current (i_{L1}) in said inductance (L1).
2. An apparatus according to Claim 1 characterized by, a source (50, C_s) of DC current coupled to said deflection winding (L_Y), said DC current having a first current portion that flows in said deflection winding at a level that is equal to the average value of said deflection current, and having a second current portion that flows in said inductance (L1).
3. An apparatus according to Claim 1 characterized by, a trace capacitor (C_s) coupled to said deflection winding (L_Y), a source (56-58) of a supply voltage and a choke (L2), said choke (L2) having a first terminal (56b) that is coupled to said source (56-58) of supply voltage and a second terminal (W10a) that is coupled to said trace capacitor (C_s) such that said deflection winding (L_Y), said trace capacitor (C_s) and said choke (L2) are included in first, second and third branches having a common junction terminal (W10a).
4. An apparatus according to Claim 3 characterized in that said conduction network (48) and said inductance (L1) are included in a fourth branch that is coupled to said common junction terminal (W10a).
5. An apparatus according to any one of the preceding Claims characterized in that said controllable conduction network (48) comprises a rectifier (D2) for conducting said current in said inductance (L1) when said current in said inductance (L1) is at a first polarity, and third means (Q3) for conducting said current in said inductance (L1) when said current in said inductance (L1) is at a second polarity corresponding to the polarity opposite the first polarity.
6. An apparatus according to Claim 5 characterized in that said rectifier comprises a first diode (D2).
7. An apparatus according to Claim 6 characterized in that said rectifier further comprises a second diode (D2a) that is coupled in series with said first diode (D2).
8. An apparatus according to any one of Claims 5 to 7 characterized in that said third means comprises a transistor (Q3) and wherein said control signal (i_b) is coupled to a control electrode (base) of said transistor (Q3) for controlling the average current in said transistor (Q3).
9. An apparatus according to any one of Claims 5 to 8 characterized in that said second means



diodes D2 and D2a are coupled in series with inductance L1, the increase in the forward resistance of the series coupled diodes D2 and D2a causes the average value $i_{L1(AV)}$ to become smaller in magnitude. A decrease in the magnitude of the average value $i_{L1(AV)}$ causes the average value of current i_Y to become larger in magnitude, as described before. Thus, the magnitude of the average value of current i_Y can be, for example, increased by adding diode D2a in series with diode D2.

Claims

1. A deflection apparatus with a raster positioning arrangement, comprising:

a source of a first signal (V_H) at a frequency that is related to a deflection frequency (f_H);

a deflection winding (L_Y) for conducting a deflection current that causes an electron beam to scan said raster on the face of a display;

switching means (24) coupled to said deflection winding (L_Y) and responsive to said first signal (V_H) for generating a deflection rate voltage (V_R);

an inductance (L1) responsive to said deflection rate voltage (V_R) for generating an alternating current (i_{L1}) in said inductance (L1) that is coupled to said deflection winding (L_Y), such that a variation in the average value of said current (i_{L1}) in said inductance (L1) produces a corresponding variation in the average value of said deflection current (i_Y) and a corresponding variation in the positioning of the raster on the face of the display; and

a controllable conduction network (48) responsive to a control signal (i_b) and coupled in the current path of said current (i_{L1}) in said inductance (L1) for rectifying said current in said inductance (L1) such that the average value of said current in said inductance (L1) is determined in accordance with said control signal (i_b); characterized by:

second means (R1) responsive to said current (i_{L1}) in said inductance (L1) for generating a signal that is indicative of the amplitude of said current in said inductance (L1); and

a control circuit (49), responsive to said signal that is indicative of the amplitude of said current in said inductance (L1), for generating said control signal (i_b) such that said control circuit (49) and said conduction network (48) form a negative feedback control loop that regulates the average value of said current (i_{L1}) in said inductance (L1).

2. An apparatus according to Claim 1 characterized by, a source (50, C_s) of DC current coupled to said deflection winding (L_Y), said DC current having a first current portion that flows in said deflection winding at a level that is equal to the average value of said deflection current, and having a second current portion that flows in said inductance (L1).

3. An apparatus according to Claim 1 characterized by, a trace capacitor (C_s) coupled to said deflection winding (L_Y), a source (56-58) of a supply voltage and a choke (L2), said choke (L2) having a first terminal (56b) that is coupled to said source (56-58) of supply voltage and a second terminal (W10a) that is coupled to said trace capacitor (C_s) such that said deflection winding (L_Y), said trace capacitor (C_s) and said choke (L2) are included in first, second and third branches having a common junction terminal (W10a).

4. An apparatus according to Claim 3 characterized in that said conduction network (48) and said inductance (L1) are included in a fourth branch that is coupled to said common junction terminal (W10a).

5. An apparatus according to any one of the preceding Claims characterized in that said controllable conduction network (48) comprises a rectifier (D2) for conducting said current in said inductance (L1) when said current in said inductance (L1) is at a first polarity, and third means (Q3) for conducting said current in said inductance (L1) when said current in said inductance (L1) is at a second polarity corresponding to the polarity opposite the first polarity.

6. An apparatus according to Claim 5 characterized in that said rectifier comprises a first diode (D2).

7. An apparatus according to Claim 6 characterized in that said rectifier further comprises a second diode (D2a) that is coupled in series with said first diode (D2).

8. An apparatus according to any one of Claims 5 to 7 characterized in that said third means comprises a transistor (Q3) and wherein said control signal (i_b) is coupled to a control electrode (base) of said transistor (Q3) for controlling the average current in said transistor (Q3).

9. An apparatus according to any one of Claims 5 to 8 characterized in that said second means



comprises a resistor (R1) that is coupled in the current path of said inductance (L1) when said current in said inductance is at said opposite polarity, and a capacitor (C1) coupled to said resistor (R1) for filtering, from said voltage in said resistor, voltage variations that occur at said deflection rate, for developing, in said resistor (R1), a voltage that is indicative of the average value of said current in said inductance (L1) that is at said opposite polarity.

10. An apparatus according to Claim 9 characterized in that said capacitor (C1) is coupled in parallel with said resistor (R1) and wherein said signal that is indicative of the amplitude of said current in said inductance (L1) is generated across said resistor (R1).

11. An apparatus according to any one of the preceding Claims characterized in that said control circuit (49) comprises an amplifier (71) having a first input terminal (71a) for receiving a feedback signal that comprises said signal that is indicative of the amplitude of said current in said inductance (L1), said amplifier having a second input terminal (71b) responsive to a second input signal (V_{REF}), and having an output terminal (71c) for generating said control signal (i_b), in accordance with the difference between the signals at said first (71a) and second (71b) input terminals of said amplifier (71), to regulate the average value of said current in said inductance (L1) in accordance with said second input signal (V_{REF}).

12. An apparatus according to any one of Claims 1 to 7 characterized in that said conduction network (48) comprises a transistor (Q3) that conducts said current in said inductance (L1) when said current in said inductance (L1) is at a second polarity, and wherein said control circuit (49) comprises an amplifier (71) that generates at an output terminal (71c) of said amplifier (71) said control signal (i_b) that is coupled to a control terminal (base) of said transistor (Q3) for controlling the average value of said current (i_{L1} in said inductance (L1) that is at said second polarity.

13. An apparatus according to any one of Claims 1 to 7 characterized in that said conduction network (48) comprises a transistor (Q3) and wherein said second means comprises a resistor (R1) that is coupled in a main current conduction path of said transistor (Q3) to form a current path that conducts said current in said inductance (L1) when said current in said inductance (L1) is at a second polarity.

Patentansprüche

1. Ablenk-Einrichtung mit einer Raster-Positionieranordnung,

- mit einer Quelle eines ersten Signales (v_H) bei einer Frequenz, die zur Ablenkfrequenz (f_H) Bezug hat;
- mit einer Ablenkwicklung (L_Y) zum Führen eines Ablenkstromes, der einen Elektronenstrahl die Front (face) einer Anzeige abtasten (scannen) läßt;
- mit Schaltmitteln (24), die mit der Ablenkwicklung (L_Y) gekoppelt sind und die abhängig von dem ersten Signal (V_H) sind zum Erzeugen einer Ablenkraten-Spannung (V_R);
- mit einer Induktivität (L1), die abhängig von der Ablenkraten-Spannung (V_R) ist zum Erzeugen eines Wechselstromes (i_{L1}) in der Induktivität (L1), die mit der Ablenkwicklung (L_Y) gekoppelt ist und zwar so, daß eine Veränderung in dem Mittelwert des Stromes (i_{L1}) in der Induktivität (L1) eine entsprechende Änderung in dem Mittelwert des Ablenkstromes (i_Y) und eine entsprechende Veränderung in der Positionierung des Rasters auf der Front der Anzeige erzeugt; und
- mit einem steuerbaren Leitungs-Netzwerk (conduction network, 48), das abhängig von einem Steuersignal (i_b) ist und in den Strompfad des Stromes (i_{L1}) in der Induktivität (L1) gekoppelt ist zum Gleichrichten des Stromes in der Induktivität (L1) so, daß der Mittelwert des Stromes in der Induktivität (L1) in Übereinstimmung mit dem Steuersignal (i_b) bestimmt wird;

gekennzeichnet durch

- zweite Mittel (R1), die abhängig von dem Strom (i_{L1}) in der Induktivität (L1) sind zum Erzeugen eines Signales, das die Amplitude des Stromes in der Induktivität (L1) anzeigt; und
- eine Steuerschaltung (49), die abhängig von dem Signal ist, das die Amplitude des Stromes in der Induktivität (L1) anzeigt zum Erzeugen des Steuersignals (i_b) so, daß die Steuerschaltung (49) und das Leitungs-Netzwerk (48) eine negativ rückkoppelnde steuerschleife bilden, die den Mittelwert des Stromes (i_{L1}) in der Induktivität (L1) regelt.

2. Einrichtung nach Anspruch 1,

gekennzeichnet durch

eine Quelle (50 C_s) von DC-Strom (Gleichstrom), der zu der Ablenkwicklung (L_Y)



gekoppelt wird, wobei der DC-Strom einen ersten Stromabschnitt hat, der in der Ablenkwicklung bei einem Pegel fließt, der gleich dem Mittelwert des Ablenkstromes ist und einen zweiten Stromabschnitt aufweist, der in der Induktivität (L1) fließt.

3. Einrichtung nach Anspruch 1, gekennzeichnet durch

- einen Hinlauf-Kondensator (C_s), der mit der Ablenkwicklung (L_v) gekoppelt ist,
- eine Quelle (56-58) von Versorgungsspannung und
- eine Drossel (L2), die einen ersten Anschluß (56b) aufweist, der mit der Quelle (56-58) von Versorgungsspannung gekoppelt ist und einen zweiten Anschluß (W10a) hat, der mit der Hinlauf-Kapazität (C_s) so gekoppelt ist, daß die Ablenkwicklung (L_v), der Hinlauf-Kondensator (C_s) und die Drossel (L2) in erstem, zweitem und drittem Zweig(e) enthalten sind, die einen gemeinsamen Verbindungsanschluß (W10a) haben.

4. Einrichtung nach Anspruch 3, dadurch gekennzeichnet,

daß das Leitungs-Netzwerk (48) und die Induktivität (L1) in einem vierten Zweig enthalten sind, der mit dem gemeinsamen Verbindungsanschluß (W10a) gekoppelt ist.

5. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet,

daß das steuerbare Leitungs-Netzwerk (48) einen Gleichrichter (D2) zum Führen des Stromes in der Induktivität (L1) aufweist, wenn der Strom in der Induktivität (L1) eine erste Polarität hat,

daß dritte Mittel (Q3) vorgesehen sind zum Führen des Stromes in der Induktivität (L1), wenn der Strom in der Induktivität (L1) eine zweite Polarität aufweist, die mit der Polarität korrespondiert, die der ersten Polarität entgegengesetzt ist.

6. Einrichtung nach Anspruch 5, dadurch gekennzeichnet,

daß der Gleichrichter eine erste Diode (D2) aufweist.

7. Einrichtung nach Anspruch 6, dadurch gekennzeichnet,

daß der Gleichrichter eine zweite Diode (D2a) aufweist, die mit der ersten Diode (D2) in Serie geschaltet ist.

8. Einrichtung nach Anspruch 5 bis 7, dadurch gekennzeichnet,

daß die dritten Mittel einen Transistor (Q3) aufweisen, wobei das Steuersignal (i_b) zu einem Steueranschluß (Basis) des Transistors (Q3) gekoppelt ist zum Steuern des Strommittelwertes in dem Transistor (Q3).

9. Einrichtung nach einem der Ansprüche 5 bis 8, dadurch gekennzeichnet,

daß die zweiten Mittel einen Widerstand (R1) aufweisen, der in den Strompfad der Induktivität (L1) gekoppelt ist, wenn der Strom in der Induktivität die entgegengesetzte Polarität aufweist und

daß eine Kapazität (C1) mit dem Widerstand (R1) gekoppelt ist zum Ausfiltern von Spannungsänderungen aus der Spannung in/an den Widerstand, die mit der Ablenkrate auftreten, wobei in/an dem Widerstand (R1) eine Spannung erzeugt wird, die den Mittelwert des Stromes in der Induktivität (L1) anzeigt, der die entgegengesetzte Polarität aufweist.

10. Einrichtung nach Anspruch 9, dadurch gekennzeichnet,

daß die Kapazität (C1) parallel zu dem Widerstand (R1) gekoppelt ist, wobei das Signal, das die Amplitude des Stromes in der Induktivität (L1) anzeigt, an dem Widerstand (R1) erzeugt wird.

11. Einrichtung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet,

- daß die Steuerschaltung (49) einen Verstärker (71) aufweist,
- der einen ersten Eingangsanschluß (71a) zum Erhalt eines Rückkopplungssignales, welches das Signal enthält, das die Amplitude des Stromes in der Induktivität (L1) anzeigt,
- der einen zweiten Eingangsanschluß (71b), der abhängig von einem zweiten Eingangssignal (V_{REF}) ist und
- der einen Ausgangsanschluß (71c) hat zum Erzeugen des Steuersignals (i_b) in Übereinstimmung mit der Differenz zwischen den Signalen am ersten (71a) und zweiten (71b) Eingangsanschluß (Anschlüssen) des Verstärkers (71), um den Mittelwert des Stromes in der Induktivität (L1) in Übereinstimmung mit dem zweiten Eingangssignal (V_{REF}) zu regeln.

12. Einrichtung nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet,



daß das Leitungs-Netzwerk (48) einen Transistor (Q3) aufweist, der den Strom in der Induktivität (L1) führt, wenn der Strom in der Induktivität (L1) eine zweite Polarität hat;

daß die Steuerschaltung (49) einen Verstärker (71) aufweist, der an seinem Ausgangsanschluß (71c) das Steuersignal (i_d) abgibt, welches an einen Steueranschluß (Basis) des Transistors (Q3) gekoppelt ist zum Steuern des Mittelwertes des Stromes (i_{L1}) in der Induktivität (L1), der die zweite Polarität aufweist.

13. Einrichtung nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet,

daß das Leitungs-Netzwerk (48) einen Transistor (Q3) aufweist, und

daß die zweiten Mittel einen Widerstand (R1) aufweisen, der in einen Hauptstrom-Leitungspfad des Transistors (Q3) gekoppelt ist, um einen Strompfad zu bilden, der den Strom in der Induktivität (L1) führt, wenn der Strom in der Induktivität (L1) eine zweite Polarität aufweist.

Revendications

1. Dispositif de déviation avec un agencement du positionnement de trame, comprenant :

une source d'un premier signal (V_H) à une fréquence qui est reliée à une fréquence de déviation (f_H) ;

un enroulement de déviation (L_V) pour conduire un courant de déviation qui entraîne un faisceau électronique à balayer ladite trame sur la face d'un dispositif d'affichage ;

des moyens de commutation (24) couplés audit enroulement de déviation (L_V) et sensibles audit premier signal (V_H) pour générer une tension nominale de déviation (V_R) ;

une inductance (L1) sensible à ladite tension nominale de déviation (V_R) pour générer un courant alternatif (i_{L1}) dans ladite inductance (L1) qui est couplée audit enroulement de déviation (L_V) de telle sorte qu'une variation de la valeur moyenne dudit courant i_{L1} dans ladite inductance (L1) produise une variation correspondante de la valeur moyenne dudit courant de déviation (i_V) et une variation correspondante du positionnement de la trame sur la face du dispositif d'affichage ; et

un circuit de conduction contrôlable (48) sensible à un signal de commande (i_b) et couplé dans le trajet suivi par ledit courant (i_{L1}) dans ladite inductance (L1) pour redresser ledit courant dans ladite inductance (L1) de sorte que la valeur moyenne dudit courant dans ladite inductance (L1) soit déterminée selon ledit signal de commande (i_b) ; caractérisé par

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des seconds moyens (R1) sensibles audit courant (i_{L1}) dans ladite inductance (L1) pour générer un signal qui est indicateur de l'amplitude dudit courant dans ladite inductance (L1) ; et

un circuit de commande (49) sensible audit signal qui est indicateur de l'amplitude dudit courant dans ladite inductance (L1) pour générer ledit signal de commande (i_b) de telle sorte que ledit circuit de commande (49) et ledit circuit de conduction (48) forment une boucle de rétroaction négative qui régule la valeur moyenne dudit courant (i_{L1}) dans ladite inductance (L1).

2. Dispositif selon la revendication 1 caractérisé par une source (50, Cs) de courant continu couplée audit enroulement de déviation (L_V), ledit courant continu ayant une première partie de courant qui circule dans ledit enroulement de déviation à un niveau qui est égal à la valeur moyenne dudit courant de déviation et ayant une seconde partie de courant qui circule dans ladite inductance (L1).

3. Dispositif selon la revendication 1, caractérisé par un condensateur de tracé (C_s) couplé audit enroulement de déviation (L_V), une source (56-58) de tension d'alimentation et une bobine de self (L2), ladite bobine de self (L2) ayant une première borne (56b) qui est couplée à ladite source (56-58) de tension d'alimentation et une seconde borne (W 10 a) qui est couplée audit condensateur de tracé (C_s) de telle sorte que l'enroulement de déviation (L_V), ledit condensateur de tracé (C_s) et ladite bobine de self (12) soient inclus dans les première, seconde et troisième dérivation comportant une borne de jonction commune (W10a).

4. Dispositif selon la revendication 3 caractérisé en ce que ledit circuit de conduction (48) et ladite inductance (L1) sont inclus dans une quatrième dérivation qui est couplée à ladite borne de jonction commune (W10a).

5. Dispositif selon l'une quelconque des revendications précédentes caractérisé en ce que ledit circuit de conduction contrôlable (48) comprend un redresseur (D2) pour conduire ledit courant dans ladite inductance (L1) quand ledit courant dans ladite inductance (L1) est d'une première polarité et des troisièmes moyens (Q 3) pour conduire ledit courant dans ladite inductance (L1) quand ledit courant dans ladite inductance (L1) est d'une seconde polarité correspondant à la pluralité opposée à la première



re polarité.

6. Dispositif selon la revendication 5 caractérisé en ce que le dit redresseur comprend une première diode (D2). 5
7. Dispositif selon la revendication 6 caractérisé en ce que ledit redresseur comprend de plus une seconde diode (D2a) qui est couplée en série avec ladite première diode (D2). 10
8. Dispositif selon l'une quelconque des revendications 5 à 7 caractérisé en ce que lesdits troisièmes moyens comprennent un transistor (Q3) et dans lequel ledit signal de commande (i_b) est couplé à une électrode de commande (base) dudit transistor (Q3) pour contrôler le courant moyen dudit transistor (Q3). 15
9. Dispositif selon l'une quelconque des revendications 5 à 8 caractérisé en ce que lesdits seconds moyens comprennent une résistance (R1) qui est couplée dans le trajet suivi par courant de ladite inductance (L1) quand ledit courant dans ladite inductance est à ladite polarité opposée et un condensateur (C1) couplé à ladite résistance (R1) pour filtrer, à partir de ladite tension dans ladite résistance, les variations de tension qui surviennent à ladite vitesse de déviation, pour développer, dans ladite résistance (R1), une tension qui est indicatrice de la valeur moyenne dudit courant dans ladite inductance (L1) qui est à ladite polarité opposée. 20
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10. Dispositif selon la revendication 9 caractérisé en ce que ledit condensateur (C1) est couplé en parallèle avec ladite résistance (R1) et dans lequel ledit signal qui est indicateur de l'amplitude dudit courant dans ladite inductance (L1) est généré à travers ladite résistance (R1). 35
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11. Dispositif selon l'une quelconque des revendications précédentes caractérisé en ce que ledit circuit de commande (49) comprend un amplificateur (71) possédant une première borne d'entrée (71a) pour recevoir un signal de réaction qui comprend ledit signal qui est indicateur de l'amplitude dudit courant dans ladite inductance (L1), ledit amplificateur comportant une seconde borne d'entrée (71b) sensible à un second signal d'entrée (V_{REF}) et comportant une borne de sortie (71c) pour générer ledit signal de commande (i_b), selon la différence entre les signaux auxdites premières (71a) et seconde (71b) bornes d'entrée dudit amplificateur (71), pour réguler la valeur moyenne dudit courant dans ladite inductance (L1) selon ledit 45
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second signal d'entrée (V_{REF}).

12. Dispositif selon l'une quelconque des revendications 1 à 7, caractérisé en ce que ledit circuit de conduction (48) comprend un transistor (Q3) qui conduit ledit courant dans ladite inductance (L1) quand ledit courant dans ladite inductance (L1) est à une seconde polarité et dans lequel ledit circuit de commande (49) comprend un amplificateur (71) qui génère à une borne de sortie (71c) dudit amplificateur (71) ledit signal de commande (i_b) qui est couplé à une borne de commande (base) dudit transistor (Q3) pour contrôler la valeur moyenne dudit courant (i_{L1}) dans ladite inductance (L1) qui est à ladite seconde polarité.
13. Dispositif selon l'une quelconque des revendications 1 à 7 caractérisé en ce que ledit circuit de conduction (48) comprend un transistor (Q3) et dans lequel lesdits seconds moyens comprennent une résistance (R1) qui est couplée dans un trajet de conduction du courant principal dudit transistor (Q3) pour former un trajet suivi par le courant qui conduit ledit courant dans ladite inductance (L1) quand ledit courant dans ladite inductance (L1) est à une seconde polarité.