

Description

The present invention relates to a device for protection against the short circuit of an MOS-type power device, with a preset dependance on the temperature at which the power device operates.

The accomplishment of a protection against the short circuit of an MOS-type power device, integrated in the same chip and using only the technology of such power devices, is a requirement which is quite widespread in the market.

The devices for protection against the short circuit currently available on the market depend substantially on temperature. Such a dependance limits the ability to supply current on the part of the power device, even though it may be considered useful for reasons of thermal protection.

DE-A-3 821 065 discloses a MOSFET power device which is provided with a short circuit protection device as defined in the preamble of claim 1.

The object of the present invention is to accomplish a device for protection against the short circuit of an MOS-type power device, wherein the limiting current is a preset function of temperature.

A further object is to accomplish the protection device in integrated technology together with the MOS power device without using any processing stage over in addition to those required for the accomplishment of the standard power device.

According to the invention such object is attained with a device for protection against the short circuit of an MOS-type power device, which includes the further features defined in the characterizing part of claim 1.

The characteristics of the present invention shall be made more evident by an embodiment illustrated as an example in the enclosed drawings wherein:

Fig. 1 illustrates a circuitual accomplishment of the unit consisting of the power device and of the protection device according to the invention;

Figs from 2 to 8 show possible embodiments in integrated technology of the power MOS device and of the components of the protection device.

The circuit shown in Fig. 1 consists essentially of a main branch 1 including a power MOS transistor T1 and two parallel secondary branches 2 and 3 including respective control MOS transistors T2 and T3 having the same characteristics as the power transistor and an ability to conduct a current equal to a fraction (say, one thousandth) of that of the power transistor. The gate and the drain of the power MOS transistor T1 are connected with the gates and with the drains of the control MOS transistors T2, T3. The source of transistor T2 is connected with the base of the NPN bipolar transistor T6 and, by means of resistance R3, with the collector of an NPN bipolar transistor T4. The emitter of transistor T4 is connected by means of a resistance R2 with the source of transistor T1 and with the emitter of an NPN bipolar transistor T5. The base of transistor T4 is connected directly with the corresponding collector and with the base of transistor T5. The collector of transistor T5 is connected with the source of transistor T3 and with the emitter of transistor T6. The collector of transistor T6 is connected with the gate of transistor T3 and, by means of a resistance R1, with a signal input I.

Figure 2 shows a possible embodiment, in integrated technology, of the power MOS transistor T1, whose gate G is accomplished at strips of polysilicon 10, while the source S is accomplished at regions 11 of type N+ which are in turn obtained inside a body region 16 of type P, set on an epitaxial stratum 12 of type N, in its turn obtained on a substratum 17 of type N+, which also constitutes the drain of transistor T1.

Figure 3 shows a possible embodiment, in vertical DMOS integrated technology, of the control MOS transistors T2, T3, whose gate G is accomplished at strips of polysilicon 13, while source S is accomplished at regions 14 of type N+ which are in turn obtained inside a body region 18 of type P set on an epitaxial stratum 15 of type N in its turn obtained on a substratum 19 of type N+ which also constitutes the drain of transistors T2, T3.

Figures 4, 5, 6 illustrate different embodiments in integrated technology of the bipolar transistors T4, T5, T6.

As illustrated in Fig. 4, on a substratum 20 of type N+ there is set an epitaxial stratum 21 of type N, on which there is obtained a body region 22 of type P which forms the base of the single transistor T4, T5, T6, whose collector is obtained in regions 23 of type N+ and whose emitter is obtained in a region 24 of type N+, regions 23 and 24 being obtained at the summit of body region 22.

The characteristics of the single transistor T4, T5, T6 are improvable by adding a type P+ masking and by enriching region 22 during the process stage. As shown in Fig. 5, there is thus formed a further region 25 of type P+ in the proximity of the bottom of region 22.

As an alternative, with reference to Figure 6, it is possible to execute a further phosphorus masking operation with the object of creating a further region 26 of type P- inside region 22 of type P.

With reference to Figure 7, an embodiment in integrated technology of resistances R1, R2, R3 provides for the formation of a region 27 of type N+ accomplished with an arsenic diffusion inside a body region 28 of

type P connected to ground. Such region 28 is obtained on an epitaxial stratum 29 of type N in turn superimposed on a substratum 30 of type N+.

With reference to Figure 8, such resistances R1, R2, R3 may also be accomplished by means of a stratum of polysilicon 31 included in superficial oxide 32.

From Figures 2-8 it is possible to observe that all the components of the protection device (circuit branches 2 and 3 of Fig. 1 with the addition of transistor T6 and of resistance R1) may be accomplished on the same chip as power device T1 without adding any process stages, except of course for those providing improvements of Figures 5 and 6.

Before going on to the description of the operation of the circuit illustrated in Figure 1 it is necessary to make some considerations on the size of the components which have been introduced into the protection device.

A first consideration refers to the fact that the area of transistor T4 is greater than that of transistor T5, so that the current supplied by transistor T4 is normally greater than that supplied by transistor T5.

A further consideration refers to the fact that resistance R2 has been dimensioned so as to cause across its terminals a voltage drop such as to equal the currents flowing through T4, T5 should the current supplied by transistor T2 reach a threshold value above which the triggering of the protection device is required.

With reference to Figure 1, the circuit operates as follows.

Under normal operating conditions, control transistors T2 and T3 are passed through by currents equal to a fraction (say, one thousandth) of that of power transistor T1 and the voltage drop across R2 is such that the current mirrored by T5 is lower than that mirrored by T4, in turn forced by T2. Under these conditions the point A, the base of transistor T6, is at a voltage high. T3, being a current generator accomplished in the same manner as T2, attempts to supply the same current as T2 and thus the collector of T5 is at a voltage high (roughly the drain voltage of T3, T2, T1). Under this condition T6 cannot conduct since the voltage between base and emitter is negative, since the voltage of the emitter of T6 is roughly equal to the drain voltage of transistor T1 and the voltage at the base of T6 is equal to the voltage at point A. There is thus no limitation of current.

Once the current of T2 has reached the threshold value above which it is required to trigger the protection device, that is in the presence of a potential short circuit condition of the power transistor T1, there is a voltage drop across the terminals of resistance R2 which gives the result of equalling the currents flowing through T4, T5. The collector of transistor T5 which is forced to conduct the same current supplied by T3, since $I(T3)=I(T2)$ is always true, and which coincides with the emitter of T6, is lowered in voltage and, as soon as the voltage drop across R2 rises a little more, T6 enters into conduction and accomplishes the protection.

With this circuit it is possible to accomplish a constant temperature protection (or at least with a very low variation less than 9%). It is thus seen that the mechanism triggering the protection is the difference of V_{be} between T5 and T4 which, as is well known, has a positive coefficient of variation with temperature.

If the dependance of such difference of V_{be} with temperature were to be equal to the dependance of R2 with temperature, there would be a protection against short circuits which is independent of temperature, that is constant with temperature.

Thus if a resistance is used which has a positive coefficient of variation with temperature an attempt may be made to obtain the same coefficient of variation of the difference of V_{be} .

The following are some examples of numerical accomplishments of the circuit.

Suppose that the current on the power MOS transistor (T1) is to be limited to 2.75A.

If we suppose that the area of T2, T3 is one thousandth of the area of T1, the current flowing on T2, T3 will always be equal to roughly one thousandth of that flowing on T1.

The example which follows refers to a limitation to 25°C.

Suppose that the ratio between the areas of T4, T5 is 2/1 (this ratio may be chosen at will so that the value of resistance R2 be the most convenient).

The difference of V_{be} for this ratio ($T4/T5=2$) so that the currents in transistors T4 and T5 are balanced is

$$\text{diff. } V_{be} = (KT)/q \times \lg[A(T5)/A(T4)] \times [I(T4)/I(T5)] = 18 \times 10^{-3} \text{V}$$

where

K = Boltzman's constant

q = electron charge

A(T5) = area of emitter T5

A(T4) = area of emitter T4

I(T4) = current of T4 collector

I(T5) = current of T5 collector

then

$$R2 = \text{diff. } V_{be} / I_{L2} = 18 \times 10^{-3} \text{V} / 2.75 \times 10^{-3} \text{A} = 6.540 \text{ ohms}$$

where IL_2 is the limitation current of T2.

R3 is dimensioned so as to ensure across its terminals a voltage drop of about 100mV, so as to ensure a certain dynamic for T5, $R3 = 100mV / 2.75mA = 36.36 \text{ ohm}$, and it may be accomplished in polysilicon.

The size of T6 and R1 may be selected so as to ensure proper operation for a certain current at circuit input I.

Considering that the coefficient of variation of the difference of V_{be} with temperature, with an areas ratio of 10 is $0.2mV/^{\circ}C$, for a ratio of 2 we will have

$$(0.2mV \times 1g2) / 1g10 = 0.06mV/^{\circ}C.$$

Moreover if R2 is accomplished in aluminium, by means of a path similar to that which connects the different elements of the integrated circuit according to the known art, it will have a coefficient of variation with temperature equal to 4500 ppm/ $^{\circ}C$.

Suppose that it is required to bring the device to operate at a temperature of $150^{\circ}C$.

At this temperature the difference of V_{be} to balance the currents of T5 and T4 shall be 25.5mV, R2 shall be equal to 10.21, $IL_1 = IL_2 \times 1000 = 2.5mA$ where IL_1 is T1's current of limitation.

There is thus accomplished a variation of only 9% in the current of limitation against a variation of $125^{\circ}C$ in temperature.

Suppose that it is required to obtain a protection device to have a preset dependance on temperature.

This is possible by replacing resistance R2, accomplished in the previous case in aluminium, with, say, resistances in polysilicon or resistances accomplished by the diffusion of arsenic of type N+, which, having different coefficients of thermal variation, shall ensure different dependencies on temperature.

In particular, since a resistance accomplished with a diffusion of arsenic of type N+ has a coefficient of variation with temperature of about 1500 ppm/ $^{\circ}C$ (against the 4500 ppm/ $^{\circ}C$ of the aluminium resistance), R2, with the same circuit configuration of the previous case, would go from 6.54 ohms to 7.76 ohms.

At the same time the difference of V_{be} , as has already been seen, goes from 18mV to 25.5mV, again for a temperature variation from $25^{\circ}C$ to $150^{\circ}C$.

In this case $IL_1 = 25.5 / 7.76 = 3.28A$.

We will thus, in this case, have a current which increases with temperature.

Similarly, if R2 is accomplished in polysilicon, since the coefficient of variation for silicon is actually negative, there will be an increase in the current of limitation as the temperature rises which is even more pronounced than in the previous case (resistance accomplished by the diffusion of arsenic of type N+).

Claims

1. Device for protection against the short circuit of an MOS-type power device, comprising a first and a second secondary circuit branch (2, 3) arranged in parallel with a main circuit branch (1) including an MOS power transistor (T1), said first secondary branch (2) including a first MOS control transistor (T2) and said second secondary branch (3) including a second MOS control transistor (T3), said MOS control transistors (T2, T3) having the same characteristics as the MOS power transistor (T1) under control and an ability to conduct a current equal to a fraction of that which flows through the MOS power transistor (T1) and having their gates connected directly with that of the MOS power transistor (T1), said first and second secondary branch (2, 3) including also means (T4, T5, T6, R2, R3) sensitive to temperature which, in the case of a current flow corresponding to the short circuit current of the MOS power transistor (T1), act on the gate common to the MOS control and power transistors (T2, T3; T1) so as to lower its voltage and thus limit the conduction of same, characterized in that said means (T4, T5, T6, R2, R3) comprise a first bipolar transistor (T4) inserted in the first secondary branch (2) and a second bipolar transistor (T5) inserted in the second secondary branch (3), said first bipolar transistor (T4) being dimensioned to conduct normally a current greater than that flowing through said second bipolar transistor (T5), said means (T4, T5, T6, R2, R3) comprising in addition a resistance (R2) connected between said first bipolar transistor (T4) and the source of said MOS power transistor (T1) and dimensioned so that the flow of a current corresponding to the short circuit current through the MOS power transistor (T1) causes a voltage drop across it so as to force equal currents through said first and second bipolar transistors (T4, T5), said means (T4, T5, T6, R2, R3) comprising lastly a third bipolar transistor (T6) connected between the common gate of said MOS transistors (T1, T2, T3) and the second bipolar transistor (T5) and with its base connected with a point (A) of said first secondary branch (2) set between said first MOS control transistor (T2) and said first bipolar transistor (T4) so as to lower the gate voltage of the MOS transistors (T1, T2, T3) when said voltage drop is established across said resistance (R2) as a consequence of a short circuit current in the MOS power transistor (T1).



where IL2 is the limitation current of T2.

R3 is dimensioned so as to ensure across its terminals a voltage drop of about 100mV, so as to ensure a certain dynamic for T5, $R3 = 100\text{mV} / 2.75\text{mA} = 36.36 \text{ ohm}$, and it may be accomplished in polysilicon.

The size of T6 and R1 may be selected so as to ensure proper operation for a certain current at circuit input I.

Considering that the coefficient of variation of the difference of Vbe with temperature, with an areas ratio of 10 is $0.2\text{mV}/^\circ\text{C}$, for a ratio of 2 we will have

$$(0.2\text{mV} \times 10) / 10 = 0.06\text{mV}/^\circ\text{C}.$$

Moreover if R2 is accomplished in aluminium, by means of a path similar to that which connects the different elements of the integrated circuit according to the known art, it will have a coefficient of variation with temperature equal to $4500 \text{ ppm}/^\circ\text{C}$.

Suppose that it is required to bring the device to operate at a temperature of 150°C .

At this temperature the difference of Vbe to balance the currents of T5 and T4 shall be 25.5mV , R2 shall be equal to 10.21 , $IL1 = IL2 \times 1000 = 2.5\text{mA}$ where IL1 is T1's current of limitation.

There is thus accomplished a variation of only 9% in the current of limitation against a variation of 125°C in temperature.

Suppose that it is required to obtain a protection device to have a preset dependance on temperature.

This is possible by replacing resistance R2, accomplished in the previous case in aluminium, with, say, resistances in polysilicon or resistances accomplished by the diffusion of arsenic of type N+, which, having different coefficients of thermal variation, shall ensure different dependences on temperature.

In particular, since a resistance accomplished with a diffusion of arsenic of type N+ has a coefficient of variation with temperature of about $1500 \text{ ppm}/^\circ\text{C}$ (against the $4500 \text{ ppm}/^\circ\text{C}$ of the aluminium resistance), R2, with the same circuit configuration of the previous case, would go from 6.54 ohms to 7.76 ohms .

At the same time the difference of Vbe, as has already been seen, goes from 18mV to 25.5mV , again for a temperature variation from 25°C to 150°C .

In this case $IL1 = 25.5 / 7.76 = 3.28\text{A}$.

We will thus, in this case, have a current which increases with temperature.

Similarly, if R2 is accomplished in polysilicon, since the coefficient of variation for silicon is actually negative, there will be an increase in the current of limitation as the temperature rises which is even more pronounced than in the previous case (resistance accomplished by the diffusion of arsenic of type N+).

Claims

1. Device for protection against the short circuit of an MOS-type power device, comprising a first and a second secondary circuit branch (2, 3) arranged in parallel with a main circuit branch (1) including an MOS power transistor (T1), said first secondary branch (2) including a first MOS control transistor (T2) and said second secondary branch (3) including a second MOS control transistor (T3), said MOS control transistors (T2, T3) having the same characteristics as the MOS power transistor (T1) under control and an ability to conduct a current equal to a fraction of that which flows through the MOS power transistor (T1) and having their gates connected directly with that of the MOS power transistor (T1), said first and second secondary branch (2, 3) including also means (T4, T5, T6, R2, R3) sensitive to temperature which, in the case of a current flow corresponding to the short circuit current of the MOS power transistor (T1), act on the gate common to the MOS control and power transistors (T2, T3; T1) so as to lower its voltage and thus limit the conduction of same, characterized in that said means (T4, T5, T6, R2, R3) comprise a first bipolar transistor (T4) inserted in the first secondary branch (2) and a second bipolar transistor (T5) inserted in the second secondary branch (3), said first bipolar transistor (T4) being dimensioned to conduct normally a current greater than that flowing through said second bipolar transistor (T5), said means (T4, T5, T6, R2, R3) comprising in addition a resistance (R2) connected between said first bipolar transistor (T4) and the source of said MOS power transistor (T1) and dimensioned so that the flow of a current corresponding to the short circuit current through the MOS power transistor (T1) causes a voltage drop across it so as to force equal currents through said first and second bipolar transistors (T4, T5), said means (T4, T5, T6, R2, R3) comprising lastly a third bipolar transistor (T6) connected between the common gate of said MOS transistors (T1, T2, T3) and the second bipolar transistor (T5) and with its base connected with a point (A) of said first secondary branch (2) set between said first MOS control transistor (T2) and said first bipolar transistor (T4) so as to lower the gate voltage of the MOS transistors (T1, T2, T3) when said voltage drop is established across said resistance (R2) as a consequence of a short circuit current in the MOS power transistor (T1).



Patentansprüche

1. Vorrichtung zum Schutz einer MOS-Typ-Leistungsvorrichtung, mit einem ersten und einem zweiten Nebenschaltungs Zweig (2, 3), die parallel zu einem Hauptschaltungs Zweig (1) mit einem MOS-Leistungstransistor (T1) angeordnet sind, wobei der erste Nebenzweig (2) einen ersten MOS-Steuertransistor (T2) und der zweite Nebenzweig (3) einen zweiten MOS-Steuertransistor (T3) aufweist und die MOS-Steuertransistoren (T2, T3) die gleichen Eigenschaften wie der gesteuerte MOS-Leistungstransistor (T1) haben und eine Fähigkeit aufweisen, einen Strom zu leiten, der gleich einem Bruchteil des durch den MOS-Leistungstransistor (T1) fließenden Stroms ist, und wobei deren Gates direkt mit dem des MOS-Leistungstransistors (T1) verbunden sind, wobei der erste und der zweite Nebenzweig (2, 3) auch eine auf Temperatur ansprechende Einrichtung (T4, T5, T6, R2, R3) aufweisen, die im Fall eines Stromflusses, der dem Kurzschlußstrom des MOS-Leistungstransistors (T1) entspricht, auf das den MOS-Steuer- und -Leistungstransistoren (T2, T3, T1) gemeinsame Gate wirken, um dessen Spannung herabzusetzen und somit deren Leiten zu begrenzen, dadurch gekennzeichnet, daß die Einrichtung (T4, T5, T6, R2, R3) einen in den ersten Nebenzweig (2) eingefügten ersten Bipolartransistor (T4) und einen in den zweiten Nebenzweig (3) eingefügten zweiten Bipolartransistor (T5) aufweist, wobei der erste Bipolartransistor (T4) so dimensioniert ist, daß er normalerweise einen Strom leitet, der größer ist als der durch den zweiten Bipolartransistor (T5) fließende Strom, daß die Einrichtung (T4, T5, T6, R2, R3) zusätzlich einen Widerstand (R2) aufweist, der zwischen den ersten Bipolartransistor (T4) und die Source des MOS-Leistungstransistors (T1) geschaltet und derart dimensioniert ist, daß der Fluß eines Stroms, der dem Kurzschlußstrom durch den MOS-Leistungstransistor (T1) entspricht, über diesem einen Spannungsabfall bewirkt, derart, daß gleiche Ströme durch den ersten und den zweiten Bipolartransistor (T4, T5) erzwungen werden, daß die Einrichtung (T4, T5, T6, R2, R3) schließlich einen dritten Bipolartransistor (T6) aufweist, der zwischen das gemeinsame Gate der MOS-Transistoren (T1, T2, T3) und den zweiten Bipolartransistor (T5) geschaltet ist und dessen Basis mit einem Punkt (A) des ersten Nebenzweiges (2) verbunden ist, der sich zwischen dem ersten MOS-Steuertransistor (T2) und dem ersten Bipolartransistor (T4) befindet, derart, daß die Gatespannung der MOS-Transistoren (T1, T2, T3) herabgesetzt wird, wenn der Spannungsabfall über dem Widerstand (R2) als eine Folge eines Kurzschlußstroms in dem MOS-Leistungstransistor (T1) festgestellt wird.

Revendications

1. Dispositif de protection contre les courts-circuits d'un dispositif de puissance de type MOS comprenant une première et une seconde branche de circuit secondaire (2, 3) agencées en parallèle avec une branche de circuit principale (1) comprenant un transistor MOS de puissance (T1), la première branche de circuit secondaire (2) comprenant un premier transistor MOS de commande (T2) et la deuxième branche secondaire (3) comprenant un deuxième transistor MOS de commande (T3), les transistors MOS de commande (T2, T3) ayant la même caractéristique de commande que le transistor MOS de puissance (T1) et une capacité à conduire un courant égal à une fraction de celui qui parcourt le transistor MOS de puissance (T1) et ayant leurs grilles connectées directement à celles du transistor MOS de puissance (T1), les première et seconde branches secondaires (2, 3) comprenant également des moyens (T4, T5, T6, R2, R3) sensibles à la température qui, en cas de circulation de courant correspondant au courant de court-circuit du transistor MOS de puissance (T1), agissent sur la grille commune aux transistors MOS de commande et de puissance (T2, T3 ; T1) pour abaisser sa tension et donc limiter sa conduction, caractérisé en ce que lesdits moyens (T4, T5, T6, R2, R3) comprennent un premier transistor bipolaire (T4) inséré dans la première branche secondaire (2) et un deuxième transistor bipolaire (T5) inséré dans la deuxième branche secondaire (3), le premier transistor bipolaire (T4) étant dimensionné pour conduire normalement un courant supérieur à celui circulant dans le deuxième transistor bipolaire (T5), lesdits moyens (T4, T5, T6, R2, R3) comprennent en outre une résistance (R2) connectée entre le premier transistor bipolaire (T4) et la source du transistor MOS de puissance (T1) et dimensionnée de sorte que la circulation d'un courant correspondant au courant de court-circuit à travers le transistor MOS de puissance (T1) provoque une chute de tension à ses bornes propre à forcer des courants égaux dans les premier et deuxième transistors bipolaires (T4, T5), lesdits moyens (T4, T5, T6, R2, R3) comprenant enfin un troisième transistor bipolaire (T6) connecté entre la grille commune des transistors MOS (T1, T2, T3) et le deuxième transistor bipolaire (T5), et dont la base est connectée à un point A de la première branche secondaire (2) disposé entre le premier transistor MOS de commande (T2) et le premier transistor bipolaire (T4) de façon à abais-



ser la tension de grille des transistors MOS (T1, T2, T3) quand la chute de tension est établie aux bornes de la résistance (R2) par suite d'un courant de court-circuit dans le transistor MOS de puissance (T1).

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