

ABSTRACT

ELECTRONIC DEVICE

5 A semiconductor memory includes: a first line; a second line; a
third line; a first memory cell disposed between the first line and the
second line at an intersection region of the first line and the second
line, the first memory cell including a first selection element layer and
a first electrode coupled to the first selection element layer; and a
10 second memory cell disposed between the second line and the third
line at an intersection region of the second line and third second line,
the second memory cell including a second selection element layer
and a second electrode coupled to the second selection element layer,
wherein a threshold voltage of the first selection element layer is
15 greater than a threshold voltage of the second selection element layer,
and a resistance of the second electrode is greater than a resistance
of the first electrode.

FIG. 2B