What is Claimed is:

1. An apparatus, comprising:

a plurality of memory cells coupled to a first access line and to a plurality of second access lines; and

a controller configured to:

apply a first signal to the first access line;

while the first signal is being applied to the first access line:

apply a second signal to a first of the plurality of memory cells via one of the plurality of second access lines; and

apply a third signal to a second of the plurality of memory cells via another of the plurality of second access lines; and

wherein a material implication operation is performed as a result of applying the first signal, the second signal, and the third signal, and wherein a result of the material implication operation is stored on the second of the plurality of memory cells subsequent to application of the third signal; and

wherein the result of the material implication operation corresponds to an output of a negated antecedent being ORed with a consequent of the material implication operation.

2. The apparatus of claim 1, wherein the controller is configured to apply the third signal to the another one of the plurality of second access lines while the second signal is being applied to the one of the plurality of second access lines.

3. The apparatus of claim 1, wherein a value stored on the first of the plurality of memory cells is the antecedent of the material implication operation.

4. The apparatus of claim 1, wherein a value stored on the second of the plurality of memory cells is the consequent of the material implication operation.

5. The apparatus of claim 1, wherein the first and the second of the plurality of memory cells are not coupled to an external load resistor.

6. The apparatus of claim 1, wherein the plurality of memory cells are resistance variable memory cells.

7. The apparatus of claim 6, wherein the resistance variable memory cells comprise at least one of:

a storage element comprising a first chalcogenide material and select element comprising a second chalcogenide material; and

a chalcogenide material serving as both a storage element and a select element.

8. An apparatus, comprising:

a first memory cell coupled to a first access line and to a first of a plurality of second access lines;

a second memory cell coupled to the first access line and to a second of the plurality of second access lines; and

a controller configured to perform a material implication operation on values stored on the first and second memory cells by:

applying a first signal to the first access line for a first period of time;

apply a second signal to the first of the plurality of second access lines for a second period of time, wherein the second period of time is within the first period of time; and

apply a third signal to the second of the plurality of second access lines for a third period of time, wherein the third period of time is within the second period of time; and

wherein a result of the material implication operation is stored on the second memory cell subsequent to the application of the third signal.

9. The apparatus of claim 8, wherein the first and the second memory cells are within an array comprising a plurality of memory cells, and wherein the controller is configured to:

program at least one of the plurality of memory cells to a first logical state by applying a first voltage whose magnitude is greater than a threshold voltage of the at least one of the plurality of memory cells; and

program at least one of the plurality of memory cells to a second logical state by applying a second voltage whose magnitude is greater than a threshold voltage of the at least one of the

plurality of memory cells, wherein a polarity of the second voltage is different than a polarity of the first voltage.

10. The apparatus of claim 8, wherein the first and the second memory cells are directly coupled to an access line decoder such that a load resistor is not used to perform the material implication operation.

11. The apparatus of claim 8, wherein the first, the second, and the third signals are square pulses.

12. The apparatus of claim 8, wherein a voltage magnitude corresponding to the second signal is less than a voltage magnitude corresponding to the third signal.

13. The apparatus of claim 8, wherein the first and the second memory cells are within an array comprising a plurality of memory cells, and wherein the controller is configured to perform a logical operation by, subsequent to performing the material implication operation, performing a number of additional material implication operations, wherein the logical operation is at least one of:

a NOT operation;

a NAND operation;

a NOR operation;

a COPY operation; and

a XOR operation.

14. A method, comprising:

applying a first signal to an access line to which a plurality of memory cells are commonly coupled, wherein a first memory cell of the plurality is coupled to a first of a plurality of second access lines and a second memory cell of the plurality is coupled to a second of the plurality of second access lines;

applying, while the first signal is being applied to the first access line, a second signal to the first of the plurality of second access lines, wherein a voltage applied across the first memory cell as a result of the application of the second signal is sufficient to switch, when the first

memory cell is programmed to a first logical state, the first memory cell from a first resistance state to a second resistance state such that a voltage on the first access line is raised subsequent to the switch of the first memory cell; and

applying, while the first and the second signals are being applied, a third signal to the second of the plurality of second access lines, wherein a material implication operation is performed as a result of applying the signals, and a result of the material implication operation is stored on the second memory cell subsequent to applying the third signal.

15. The method of claim 14, wherein the first logical state is a set state, and wherein a voltage applied across the second memory cell as a result of the application of the third signal is, when the first memory cell is not switched, sufficient to program a logical state of the second memory cell to the set state regardless of a previous logical state of the second memory cell.

16. The method of claim 14, wherein the voltage magnitude applied across the second memory cell is greater than a threshold voltage magnitude of the second memory cell.

17. The method of claim 14, wherein a voltage magnitude applied across the second of memory cell as a result of the application of the third signal is not, when the voltage on the word line is raised subsequent to the switch of the first memory cell, sufficient to change a logical state of the second memory cell.

18. The method of claim 17, wherein the voltage magnitude applied across the second memory cell is equal to or less than a threshold voltage magnitude of the second memory cell.

19. The method of claim 14, wherein a second logical state is a reset state, and wherein the voltage magnitude applied across the first memory cell as a result of applying the second signal is not sufficient to switch those memory cells that are programmed to the reset state such that the voltage on the word line is not affected.

20. The method of claim 19, wherein the voltage magnitude applied across the first memory cell is greater than a threshold voltage magnitude of the first memory cell.

21. The method of claim 14, wherein at least one of the first, second, and third signals are voltage signals.

22. The method of claim 14, wherein:

the first resistance state is a non-conductive state; and

the second resistance state is a conductive state.

23. The method of claim 14, wherein the switched resistance state of the first memory cell does not change a logical state of the first memory cell.

24. A method, comprising:

performing a material implication operation on values stored on one and another of a plurality of memory cells coupled to a first access line by applying a plurality of material implication signals in a particular sequence on the one and the another of the plurality of memory cells, which comprises:

applying a first of the plurality of material implication signals on the first access line;

applying, while the first of the plurality of material implication signals is being applied to the first access line, a second of the plurality of material implication signals on a second access line to which the one of the plurality of memory cells is coupled;

applying, while the second of the plurality of material implication signals is being applied to the second access line, a third of the plurality of material implication signals on a second access line to which the another of the plurality of memory cells is coupled; and

wherein:

a value stored on the one of the plurality of memory cells is an antecedent of the material implication operation;

a value stored on the another of the plurality of memory cells is a consequent of the material implication operation; and

a result of the material implication operation performed on values stored on the one of the plurality of memory cells and the second of the plurality of memory cells is stored in the another of the plurality of memory cells.

25. The method of claim 24, wherein the method includes performing a NOT operation on an input stored on a first of the plurality of memory cells by:

applying the plurality of material implication signals in the particular sequence on a first and a second of the plurality of memory cells, wherein:

the second of the plurality of memory cells is programmed to a reset state prior to applying the plurality of material implication signals; and

a result of the NOT operation is stored on the second of the plurality of memory cells.

26. The method of claim 24, wherein the method includes performing a NAND operation using inputs stored on a first and a second of the plurality of memory cells by:

applying the plurality of material implication signals in the particular sequence on the first and a third of the plurality of memory cells, wherein the third of the plurality of memory cells is programmed to a reset state prior to applying the plurality of material implication signals; and

applying the plurality of material implication signals in the particular sequence on the second and the third of the plurality of memory cells, wherein a result of the NAND operation is stored on the third of the plurality of memory cells.

27. The method of claim 24, wherein the method includes performing a NOR operation on inputs stored on a first and a second of the plurality of memory cells by:

applying the plurality of material implication signals in the particular sequence on the first and a third of the plurality of memory cells, wherein the third and a fourth of the plurality of memory cells are programmed to a reset state prior to applying the plurality of material implication signals;

applying the plurality of material implication signals in the particular sequence on the third and the second of the plurality of memory cells; and

applying the plurality of material implication signals in the particular sequence on the second and the fourth of the plurality of memory cells, wherein a result of the NOR operation is stored on the fourth of the plurality of memory cells.

28. The method of claim 24, wherein the method includes performing a COPY operation on an input stored on a first of the plurality of memory cells by:

applying the plurality of material implication signals in the particular sequence on the first and a second of the plurality of memory cells, wherein the second and a third of memory cells are programmed to a reset state prior to applying the plurality of material implication signals; and

applying the plurality of material implication signals in the particular sequence on the second and the third of memory cells, wherein a result of the COPY operation is stored on the third of the plurality of memory cells.

29. The method of claim 24, wherein the method includes performing a XOR operation on inputs stored on a first and a second of the plurality of memory cells by:

programming a third, a fourth, and a fifth of the plurality of memory cells to a reset state;

copying the input stored on the first of the plurality of memory cells to the third of the plurality of memory cells;

copying the input stored on the second of the plurality of memory cells to the fourth of the plurality of memory cells;

applying the plurality of material implication signals in the particular sequence on the first and the fourth of the plurality of memory cells;

applying the plurality of material implication signals in the particular sequence on the second and the third of memory cells;

applying the plurality of material implication signals in the particular sequence on the third and the fifth of memory cells; and

applying the plurality of material implication signals in the particular sequence on the fourth and the fifth of memory cells, wherein a result of the XOR operation is stored on the fifth of the plurality of memory cells.

30. The method of claim 24, wherein the method includes performing the material implication operation without transferring values corresponding to operands of the material implication operation to sensing circuitry coupled to the memory array.