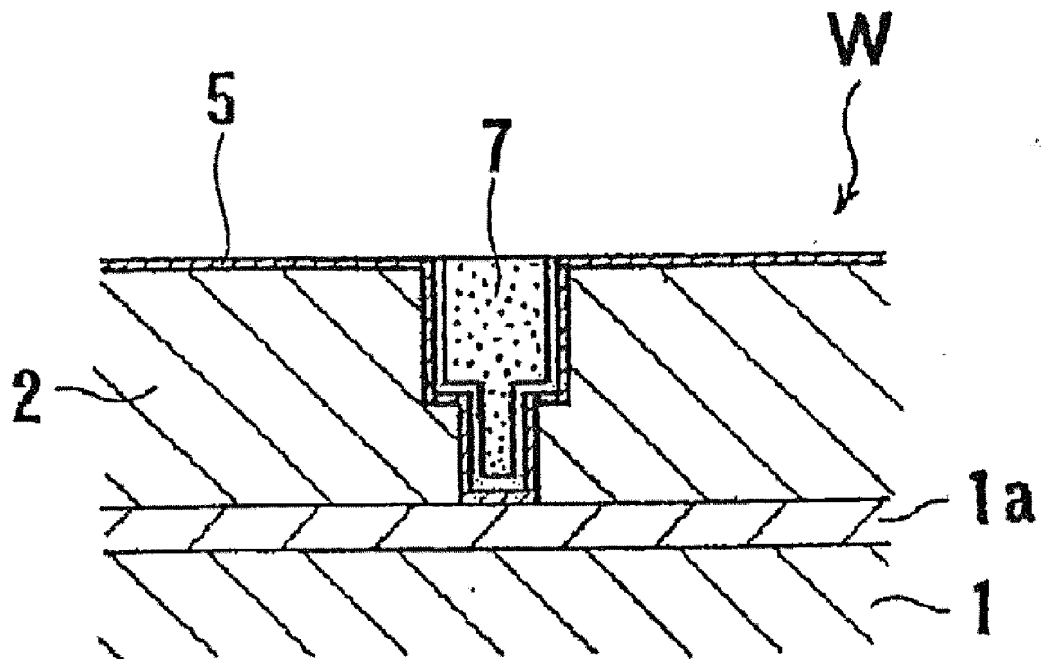
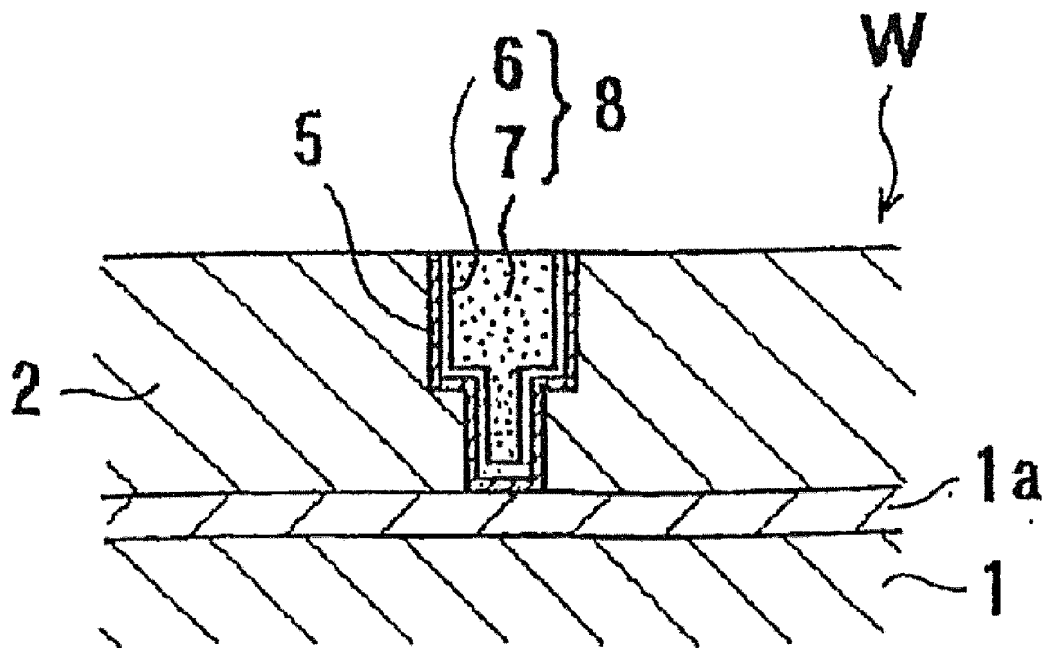


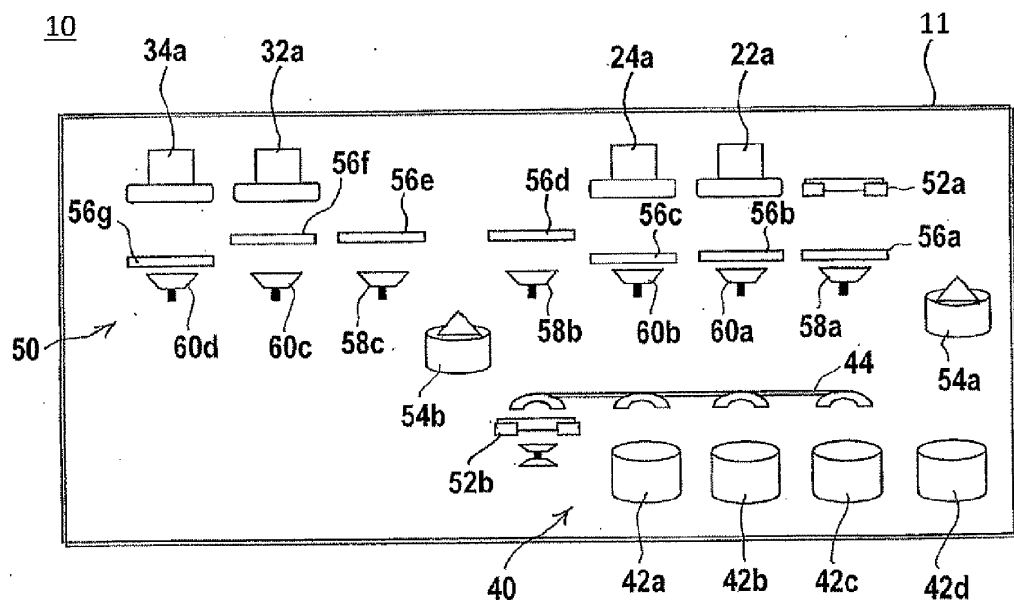
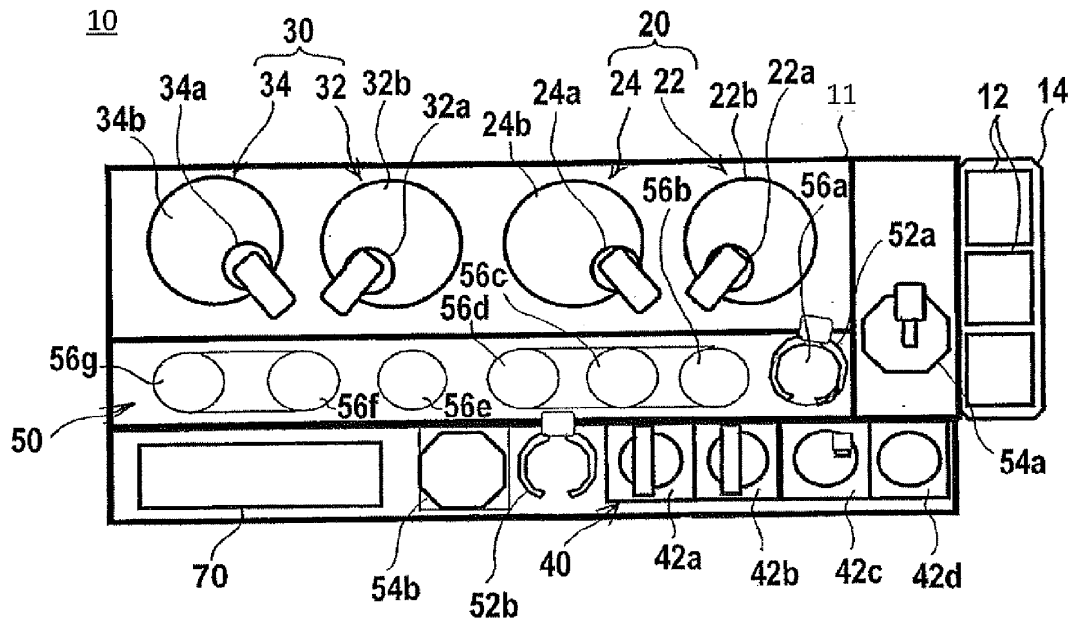
A cross-sectional view of a semiconductor device. A substrate 1 is shown with a layer 1a on its top surface. A trench 2 is formed in the substrate 1. A conductive layer 5 is deposited on the bottom and side walls of the trench 2. A dielectric layer 6 is deposited over the conductive layer 5. A top layer 7 is deposited over the dielectric layer 6. A window W is formed in the top layer 7, exposing the dielectric layer 6 and the conductive layer 5.

[図1C]

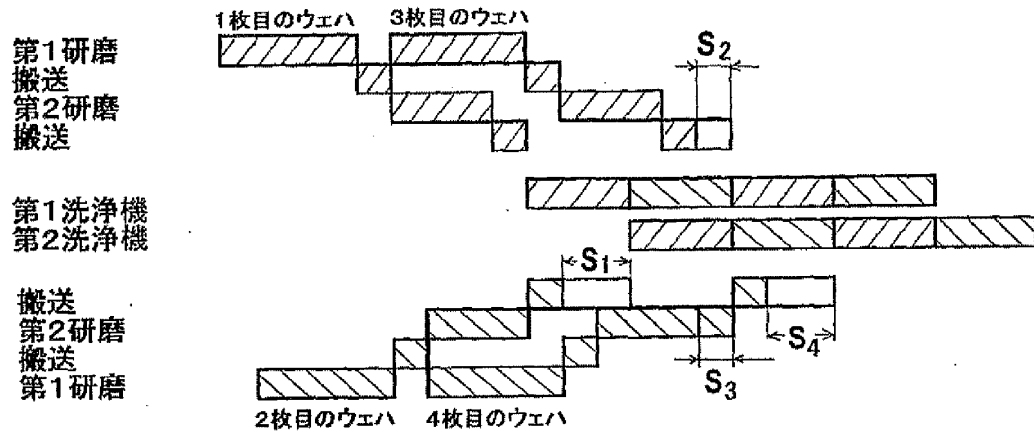


[図1D]

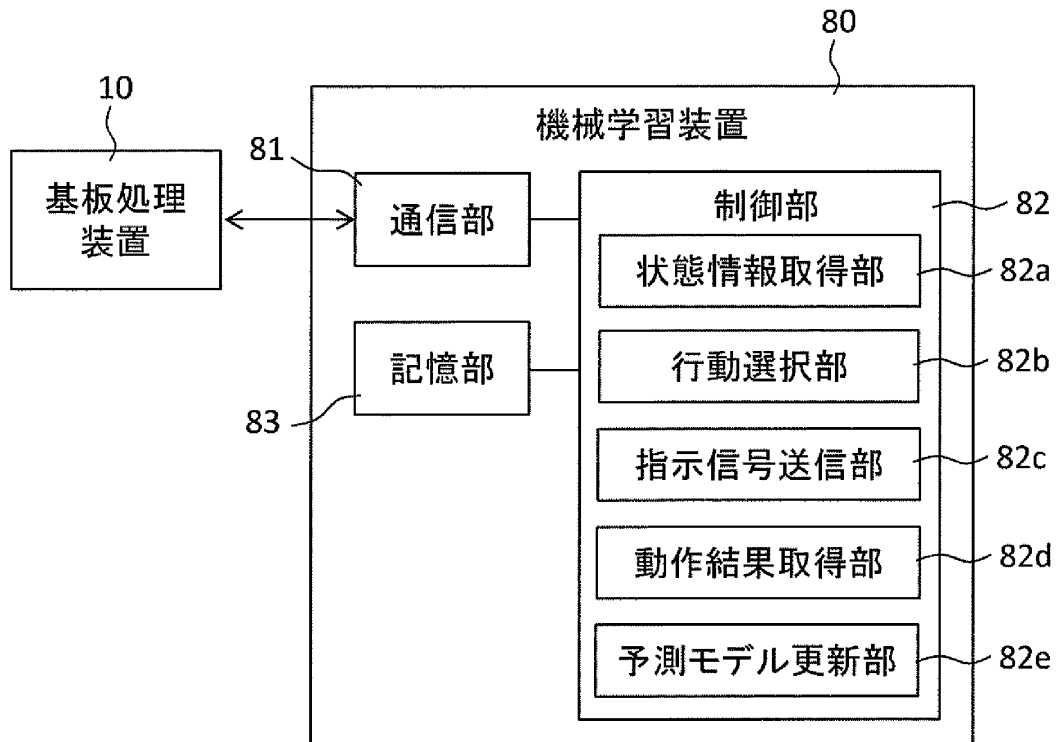




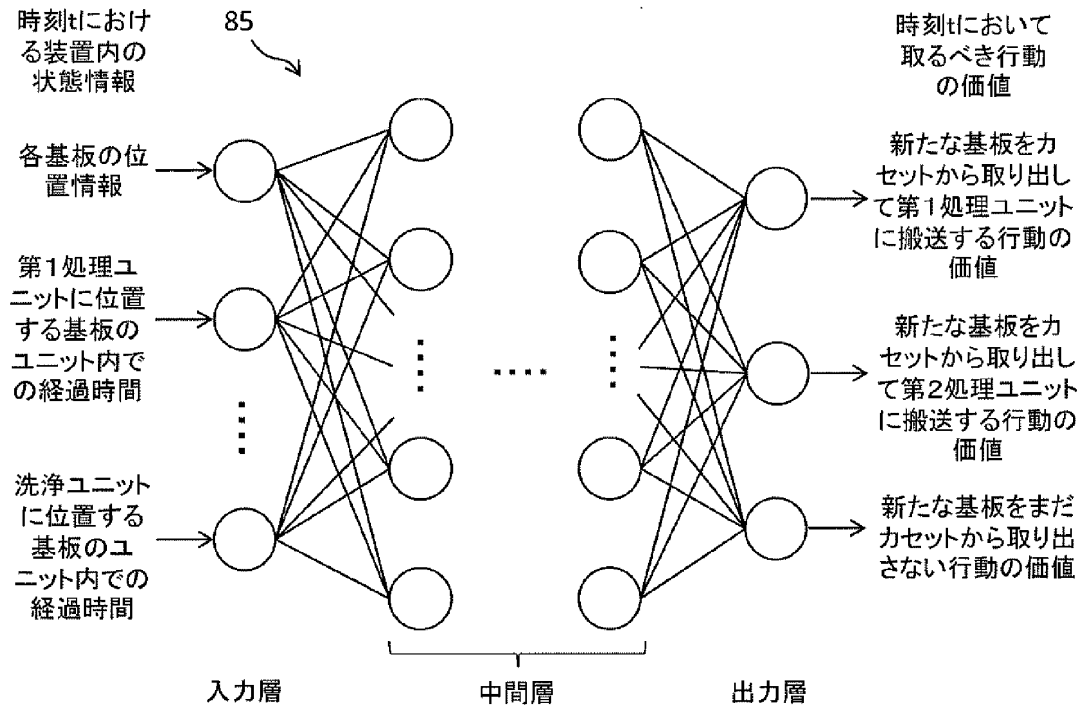
[図4]



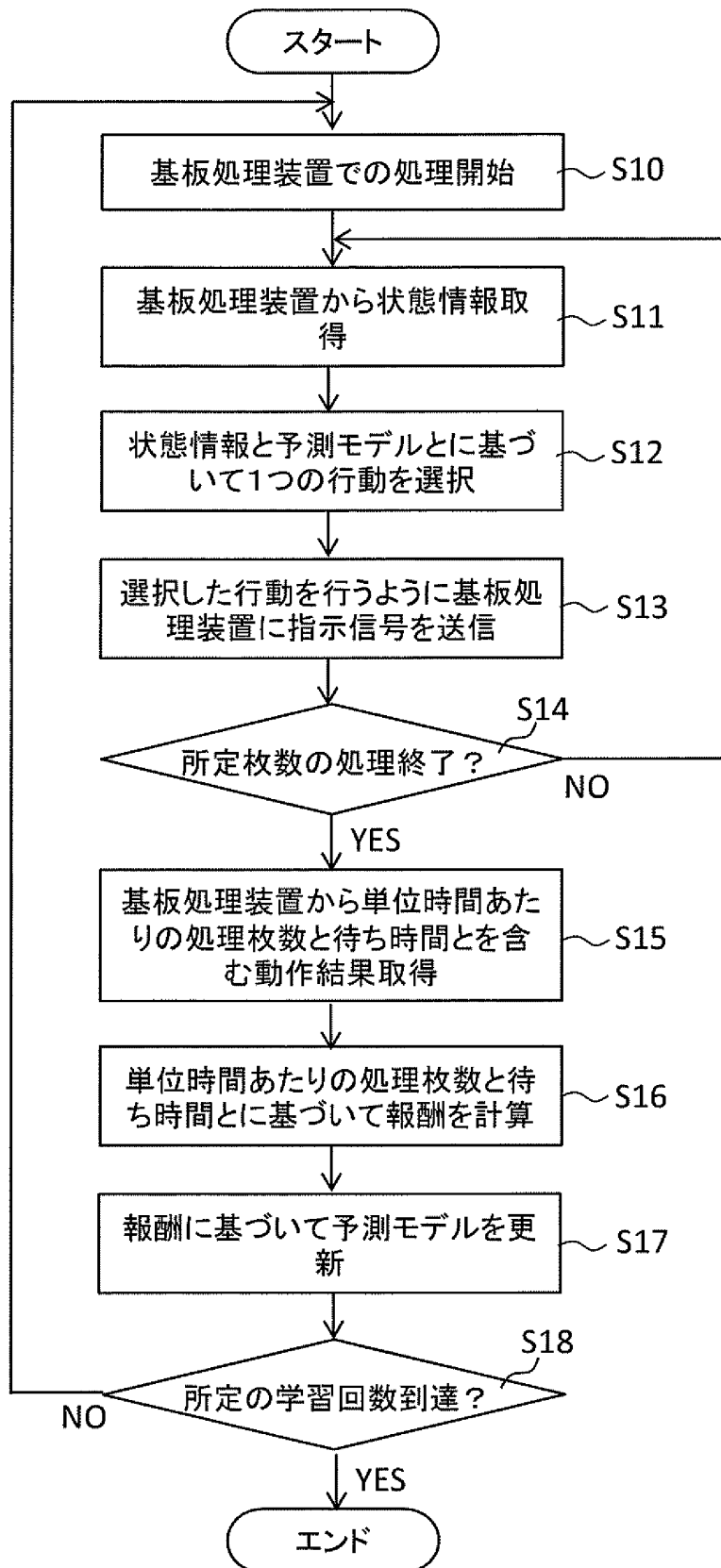
[図5]



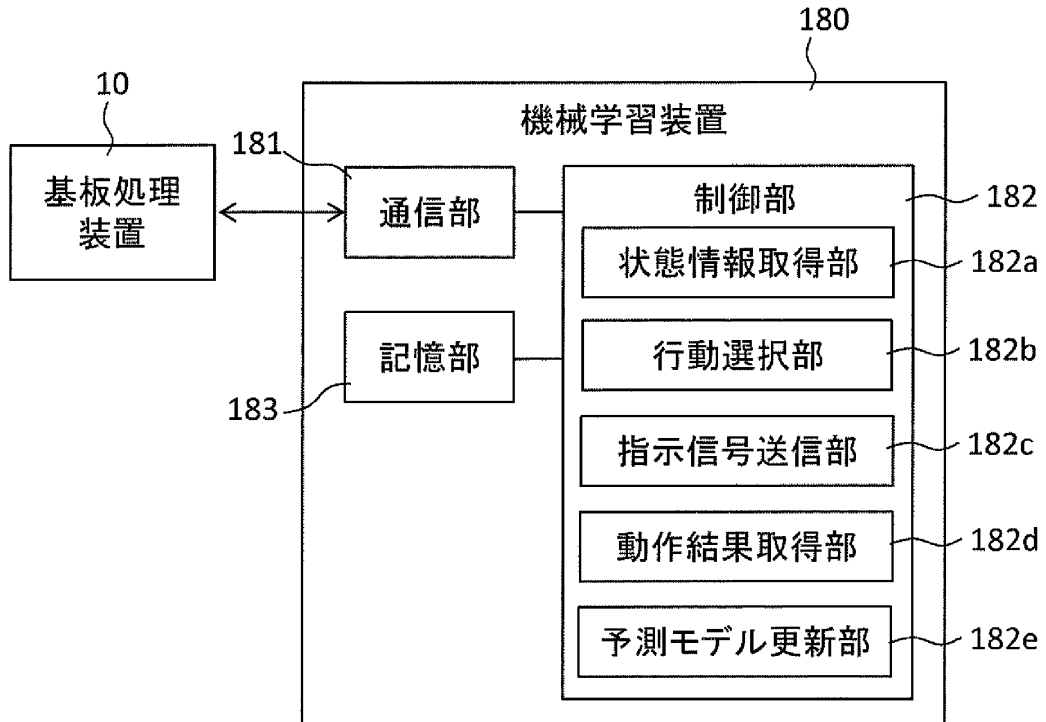
[図6]



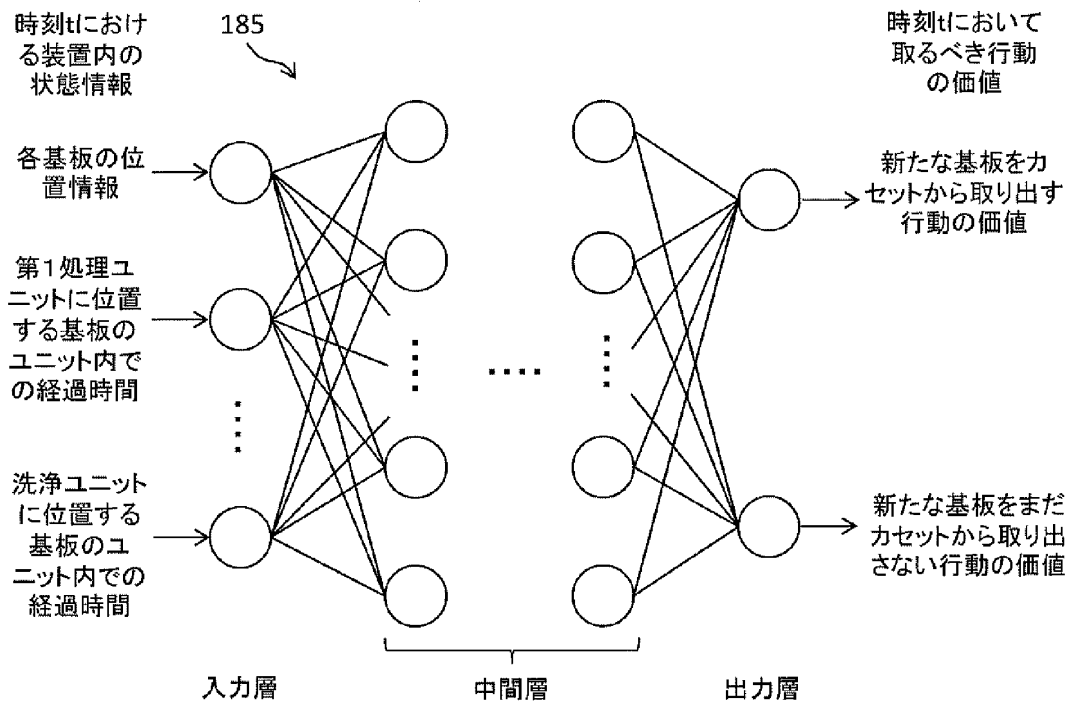
[図7]



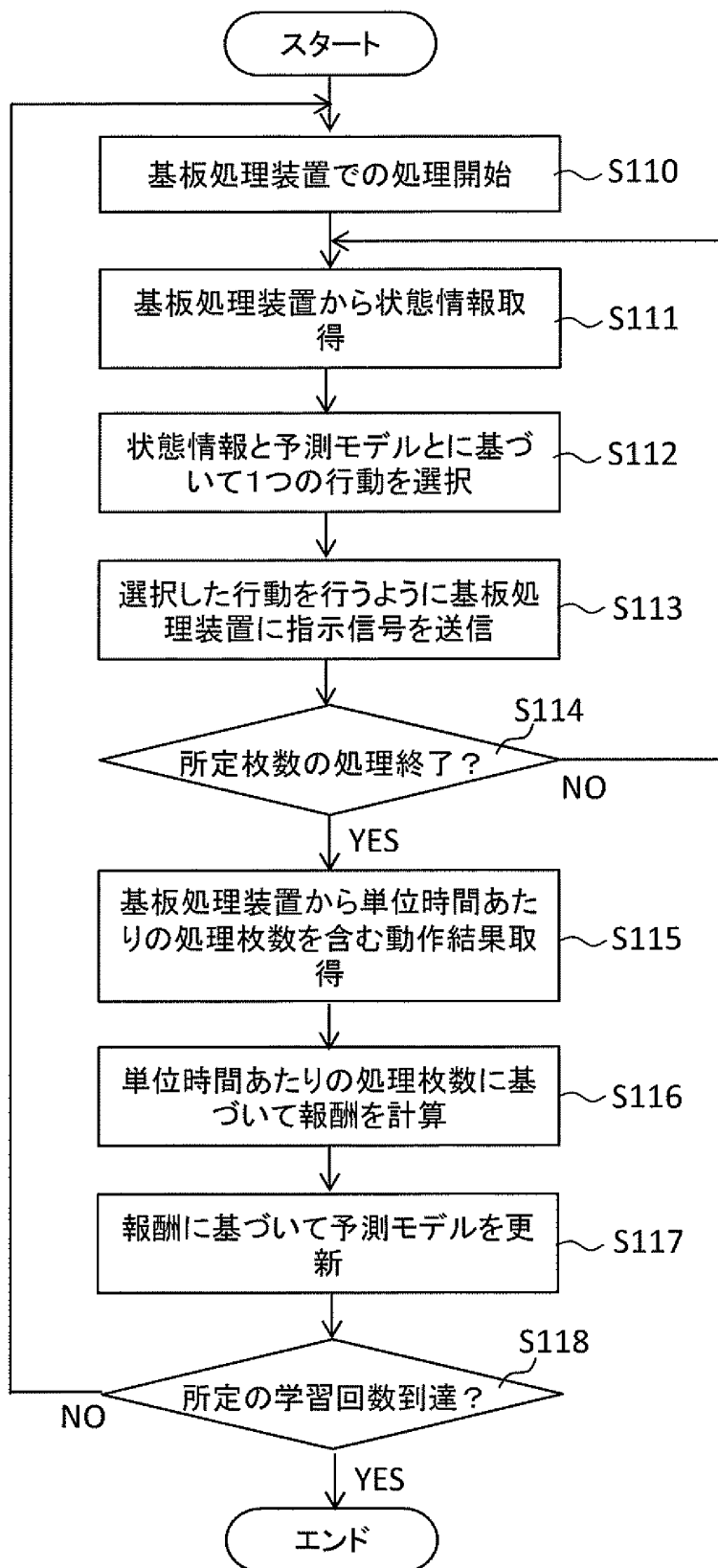
[図8]



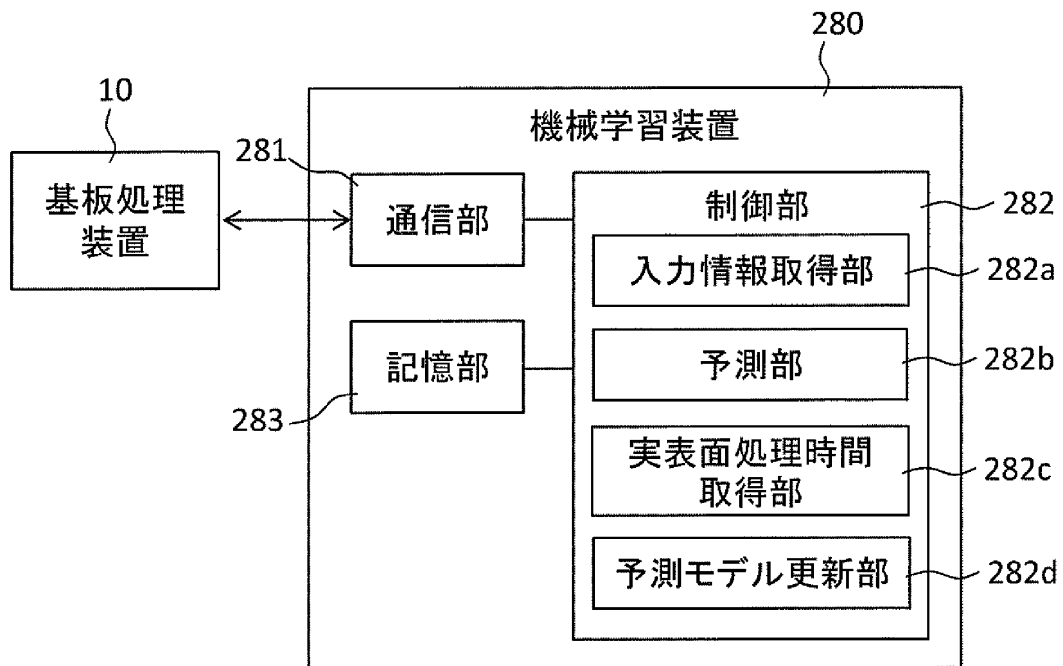
[図9]



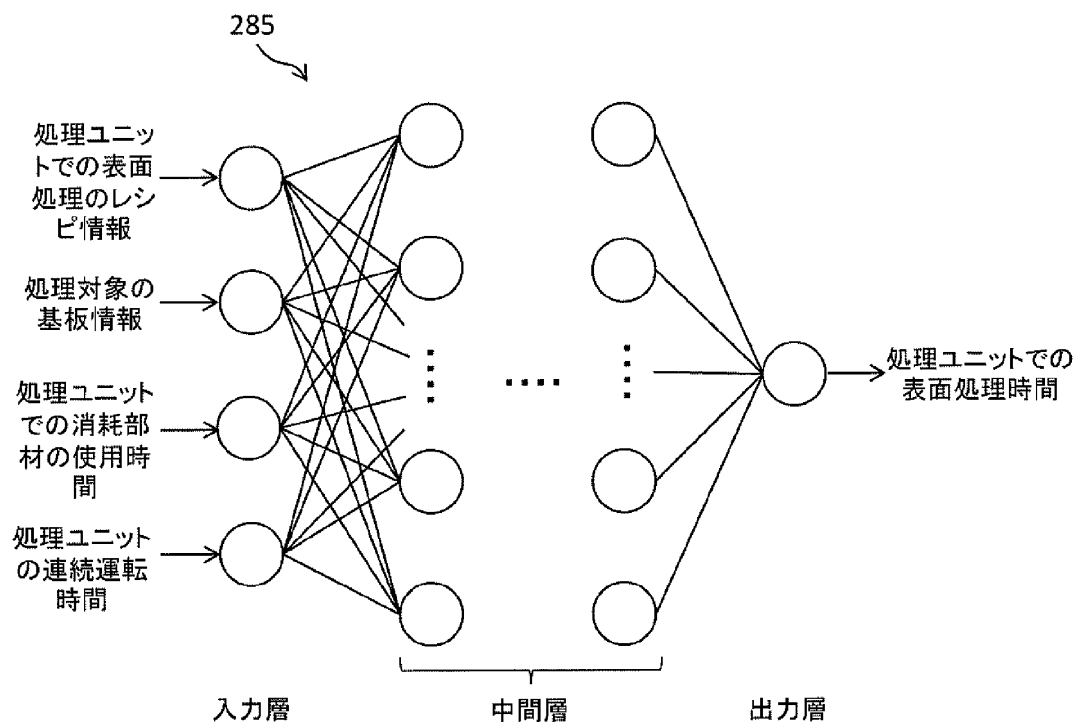
[図10]



[図11]



[図12]



[図13]

