

ABSTRACT

SUPERSCALAR MICROPROCESSOR INSTRUCTION PIPELINE INCLUDING INSTRUCTION DISPATCHING AND KILL CONTROL

An apparatus and method for providing a fast and efficient pipeline in a superscalar microprocessor having a multiple implementation is provided. The pipeline of the present invention quickly matches instructions to be dispatched in a pipeline with available resources. Exceptions occurring in the pipeline are processed efficiently, all in the same pipeline stage, in a uniform manner.

The method comprises predecoding a fetched instruction prior to the fetched instruction being advanced to the instruction decode stage by appending a first field and a second field to the fetched instruction wherein the first field includes resource information extracted from the fetched instruction and the second field includes a resource categorization field identifying a class of resources used by instructions of a type similar to the fetched instruction; and furthermore

dispatching the fetched instruction after advancing it to the instruction decode stage to produce a decoded instruction, the dispatching step using the first field and the second field to route the decoded instruction to a functional unit for processing.

FIG. 6

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