

Claims

1. A non-speculative cache memory in a processor-based system, comprising:
 - a main data array comprising a plurality of cache entries each configured to store cache data associated with a memory address in a memory system of the processor-based system;
 - a speculative buffer memory comprising a plurality of buffer entries each comprising a data entry configured to store cached data associated with a memory address in the memory system; and
 - a cache controller configured to:
 - receive a data request from a requestor comprising a target address and an instruction identification (ID) identifying a load instruction comprising the target address processed by a processor in the processor-based system;
 - search for a cache entry in the main data array associated with the target address of the data request;
 - search the speculative buffer memory for a buffer entry associated with the target address of the data request;
 - send a data response to the data request to the requestor based on cache data in the main data array being associated with the target address and cache data in a buffer entry in the speculative buffer memory being associated with the target address;
 - receive a commit indicator comprising an instruction ID of an instruction that is non-speculative; and
 - in response to the received instruction ID in the commit indicator indicating the load instruction of the data request is non-speculative:
 - update a cache state of a cache entry in the main data array associated with the target address of the data request.
2. The non-speculative cache memory of claim 1, wherein:
 - the cache controller is further configured determine if a cache entry in the main data array is associated with the target address of the data request; and
 - in response to a cache entry in the main data array associated with the target address of the data request, the cache controller is configured to send the data response to the data request to the requestor comprising cache data in the cache entry in the main data array having the target address associated with

the target address of the data request.

3. The non-speculative cache memory of claim 2, wherein the cache controller is configured to, in response to the received instruction ID in the commit indicator indicating the load instruction of the data request is non-speculative, update the cache state comprising a cache replacement state of the cache entry in the main data array associated with the target address of the data request.

4. The non-speculative cache memory of claim 3, further comprising a speculative access record (SAR) circuit configured to store a SAR entry comprising an instruction ID entry and a main data array entry;

wherein, the cache controller is further configured to:

in response to a cache entry in the main data array associated with the target address of the data request, the cache controller is further configured to:

allocate a SAR entry in the SAR circuit, the SAR entry comprising an instruction ID entry comprising the instruction ID of the load instruction of the data request, and a main data array entry comprising an index to a cache entry in the main data array associated with the target address of the data request; and

in response to the received instruction ID in the commit indicator indicating the load instruction of the data request is non-speculative:

determine if the received instruction ID is contained in an instruction ID entry in a SAR entry in the SAR circuit; and

in response to determining the received instruction ID is contained in a SAR entry in the SAR circuit, update the cache replacement state of the cache entry in the main data array corresponding to the index in the main data array entry in the SAR entry containing the received instruction ID.

5. The non-speculative cache memory of claim 2, wherein the cache controller is further configured to, in response to a cache entry in the main data array *not* associated with the target address of the data request:

determine if a buffer entry in the speculative buffer memory is associated with the target address of the data request; and

in response to a buffer entry in the speculative buffer memory associated with the

target address of the data request, the cache controller is configured to send the data response to the data request to the requestor comprising cache data in the buffer entry in the speculative buffer memory having the target address associated with the target address of the data request.

6. The non-speculative cache memory of claim 5, wherein the cache controller is further configured, in response to a buffer entry in the speculative buffer memory *not* associated with the target address of the data request:

send the data request to a next higher level memory in the processor-based system;
receive data for the data request from the next higher level memory;
determine if a buffer entry in the speculative buffer memory is available to store cache data; and

in response to determining a buffer entry in the speculative buffer memory is available to store cache data, write the data for the data request received from the next higher level memory in an available buffer entry in the speculative buffer memory and an available buffer entry associated with the target address of the data request.

7. The non-speculative cache memory of claim 6, wherein the cache controller is configured to, in response to the received instruction ID in the commit indicator indicating the load instruction of the data request is non-speculative:

update the cache state of the cache entry in the main data array associated with the target address of the data request, by being configured to write data for the data request in the buffer entry in the speculative buffer memory associated with the target address of the data request, to a cache entry in the main data array associated with the target address of the data request.

8. The non-speculative cache memory of claim 7, wherein the cache controller is further configured to select a buffer entry among the plurality of buffer entries in the speculative buffer memory to evict from the speculative buffer memory based on the speculative state in non-speculative indicators of the respective buffer entries.

9. The non-speculative cache memory of claim 6, wherein:

each buffer entry in the speculative buffer memory further comprises a non-speculation indicator indicating if the buffer entry is non-speculative; and
the cache controller is further configured to:

in response to a buffer entry in the speculative buffer memory associated with the target address of the data request:

- set a non-speculative indicator in the buffer entry in the speculative buffer memory associated with the target address of the data request to a speculative state;
 - in response to the received instruction ID in the commit indicator indicating the load instruction of the data request is non-speculative:
 - set the non-speculative indicator in the buffer entry in the speculative buffer memory associated with the target address of the data request to a non-speculative state; and
 - in response to the non-speculative indicator in the buffer entry in the speculative buffer memory associated with the target address of the data request being set to a non-speculative state:
 - update the cache state of the cache entry in the main data array associated with the target address of the data request, by being configured to write data for the data request in the buffer entry in the speculative buffer memory associated with the target address of the data request, to a cache entry in the main data array associated with the target address of the data request.
10. The non-speculative cache memory of claim 9, further comprising:
- a speculative access record (SAR) circuit configured to store a SAR entry comprising an instruction ID entry and a virtual fill buffer (VFB) index entry; and
 - a VFB circuit configured to store a VFB entry comprising an instruction ID entry and a VFB index entry;
- the cache controller is further configured to:
- in response to a buffer entry in the speculative buffer memory not associated with the target address of the data request:
 - allocate a VFB entry in the VFB circuit, the VFB entry comprising an instruction ID entry comprising the instruction ID of the load instruction of the data request, and a VFB index entry comprising an index to a buffer entry in the speculative buffer memory associated with the target address of the data request; and
 - allocate a SAR entry in the SAR circuit, the SAR entry comprising the instruction ID entry storing the instruction ID of the load

- instruction of the data request, and the VFB index entry storing an index to a VFB entry in the VFB circuit having an instruction ID entry containing the instruction ID; and
- in response to the received instruction ID in the commit indicator indicating the load instruction of the data request is non-speculative:
- determine a VFB entry in the VFB circuit associated having an instruction ID entry containing an instruction ID indexed, based on an index in the VFB index in a SAR entry in the SAR circuit having an instruction ID entry containing the received instruction ID; and
- determine the buffer entry in the speculative buffer memory associated with the target address of the data request set to a non-speculative state, based on an index in the VFB index entry in the determined VFB entry in the VFB circuit;
- the cache controller configured to:
- set the non-speculative indicator in the buffer entry in the determined buffer entry in the speculative buffer memory associated with the target address of the data request to a non-speculative state.
11. The non-speculative cache memory of claim 10, wherein the cache controller is further configured to, in response to allocating the SAR entry in the SAR circuit:
- determine if another SAR entry contained in the SAR circuit comprises the instruction ID in its instruction ID entry and the VFB index entry in its VFB entry; and
- in response to determining the other SAR entry is contained in the SAR circuit, deallocate the SAR entry in the SAR circuit.
12. The non-speculative cache memory of claim 1, wherein the cache controller is further configured to evict a buffer entry in the speculative buffer memory in response to a cache entry in the main data array being evicted corresponding a memory address corresponding to the buffer entry.
13. A method of updating a cache state in a non-speculative cache memory in a processor-based system, comprising:
- receiving a data request from a requestor comprising a target address and an instruction identification (ID) identifying a load instruction comprising the

target address processed by a processor in the processor-based system;
searching a main data array for a cache entry associated with the target address of the data request among a plurality of cache entries each configured to store cache data associated with a memory address in a memory system of the processor-based system;
searching a speculative buffer memory for a buffer entry associated with the target address of the data request among a plurality of buffer entries each configured to store cache data associated with a memory address in the memory system;
sending a data response to the data request to the requestor based on a cache entry in the main data array being associated with the target address and a cache data in a buffer entry in the speculative buffer memory being associated with the target address;
receiving a commit indicator comprising an instruction ID of an instruction that is non-speculative; and
updating a cache state of a cache entry in the main data array associated with the target address of the data request, in response to the received instruction ID in the commit indicator indicating the load instruction of the data request is non-speculative.

14. The method of claim 13:

further comprising determining if a cache entry in the main data array is associated with the target address of the data request; and
comprising sending the data response to the data request to the requestor comprising cache data in the cache entry in the main data array having the target address associated with the target address of the data request, in response to a cache entry in the main data array associated with the target address of the data request.

15. The method of claim 14, further comprising, in response to a cache entry in the main data array not associated with the target address of the data request:

determining if a buffer entry in the speculative buffer memory is associated with the target address of the data request; and
sending the data response to the data request to the requestor comprising cache data in the buffer entry in the speculative buffer memory having the target address associated with the target address of the data request.