

SIGNAL MASKING CIRCUIT AND SEMICONDUCTOR MEMORY

ABSTRACT

A signal masking circuit and a semiconductor memory are provided. The signal masking circuit includes a receiving circuit, a delay control circuit, and a logical operation circuit. The receiving circuit is configured to: receive a signal to be processed and a chip select (CS) signal, and output an initial processing signal and an initial CS signal. The delay control circuit is configured to perform delay and logical control operations on the initial CS signal to obtain a CS masking signal, where a pulse width of the CS masking signal is greater than or equal to two preset clock periods. The logical operation circuit is configured to perform invalid masking on the initial processing signal according to the CS masking signal to obtain a target signal.

[Fig. 7]