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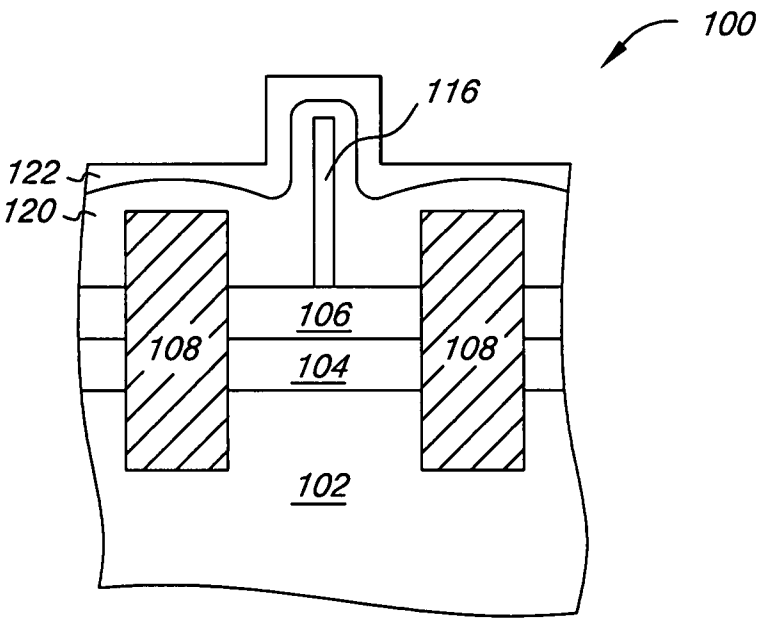
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(57) Abstract: A memory cell (100) is provided including a tunnel dielectric layer (104) overlying a semiconductor substrate (102). The memory cell also includes a floating gate having a first portion (106) overlying the tunnel dielectric layer and a second portion (116) in the form of a nanorod extending from the first portion. In addition, a control gate layer (122) is separated from the floating gate by an intergate dielectric layer (120).

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