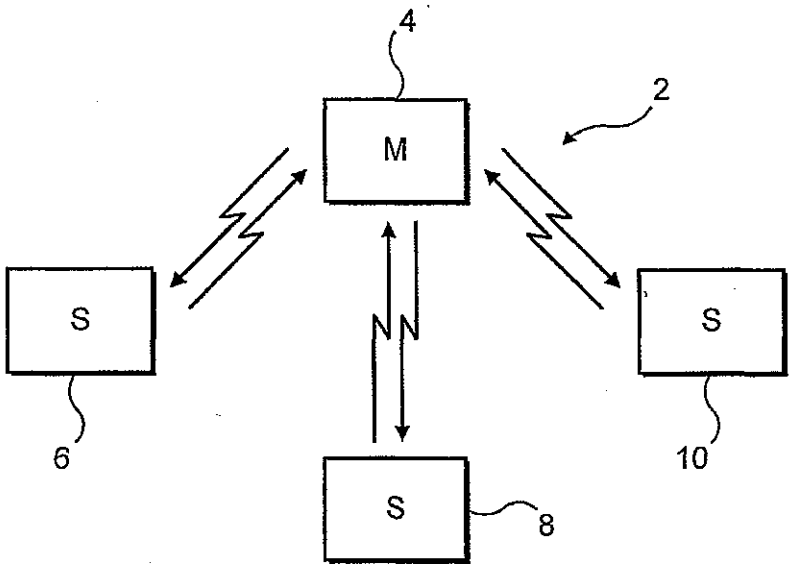



FIG.1

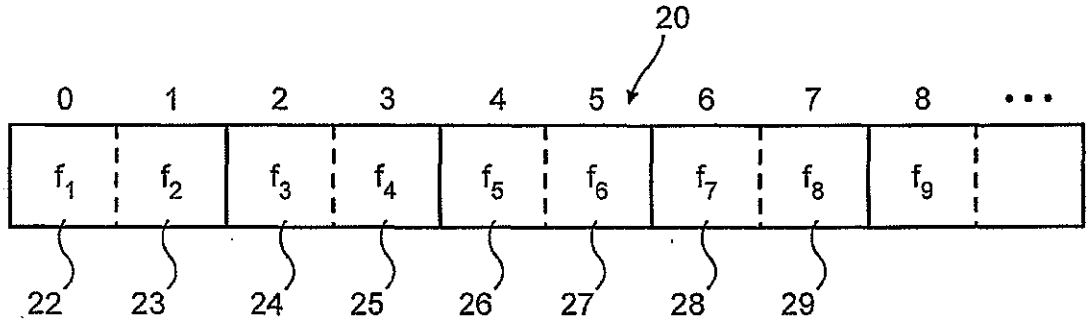



FIG.2

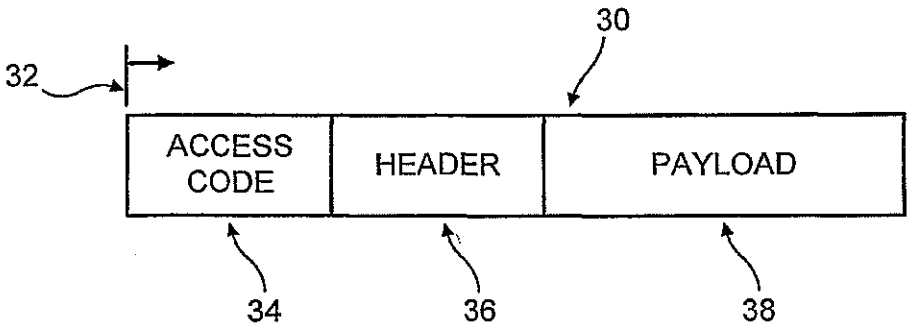



FIG.3

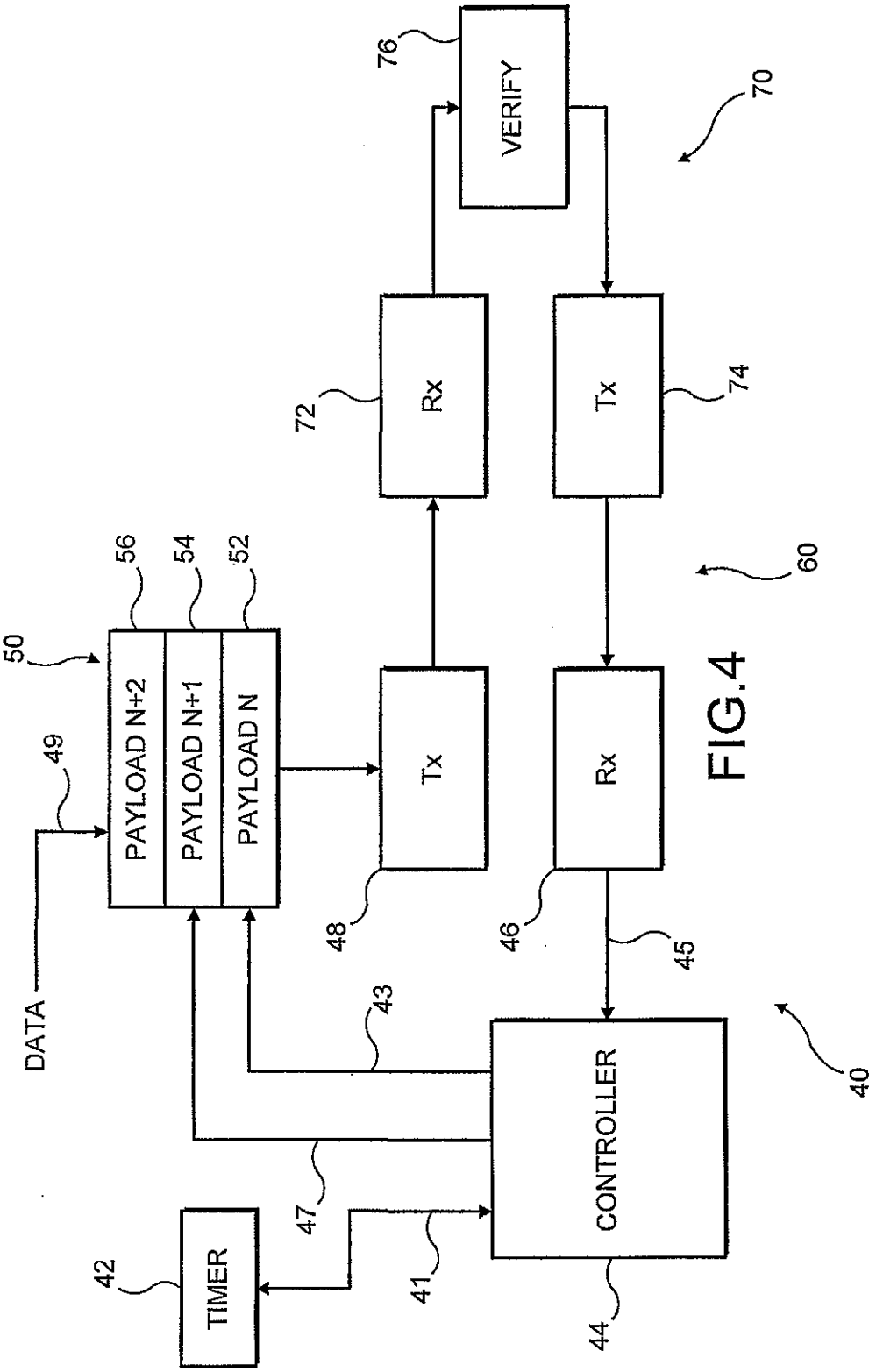

VERIFY
76
70
Rx
72
Tx
74
60
56
54
52
50
PAYLOAD N+2
PAYLOAD N+1
PAYLOAD N
49
Tx
Rx
48
46
45
DATA
43
CONTROLLER
40
47
TIMER
42
41
44

FIG.4

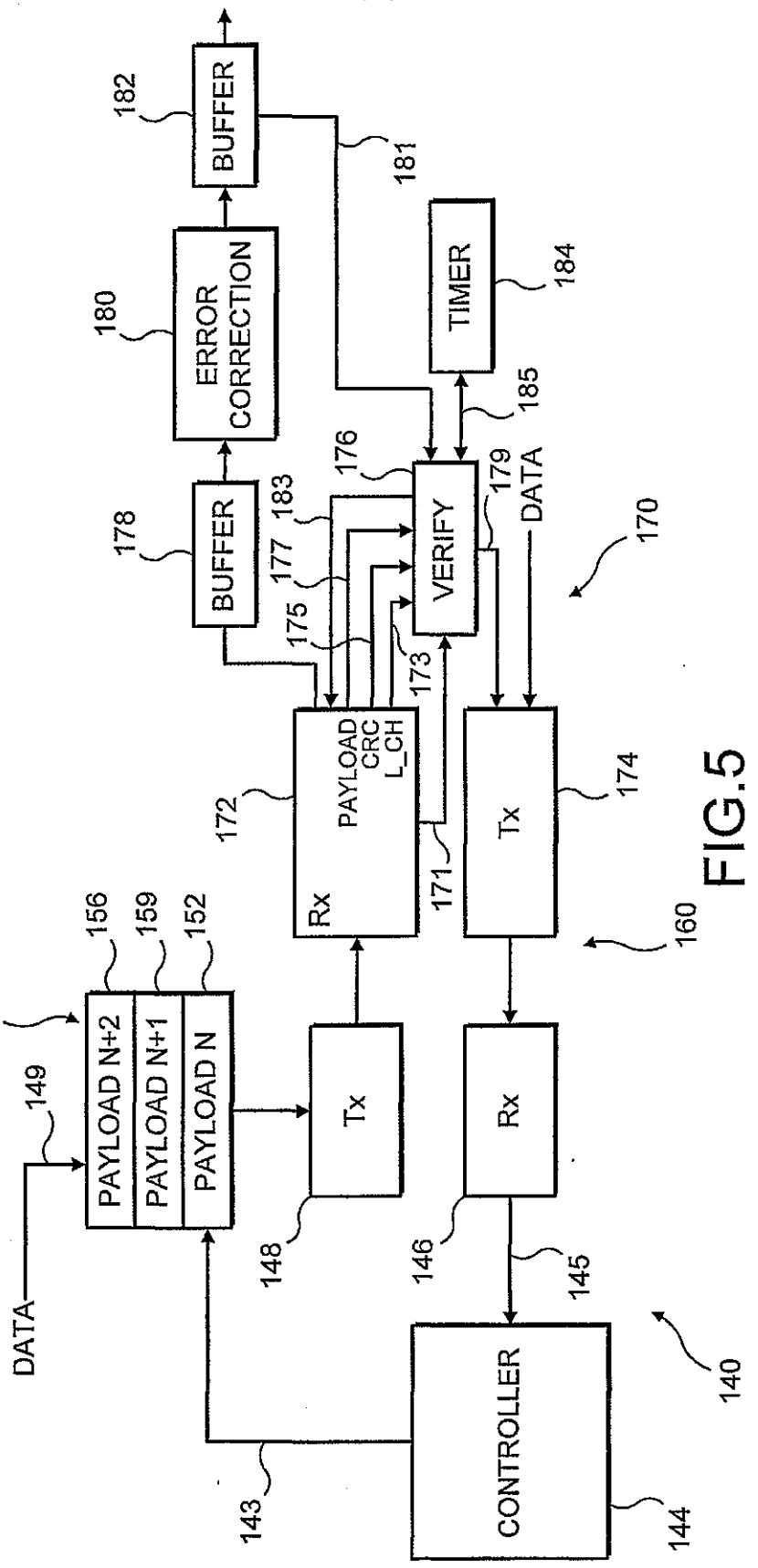

DATA
149
150
PAYLOAD N+2
PAYLOAD N+1
PAYLOAD N
156
159
152
Tx
148
Rx
146
145
CONTROLLER
140
143
144
Rx
PAYLOAD
CRC
L_CH
172
171
Tx
174
160
VERIFY
179
DATA
170
176
183
177
175
173
BUFFER
178
ERROR
CORRECTION
180
BUFFER
182
181
TIMER
184
185

FIG.5