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**A SUBSTRATE HAVING THIN-FILM DIELECTRIC AND CONDUCTOR LAYERS
FORMED THEREON AND METHOD FOR FABRICATING THE SAME**

FIELD OF THE INVENTION

The invention relates generally to thin-film processes, and, more particularly, to a substrate having a thin-film polytetrafluoroethylene (PTFE) dielectric layer and a thin-film metal conductor layer formed on the substrate, and fabricating the same.

BACKGROUND OF THE INVENTION

The current trend of electronic circuits continues towards decreasing size and weight, increasing operational speed, reducing crosstalk and noise, and improving operational reliability.

The development of integrated circuits (ICs) were a major advancement towards downsizing electronic circuits. Typically, ICs are either monolithic or hybrid circuits. A monolithic circuit is an IC that is included entirely on a single piece of semiconductor with insulating layers and metallization patterns bonded to the surface of the chip, while a hybrid circuit is an IC that contains one or more monolithic circuits bonded to an insulating substrate with resistors, capacitors, connectors, and the like. When resistors, capacitors and connectors are made external to a monolithic chip, it is common that these passive elements are fabricated and interconnected by either thick-film or thin-film processes.



In thick-film circuits, the resistors and interconnection patterns are printed on a substrate by silk-screen or similar processes. Conductive and resistive pastes consisting of metal powders in organic binders are printed on the substrate and cured in a curing oven. These conductive and resistive films are typically over 25 microns thick. However, thin-film circuits permit greater precision and miniaturization.

Thin-film interconnection patterns and resistors can be vacuum deposited on, for example, ceramic or glass substrates. Such thin-films are less than 25 microns thick and are typically only 1 to 5 microns thick.

To support a high-speed device, it is desirable to use thin-film integrated circuits having a thin-film metal conductor layer deposited on a thin-film dielectric layer that is formed on a substrate. The dielectric layer acts as an insulator for insulating the metal conductor layer.

Polyimides are known in the art for forming such thin-film dielectric layers. Polyimides have a relatively low dielectric constant ($\epsilon = 3$ to 4) and therefore are widely used for permitting the electronic devices mounted thereon to operate at high speeds. Further, it is known to combine a polyimide dielectric layer with an appropriate metal layer having a small conductive electric resistance, such as copper or aluminum.

For example, a copper-polyimide multi-layer substrate has been used to support high-speed devices. In one such device, a thin-film conductor pattern, formed mainly of copper, having a thickness of about 1 to 10 microns, and a polyimide layer, having a thickness of about 10 microns, are alternately superimposed a plurality of times on

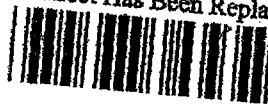


a ceramic substrate. Therefore, in this structure the copper-polyimide combination permits a device mounted thereon to operate at high-speeds due to the low dielectric constant of the polyimide and the small conductive electric resistance of copper.

However, for ultra high-speed, high-frequency applications, such as in superconductors, communications, and radar, the use of a polyimide thin-film as the dielectric layer is fast approaching the maximum frequency which may be applied before there is a loss of insulation. Thus, there is a need to increase the frequency on one hand, while cutting down crosstalk and noise on the other. Further, the polyimide dielectric layer has an inherent disadvantage in that polyimide resins are hygroscopic. This small amount of moisture, that is embedded in all polyimide polymers, are a liability in that the moisture may permeate through the polyimide dielectric layer to the proximate metal elements. Polytetrafluoroethylene (PTFE), on the other hand, allows for the much needed increase in the maximum frequency due to its extremely low dielectric constant ($\epsilon = 2.0$). Additionally, unlike polyimide polymers, the amount of water that is embedded inside the polymer lattice of PTFE is close to zero.

Currently, the state-of-the-art radars and sophisticated telecommunications systems use relatively large copper-on-PTFE wiring boards. However, the precise fabrication of these boards are difficult because copper, as well as other low resistance metals, resists bonding to PTFE. Thus, these Cu/PTFE/Cu boards are fabricated by a mechanical laminating process using adhesives to bind the metal to the PTFE film.

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This lamination process comprises multiple steps and may damage the boards due to the heat and pressure required to bond the PTFE film to the copper. Briefly, the copper laminate is first patterned into electronic circuits using a series of standard photolithographic process steps including the use of photoresists. Thereafter, the copper layers are chemically etched. This process requires five basic lamination process steps and at least eight standard photolithographic process steps. For example, the basic five-step lamination process includes: 1) preparing the copper conductor layers and PTFE or other dielectric films for lamination by, e.g., degreasing and microetching; 2) photolithic patterning and etching the copper layers; 3) drilling
vias through the individual or combination layers; 4) laminating the individual layers by heat and pressure; and 5) copper plating the drilled vias to form interconnects. The basic eight-step photolithographic process includes: 1) vapor priming a copper substrate; 2) spin or spray coating a photoresist on the primed substrate; 3) soft baking the photoresist at approximately 80 °C; 4) exposing the photoresist with UV
light using a patterned mask and aligner; 5) developing the photoresist; 6) hard baking the photoresist at approximately 120 °C; 7) chemically etching the copper layer; and 8) removing the photoresist.

Further, due to the relatively thick copper layers (typically in the mm scale) which are used in the prior art, it is extremely difficult to pattern any circuits close to the micron scale for use in thin-film circuits. In addition, the adhesives used in the lamination process reduces the electrical performance of the PTFE films and increases the overall size of the circuits.



Such use of adhesives in the prior art is necessary since, although PTFE has excellent electrical properties including a very low dielectric constant, its superior non-stick and low frictional properties make it extremely difficult to apply to multi-layer thin-film applications. In fact, PTFE is among the most inert of all plastics.

5 It is therefore an object of the present invention to provide a process of fabricating thin-film combinations of low resistance metal conductors on PTFE dielectric layers, in lieu of polyimide dielectric layers, to yield devices that are far superior in electrical performance and speed.

10 Another object of the invention is to provide a thin-film fabrication process, that, if desired, eliminates the need to pattern the metal conductor layer by standard photolithographic processing steps.

A further object of the invention is to provide a thin-film fabrication process that eliminates the need to use adhesives to bind the metal conductor layer to the PTFE polymer layer via a lamination process.

15 Various other objects, advantages and features of the present invention will become readily apparent from the ensuing detailed description and the novel features which will be particularly pointed out in the appended claims.

SUMMARY OF THE INVENTION

20 These and other objectives are realized by a method for fabricating thin-film layers onto a substrate. Such a multi-layer substrate is particularly useful in ultra high-speed, high-frequency devices. For example, thin-film PTFE-metal layer circuits have



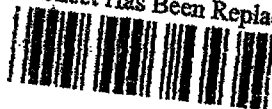
the potential of increasing the speed of today's microprocessors by up to 500 times or more. Specifically in one aspect of the present invention, a substrate is first coated with a thin-film layer dielectric layer, such as PTFE. Next, portions of the PTFE coated surface (where subsequent metalization is not desired) are selectively radiated to cross-link the chemical chains of the PTFE, which forms a chemically inert surface on the exposed portions.

The selected portions of the PTFE coated surface may be radiated with x-rays after an x-ray mask is formed to protect the areas on the surface where subsequent metal depositing is desired. Alternatively, the selected portions of the PTFE coated surface are radiated by writing radiation patterns on the selected portions of the surface using an electron beam mask writer. Subsequently, the coated and radiated PTFE surface is etched to increase friction of the coated and non-radiated portions of the surface, so that the etched surface is not smooth, thereby increasing the frictional properties.

In one embodiment of this aspect of the present invention, a patterned mask layer is then formed on the radiated portions of the PTFE surface for depositing a thin-film metal conductor layer at the openings in the patterned mask layer. Once deposited, the metal conductor layer adheres to the non-smooth etched coated surface.

In another embodiment of this aspect of the present invention, the thin-film metal conductor layer is deposited on the entire coated and selectively radiated PTFE surface. Thereafter, the metal layer may be treated with, e.g., an adhesive tape to

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remove the loosely packed, non-adhering portions of the metal layer, i.e. the metal portions on the radiated portions of the PTFE film.

In another aspect of the present invention, a substrate is first coated with a thin-film layer dielectric layer, such as PTFE. The surface of the PTFE layer is etched to increase its frictional properties. Next, a thin-film metal conductor layer is deposited on the etched surface of the PTFE layer, so that the metal conductor layer adheres to the etched surface of the PTFE layer. The metal layer is subsequently selectively patterned by conventional photolithography and etched.

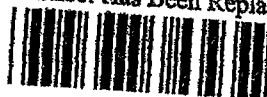
In a further aspect of the present invention, a substrate having a thin-film combination formed thereon is described which includes a thin-film PTFE dielectric layer, coated onto the substrate, having selected portions coarsely etched and the remaining portions radiated, and a thin-film metal conductor layer that is deposited directly on the coarsely etched portions of the PTFE dielectric layer.

All aspects of the present invention include at least one dielectric layer and corresponding metal layer to form multi-layer thin-film circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

The following detailed description, giving by way of example and not intended to limit the present invention solely thereto, will best be understood in conjunction with the accompanying drawing in which:

Fig. 1 illustrates the steps carried out in fabricating thin-film combinations onto a substrate in accordance with various embodiments of the present invention.



DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

As will be described in greater detail with reference to Fig. 1, a thin-film dielectric layer, preferably of PTFE, is coated on the surface of a substrate. The types of substrates that are suitable include metal, glass, silicon, ceramic and plastic. For metal substrates such as titanium, aluminum, and EP copper, the PTFE layer adheres relatively well when the metal surfaces are pretreated by degreasing and microetching. In the case of glass, silicon and ceramic substrates, pretreating the substrate surface with an adhesion promotor prior to coating with the PTFE is desired. Such adhesion promoters include fluorosilane. With respect to plastic substrates, these surfaces are preferably roughened in a pretreatment step by sandblasting or mechanical polishing before coating the PTFE layer. If the plastic used has fluoro-functional groups, no surface treatment or the use of adhesion promoters are necessary to achieve adhesion.

The PTFE resins described in this invention are preferably part of a new family of "amorphous fluoropolymers" based on tetrafluoroethylene copolymerized with 2,2-bistrifluoromethyl-4, 5 difluoro-1, 3 dioxole. Unlike conventional PTFE polymers this new amorphous PTFE is stiffer, exhibits high tensile strength, and is chemically active to perfluorinated solvents, such as fluoro-alkylvinyl ether solvents.

After the PTFE layer is coated on the selected substrate, a thin-film metal conductive layer is selectively formed on the PTFE layer. The metal conductive layer is preferably aluminum, copper, or tungsten, or their alloys, but may also be formed of gold, silver, or other low conductive electric resistance metals.

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Fig. 1 illustrates the fabrication process for forming each thin-film combination onto the substrate. Steps 10, 20, 30, 40, 50 and 60 illustrate a first process in fabricating thin-film device 100. Steps 10, 20, 30, 40 and 65 illustrate a second process in fabricating device 100, while steps 10, 20, 70, 80 and 90 illustrate a third process in fabricating a slightly modified device 100 as will be discussed hereinlater.

In the first process, step 10 shows a liquid PTFE resin 12, that has been sprayed onto the substrate 15 so as to have a thickness preferably ranging from 1 to 25 microns. Alternatively, liquid PTFE resin 12 may be spin-coated onto substrate 15. In Step 20, substrate 15, which is coated with liquid PTFE resin 12, is baked at a temperature of about 112°C for approximately 10 minutes, cured at a temperature of about 175°C for approximately 10 minutes and then at a temperature of about 330°C for approximately 20 minutes. This allows cured PTFE film 22 to be substantially pin-hole free.

In addition, a solid PTFE film (not shown), instead of liquid PTFE resin 12, may be used which eliminates the step of curing and the need for substrate 15.

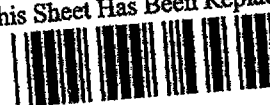
At Step 30, the surface portions on the cured PTFE film 22, where subsequent metallization of the metal conductor layer is not wanted, is treated with radiation by an electron beam emitting electrons $h\nu$ 34. An electron beam mask writer can be used to write the desired patterns directly without a mask onto PTFE film 22 to form irradiated portions 36 that will be immune from having subsequent metal conductive layers permanently formed thereon.



Alternatively, such portions may be radiated with X-rays. If X-rays are used, a patterned X-ray mask is utilized (not shown) to protect the portions where metallization is desired. Thereafter, X-rays are exposed into the unmasked portions of the PTFE film 22 to produce the irradiated portions 36 of coated and radiated PTFE layer 39. By selectively irradiating certain patterns, the polymer chains of the exposed PTFE portions are cross-linked and chemically altered, thus giving a surface that is smooth and inert to chemical attack. Although irradiated portions 36 appear to be cross-linked through the entire depth of PTFE film 22, it should be understood that only the surface of the PTFE film is cross-linked.

At Step 40, the coated and radiated PTFE layer 39 is etched with a commercial etching solution for PTFE polymers, such as fluoroalkylvinyl ethers and perfluorinated FC-75. The etchant solution yields a rough, uneven PTFE surface 45 on etched PTFE layer 49. Since the irradiated portions 36 remain smooth and unetched, as discussed above, they are inert to chemical attack.

At Step 50, a patterned mask 57 is formed over the irradiated portions 36 on the etched PTFE layer 49. Thereafter, at Step 60, metal conductor layers 68, preferably of aluminum or tungsten, is vacuum deposited in the gaps or openings of mask 57 by using a chemical vapor deposition (CVD) at a temperature of approximately 180° - 200°C under high vacuum pressure. Alternatively, the metal conductor layers may be deposited by conventional sputtering or other known processes. For example, details of depositing aluminum thin-films at room temperature

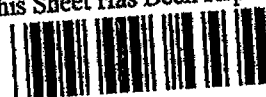


using a non-aqueous electrodeposition process may be found in my earlier U.S. Patent Nos. 4,003,804, 4,071,405 and 4,126,523, fully incorporated herein by reference.

Due to the rough uneven chemically etched portions of etched PTFE layer 49, the thin-film metal conductor layers 68 will adhere securely to PTFE layer 49 in the open gaps of mask 57. To produce thin-film device 100, mask 57 is removed.

In the second process, steps 10, 20, 30 and 40 are followed, as discussed above. The process then proceeds directly to Step 65 by depositing metal conductor layer 68 onto the top surface of PTFE layer 49 by CVD or sputtering, as described in Step 60 above. Note that in this process, a patterned mask 57 is not used. Although the deposited metal layer 68 will cover the entire PTFE layer 49, metal layer 68 will only adhere securely to the rough, uneven chemically etched portions 45 of PTFE layer 49. The portions of conductive metal layer 68 which do not adhere to the virtually non-stick and low frictional irradiated cross-linked portions 36 of layer 49, are easily removed by treating layer 68 with, for example, an adhesive tape, yielding device 100.

Accordingly, the two above-described process sequences selectively deposit thin-film patterns of conductor metals onto the PTFE film without the use of photoresist polymers or the need to utilize normal photolithographic processes. Thus, fabrication using a subtractive process, that requires at least 8 additional steps, is avoided. The use of photolithography not only is time consuming, but also more costly and is extremely difficult to pattern close to the micron scale in the case of the PTFE laminates. However, the above notwithstanding, since photolithography is still



one of the most utilized fabrication techniques, this invention includes an inventive third process that includes photolithographic processes, as describe below.

Steps 10 and 20 are first performed, followed by step 70. At Step 70, the cured PTFE film 22 from Step 20, is chemically etched with, e.g., Fluoroalkylvinyl Ether or Perfluorinated FC-75, as in Step 40, to yield layer 72. At Step 80, the metal
5 conductive layer 68 is vacuum deposited by using CVD or sputtering similar to Step 60. Then, at Step 90, photoresist 97 is formed on metal layer 68 by conventional photolithographic processes.

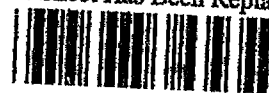
After completion of Step 90, the conductive metal layer 68 is selectively
10 chemical etched (or dry plasma etched) through the open gaps of photoresist 97. The final step involves stripping off photoresist 97 to yield a slightly modified device 100. Specifically, the third process yields device 100 without cross-linked surfaces 36.

The thin-film combination, 49, 68, of device 100, formed on substrate 15 by the processes described above, which uses a PTFE polymer as the dielectric layer in
15 place of polyimides, yields devices that are superior in electrical performance and speed. It should be appreciated that although the processes of FIG 1 only show that a single thin-film combination is fabricated, each process may be repeated from step 10 to form multi-layer thin-film combinations, as desired.

While several embodiments have been chosen to illustrate the invention, it will
20 be understood by those skilled in the art that various changes and modifications can be made herein without departing from the scope or spirit of the invention as defined in the appended claims.



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WHAT IS CLAIMED IS:

1. A method for fabricating thin-films onto a substrate, comprising the steps of:

coating a dielectric compound layer onto said substrate, the compound coated
5 surface acting as a thin-film dielectric layer;

selectively radiating portions of said compound coated surface to cross-link the
chemical chains of said compound which forms a chemically inert surface on the
exposed portions;

etching the coated and radiated surface to increase the frictional properties of
10 said coated surface, such that the frictional properties of said coated surface is greater
than the frictional properties of said radiated surface; and

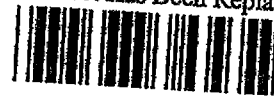
depositing a thin-film metal conductor layer on the etched coated surface, such
that said metal conductor layer adheres to said etched coated surface.

15 2. The method of claim 1, wherein said dielectric compound is PTFE, said
PTFE being one of polytetrafluoroethylene and amorphous fluoropolymers.

3. The method of claim 2, further comprising the step of forming a patterned
mask layer on the radiated portions of the compound surface, such that said metal
20 conducting layer being deposited at the openings in said patterned mask layer.



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4. The method of claim 3, wherein said thin-film conductor layer comprises at least one of aluminum, copper and tungsten.

5. The method of claim 2, wherein said thin-film metal conductor layer being
5 selected from the group consisting of aluminum, tungsten, copper, gold or silver.

6. The method of claim 2, further comprising the step of removing said patterned mask after depositing said metal conductor layer.

10 7. The method of claim 2, wherein said PTFE, coated on said substrate, is a liquid PTFE resin.

8. The method of claim 2, wherein the step of coating said PTFE layer, comprises the steps of:

15 one of spraying and spin coating said liquid PTFE resin onto the surface of said substrate,

baking the PTFE coated substrate at a temperature of approximately 112 °C, and

curing the PTFE coated substrate in a high temperature cure oven.

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9. The method of claim 6, wherein the temperature of said cure oven ranges between approximately 175 °C to 330 °C, and said PTFE coated substrate being cured for approximately 1 hour.

5 10. The method of claim 2, wherein said PTFE, coated on said substrate, is a solid PTFE film.

11. The method of claim 2, wherein the step of selectively radiating, comprises the steps of:

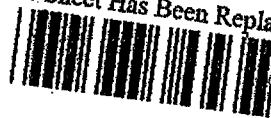
10 forming a patterned X-ray mask on said PTFE coated surface so that only the selected portions of the surface are exposed to radiation,
exposing the masked PTFE coated surface with X-rays, and
removing said X-ray mask from the radiated PTFE coated surface.

15 12. The method of claim 2, wherein the step of selectively radiating comprises the step of writing radiation patterns on the selected portions of said PTFE coated surface using an electron beam mask writer.

20 13. The method of claim 2, wherein the step of etching chemically etches said coated and radiated surface with a liquid etching solution.



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14. The method of claim 2, wherein the step of depositing a thin-film metal conductor layer deposits said metal conductor layer by chemical vapor deposition (CVD) performed in a vacuum at a temperature of approximately 180° to 200°C.

5 15. The method of claim 1, further comprising repeating said coating, radiating, etching and depositing steps at least one time to produce multi-layer thin-film combinations on said substrate, wherein each repeated coating step coats said dielectric compound layer onto said metal conductor layer.

10 16. The method of claim 2, further comprising the step of treating the deposited metal conductor layer with an adhesive tape for removing the non-adhering portions of said metal conductor layer from the radiated portions of said PTFE layer.

15 17. A substrate having a thin-film combination formed thereon, comprising:
a thin-film dielectric compound layer, coated onto said substrate, having selected portions etched and the surface of the remaining portions radiated; and
a thin-film metal conductor layer that is deposited directly on the coarsely etched portions of said compound dielectric layer.

20 18. The substrate of claim 17, wherein said dielectric compound is PTFE, said PTFE being one of polytetrafluoroethylene and amorphous fluoropolymers.



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19. The substrate of claim 18, wherein said substrate further comprises additional PTFE and metal conductor layers superimposed a plurality of times.

20. The substrate of claim 19, wherein said PTFE dielectric layer has a
5 thickness ranging approximately from 1 micron to 25 microns.

21. The substrate of claim 19, wherein said metal conductor layer comprises at least one of aluminum, copper and tungsten.

10 22. The substrate of claim 19, wherein said metal conductor layer being selected from the group consisting of aluminum, tungsten, copper, gold or silver.

23. A substrate having a thin-film combination formed thereon, comprising:
at least one thin-film PTFE layer, wherein the first of said at least one PTFE layer
15 being coated on said the surface of said substrate, each of said at least one PTFE layer being selectively etched; and

at least one metal conductor layer, corresponding to each at least one PTFE layer, deposited directly on each corresponding PTFE layer.

20 24. A method for fabricating thin-films onto a substrate, comprising the steps of:



coating a dielectric compound layer onto said substrate, the compound coated surface acting as a thin-film dielectric layer;

etching the surface of said dielectric compound layer to increase its frictional properties;

5 depositing a thin-film metal conductor layer on the etched surface of said dielectric compound layer, such that said metal conductor layer adheres to said etched surface; and

selectively patterning said metal conductor layer by conventional photolithography.

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25. The method of claim 24, wherein said dielectric compound is PTFE, said PTFE being one of polytetrafluoroethylene and amorphous fluoropolymers.

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26. The method of claim 25, wherein said thin-film conductor layer comprises at least one of aluminum, copper and tungsten.

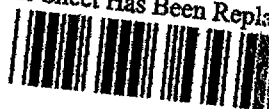
27. The method of claim 25, wherein said thin-film metal conductor layer being selected from the group consisting of aluminum, tungsten, copper, gold or silver.

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28. The method of claim 25, wherein said PTFE, coated on said substrate, is a liquid PTFE resin.



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29. The method of claim 25, wherein the step of coating said PTFE layer, comprises the steps of:

one of spraying and spin coating said liquid PTFE resin onto the surface of said substrate,

5 baking the PTFE coated substrate at a temperature of approximately 112 °C, and
curing the PTFE coated substrate in a high temperature cure oven.

30. The method of claim 29, wherein the temperature of said cure oven
10 ranges between approximately 175 °C to 330 °C, and said PTFE coated substrate being cured for approximately 1 hour.

31. The method of claim 25, wherein said PTFE, coated on said substrate, is a solid PTFE film.

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32. The method of claim 25, wherein the step of etching chemically etches said PTFE layer with a liquid etching solution.

33. The method of claim 25, wherein the step of depositing a thin-film metal
20 conductor layer deposits said metal conductor layer by chemical vapor deposition (CVD) performed in a vacuum at a temperature of approximately 180° to 200°C.

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34. The method of claim 24, further comprising repeating said coating, etching, depositing and patterning steps at least one time to produce multi-layer thin-film combinations on said substrate, wherein each repeated coating step coats said dielectric compound layer onto said metal conductor layer.

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35. The method of claim 25, wherein the step of selectively patterning includes forming a photoresist pattern having open gaps on said metal layer and etching said metal layer through said open gaps of said pattern.